A 380µW Rx, 2.6mW Tx 433MHz FSK Transceiver with a 102dB Link Budget and Bit-Level Duty Cycling

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***Abstract*— This paper presents a low-power, long-range 433MHz transceiver designed for 2-FSK modulation at 1kbps in 8 different physical channels capable of communicating with a Texas Instruments CC1101. Designed in a 130nm CMOS process with an area of 1.1mm^2, the transmitter's output power is 0dBm and the receiver has a sensitivity of -102dBm producing a link budget >100dB and a theoretical range >5km assuming 1/d^2 path loss. Low transmitter power is achieved using a 0.5V Class-E PA and low receiver power is achieved by implementing a digitally-assisted demodulator with further power reduction achieved through bit-level duty cycling with an off power of 110nW.**

***Index Terms*—Low power radios, Internet of Things, duty cycling, FSK**

I. Introduction

Home automation and the industrial Internet of Things (IoT) have benefited from double-digit annual growth rates since 2010, largely because wireless connectivity of these devices has simplified their installation and reduced costs. Sub-1GHz frequency radios are used in these applications for better penetration through multiple walls, where WiFi radios in the 2.4GHz and 5GHz bands suffer. Mesh networking is also used to extend the range of these networks; nevertheless around 100dB link budgets are often required for robust operation in worst-case scenarios [1]. For example, the Texas Instruments CC1101 provides a 118dB link budget at 433MHz at a power consumption of 48mW [2]. For battery-operated sensors such as passive infrared motion detectors, temperature, or smoke sensors, the majority of the energy is consumed by the radios [3]. For these sensors, the battery, and the cost to replace the battery, is the most expensive component and extending battery lifetime (or eliminating batteries altogether) by lowering the power of the radio becomes a top priority.

This paper addresses that need by presenting a 433MHz 2-FSK wireless transceiver (LRTRx) capable of km-range communication at 1kbps in 8 different physical channels. The transmitter has an overall efficiency of 38.9% with 0dBm output power and the receiver has a power of 378µW with a sensitivity of -102dBm for a link budget of 102dB. Low receiver power is achieved by implementing a digitally-assisted, analog 2-FSK demodulator, and power can be further reduced through both bit-level and packet-level duty cycling with 110nW sleep power.

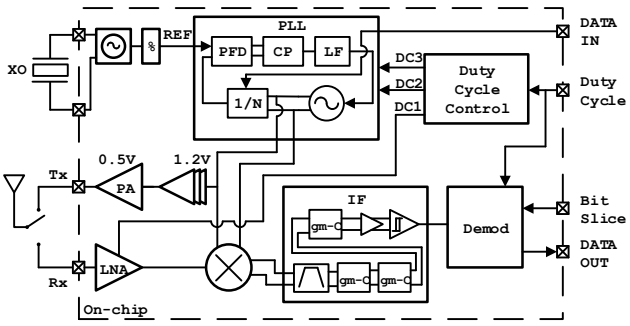

Figure 1: Block diagram of the LRTRx.

II. System Architecture

This LRTRx communicates directly with the Texas Instruments CC1101, adopting the same RF frequency and data rate specifications. The RF frequency is the 433MHz ISM band which is broken up into eight physical 203kHz channels. The frequency deviation for the 2-FSK modulation is 50.781kHz and the data rate is 1001.2bps. A block diagram of the system architecture can be seen in Figure 1. Signals DC1-3 of the duty cycle block refer to the timing diagram in Figure 2.

An RF switch precedes the LRTRx and allows for independent tuning of the Tx and Rx matching networks. The receive portion of the LRTRx consists of a single-ended LNA with a passive mixer and transimpedance amplifier (TIA). The IF stage operates at 863kHz and contains a 6th order g_m-C bandpass filter which provides gain and channel selection. The received signal is then squared up with a comparator and driven into the digitally-assisted demodulator. The transmitter consists of a Class-E power amplifier operating from a 0.5V supply switched by a standard cell clock buffer. The reference for the entire LRTRx is a 26MHz crystal with on-chip oscillator. The LO for the transceiver is a charge pump-based type-2 PLL which provides the channel selection. Sleep headers or footers are included on all blocks, and are designed using thick-oxide FETs to reduce current leakage in the sleep state.

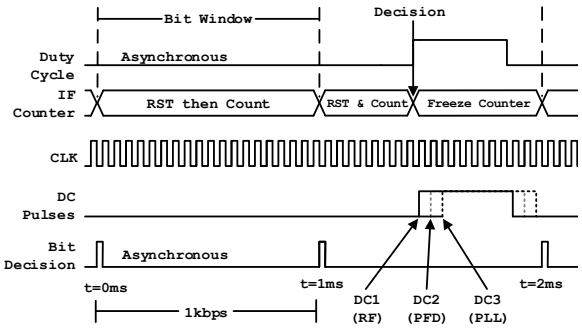

Figure 2: Timing diagram of receiver bit-level duty cycling.

III. Bit-Level Duty Cycling

In an environment with good SNR, bit-level duty cycling can be used to reduce power even further. If a bit decision can be made before the end of a bit window, then the receiver can turn off its high powered circuits for the remaining duration of the window. Figure 2 shows a timing diagram of a 3-stage shutdown sequence that takes place once the duty cycle pulse is asserted. The first bit window shows no duty cycling, with the bit decision being made at t=1ms based on a received count value. The second bit window demonstrates the duty-cycle sequence between t=1ms and t=2ms. Upon assertion of the duty cycle pulse, first the baseband demodulator makes its bit decision. On the three subsequent 50.781kHz rising clock edges the LNA shuts off, then the PFD UP/DN pulses are paused, and finally the VCO's buffer and the PLL divider are shut down. The ordering of the shutdown maintains the PLL's state on the loop filter since neither the charge pump nor VCO are disabled. The measured droop on the loop filter is 200mV/ms. This improves the startup time for the PLL between data bits.

Prior to the start of the next bit window, the circuits are all woken up in reverse order. Since the VCO will be close in frequency, but not in phase, there will be a necessary time to lock, but that time is shorter than the original startup time of the PLL. Duty cycling in the RFFE is implemented by controlling the sleep footers, shown in Figure 3. Figure 4 shows the duty cycling implementation in the PLL. In the bottom right corner, the divider and VCO buffer are both turned off using a thick oxide header. The PFD does not have a header, but asserting the duty cycle bit will force the UP/DN pulses into a static 'off' mode so they won't pulse the charge pump.

IV. Circuit Description

A. RF Front End

The RF front-end consists of a 433MHz antenna followed by an RF switch. The RF switch allows for the use of independent matching networks for both the power amplifier (PA) and the LNA. On-chip the LNA is an AC-coupled single-ended cascode amplifier with a tunable current source and an on-chip switchable cap bank for frequency tuning. A footer is used between the LNA and current source to control both duty cycling and sleep. The mixer consists of a single-balanced passive switching stage controlled by the differential PLL square wave output. A TIA follows the passive switching stage to improve linearity and provide gain.

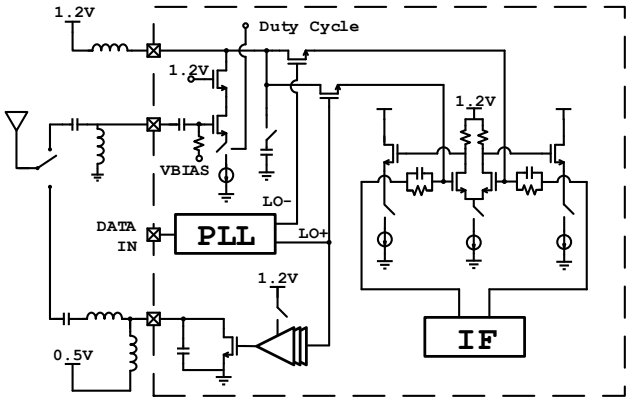

Figure 3: LRTRx RF front-end.

To achieve both low power and high efficiency the transmitter uses a Class-E power amplifier operating at 0.5V and is switched using a 4-stage clock buffer created with standard cells at 1.2V. The higher drive strength of the 1.2V buffer improves overall efficiency. 2-FSK modulation is implemented in the PLL by dynamically changing its division ratio. Figure 3 shows the design of the RF front-end.

B. Channel-Selection PLL

A PLL provides the LO for Rx and direct FSK modulation for Tx. Figure 4 shows the architecture of the PLL's main circuits. The 26 MHz XO chip reference frequency is divided before becoming the PLL's reference

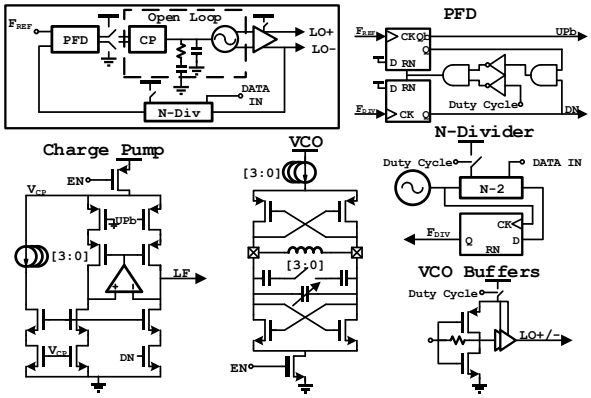

Figure 4: PLL block diagram and circuits showing duty cycling.

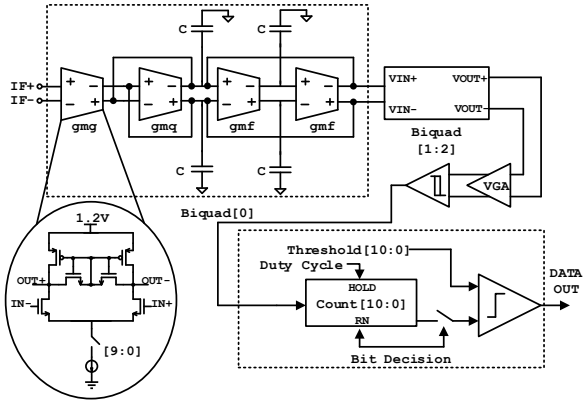

Figure 5: Baseband amplifiers and digitally-assisted demodulator

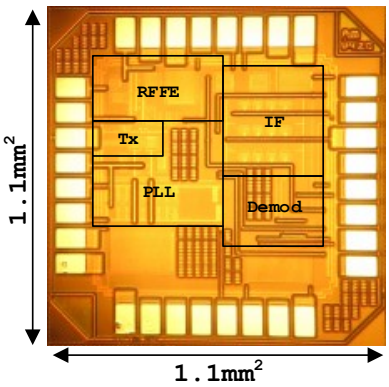

Figure 6: Die photo.

frequency in order to match the 2-FSK frequency deviation of the CC1101. Because the divide value between the reference frequency and the 433MHz output frequency is so large the PLL uses a synchronous divider retimed by the VCO at the output.

In addition, a 2-bit FSK value is controlled from an FPGA and dynamically modulates the division ratio in the PLL. The programmable divider also allows the LRTRx to frequency hop between the 8 non-overlapping physical channels.

C. Baseband Amplifiers

A 6th-Order bandpass g_m-C filter follows the mixer's TIA and provides channel filtering. It is created using 3 series biquad stages which each provide a 1st-Order high pass and low pass response. To provide a maximally flat Butterworth passband over the desired channel, each biquad is tuned to different center frequencies and quality factors. Additionally, the quality factor g_m-C cells in each biquad are biased in positive feedback preventing the need for high current sources which optimizes the low power architecture of our receiver. The gain of each of the biquads is also controllable providing a 40dB range of gain. This gain may also be used in combination with the quality factor to create different filter responses such as Chebyshev or Bessel.

The hysteretic comparator has tuneable hysteresis in 10mV steps to adjust for different noise levels. In areas with significant RF interference, the IF gain is bolstered to provide effectively higher hysteresis while in areas with low RF background noise, the IF gain is reduced to provide lower power consumption.

D. Digital Demodulation

As seen in Figure 1, the received IF signal is squared-up by a hysteretic comparator and driven into the digitally-assisted demodulator, shown in Figure 5. The incoming IF signal clocks a counter in between pulses that are used to indicate the time for the demodulator to make a decision on the incoming bit. These bit decision pulses are controlled by a synchronization algorithm implemented in an FPGA. Once the bit decision pulse is asserted the baseband demodulator compares the IF count with a user-programmed threshold. This technique enables the ability to adaptively control the data rate based on range or to perform bit-level duty cycling that was previously discussed. Increasing the data rate or duty cycling will result in a fewer counts separating the decision between a received 1 or 0 so will trade off performance for sensitivity.

V. Measurement Results

The LRTRx was designed in an IBM 130nm process and has an area of 1.1mm^2, including pads. The entire chip runs off a 1.2V supply with the exception of the Tx power amplifier which runs at 0.5V. A die photo can be seen in Figure 6.

The plot on Figure 7 shows the impact of bit-level duty cycling on both power and sensitivity at a data rate of 250bps. Increased duty cycling linearly reduces power, and therefore energy/bit, while sensitivity decreases exponentially, showing the trade-off between SNR and power.

The receiver's BER sensitivity curve and adjacent channel rejection are shown in Figure 8. The sensitivity was measured at -102.5dBm at a BER of 10^{-3}. Adjacent channel rejection is 14dB and drops to 34dB two channels away. The power amplifier was measured to have a 0.04dBm output power with a PAE of 47.5%. The theoretical communication range for the LRTRx is around 5km assuming a $1/d^2$ path loss.

Table I shows a power breakdown for the LRTRx. The crystal oscillator (XO) and PLL are shared between both the transmitter and receiver and consume 31µW and 226µW respectively. On the receive side, the LNA and mixer consume just under 100µW while the IF gain and filtering stages plus the digital demodulation block

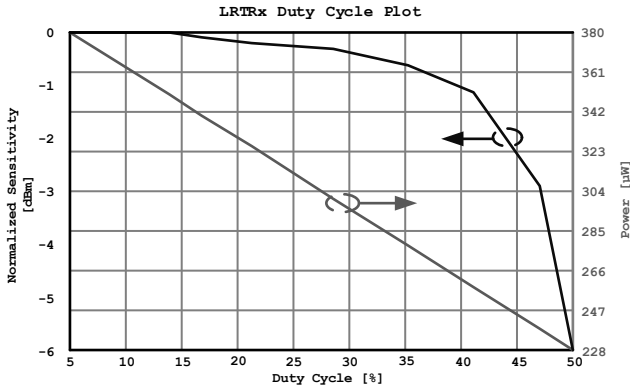

Figure 7: Bit-level duty cycling measurements at 250b/s.

consume 22µW. On the transmitter side, the power amplifier consumes 2.13mW in order to produce 1mW output power at the antenna. The standard cell clock buffer consumes 182µW. The entire receiver has a sleep power of 10.2nW and the transmitter has a sleep power of 98.9nW.

Table II compares the LRTRx with the CC1101 [2] and two published radios [1,4]. The CC1101 has more configuration and design overhead compared to the LRTRx so similar settings were chosen for comparison. Partially because of the overhead, the power in the LRTRx is much lower compared to the CC1101 for otherwise equivalent specifications. The 1kbps data rate reduces the LRTRx's energy/bit FOM compared to the published radios, but this work has the highest reported link budget and lowest power consumption.

VI. Conclusion

This paper presented a 2-FSK 1kbps 433MHz transceiver for low-power, long-range communication for sub-1GHz applications. Power reduction was achieved by using a 0.5V Class-E PA in the transmitter and a digitally-assisted demodulator along with bit-level duty cycling in the receiver, allowing the receiver to have a link budget of 102dB, similar to higher power available transceivers [2] with a 30X reduction in power.

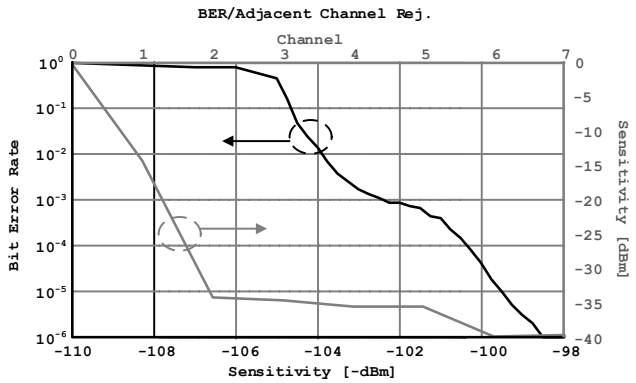

Figure 8: BER and adjacent channel rejection.

Table I: Power Breakdown

Power Consumption			
Rx		**Tx**	
LNA+Mixer	99µW	PA	2.13mW
IF+Demod	22µW	PA Buffer	182µW
PLL	226µW	PLL	226µW
XO	31µW	XO	31µW
TOTAL	**378µW**	**TOTAL**	**2.57mW**
SLEEP	10.2nW	SLEEP	98.9nW

Table II: Comparison with State of the Art

	[1]	**[2]**	**[4]**	**This work**
Freq. [MHz]	915	433	403	433
Modulation	FSK	2-FSK	FSK	2-FSK
DR [kbps]	50	1	128	1
Ch. BW [kHz]	200	203	--	203
PLL St [µs]	--	712	--	600
Tx Pwr [mW]	2.64	48	1.7	2.57
PA OP [dBm]	-7	0	-12	0.04
PAE [%]	--	--	--	47.5
Rx Pwr [µW]	2092	48000	2000	378
Rx Sens. [dBm]	-102	-112	-93	-102.5
Eb [nJ/bit]	41.84	48000	15.6	378
Adj. Ch. Rej [dB]	--	--	--	14
Tx Sleep [nW]	1000	600	--	98.9
Rx Sleep [nW]			--	10.2

Acknowledgment

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