A 98nW Wake-up Radio for Wireless Body Area Networks

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***Abstract* — A 0.13µm CMOS low power wake-up radio is presented. The wake-up radio operates with -41dBm sensitivity at 915MHz using OOK modulation with a data rate of 100kbps while consuming 98nW active power, 11pW sleep power, and has an energy efficiency of 0.98pJ/bit. The wake-up radio occupies 0.03mm^2 and uses two off-chip components (an inductor and a capacitor). All biasing and calibration for process variation and mismatch is included on-chip. The entire radio operates from a single 1.2V supply.**

***Index Terms* — Wakeup radio, low power radio, body area networks, wireless sensor networks.**

I. Introduction

Two important challenges leading to the ubiquitous use of wireless sensor nodes in body area networks (BAN) are small size and low power consumption. Radio power typically consumes the majority of the total power in a sensor node and therefore is a significant bottleneck in energy-efficient design. One technique used to reduce power consumption in a BAN is to use asynchronous communication that keeps the higher-power communication radio in a low-power sleep state. Wake up radios, with power consumption as low as 50µW [1-2], are a common technique used to achieve this. However, they are on at all times, and therefore contribute significantly to the total energy consumption of the node. Further power reduction is needed to improve sensor node lifetime to the point where it can be used without interruption in a BAN.

In this paper, a 98nW wake-up radio with an active area of 0.03mm^2 is presented to address both these challenges. The radio has a sensitivity of -41dBm and a data rate of 100kbps while requiring two off-chip passive components, both smaller than the size of the a typical 915MHz chip antenna, as well as a single external 1.2V power supply.

Section II discusses the power versus sensitivity tradeoff between recently published low power radios and energy harvesters while Section III will introduce the system architecture and circuit implementation of the wake up radio. Section IV will discuss measurement results and Section V concludes the paper.

II. Target Specifications

Figure 1 shows a power vs. sensitivity comparison survey of published ultra-low power radios (blue) and energy harvesters (red) from 2005-2012. The plot is divided into two sections: 1) low-power radios that consume power, and 2) energy-harvesters that generate power.

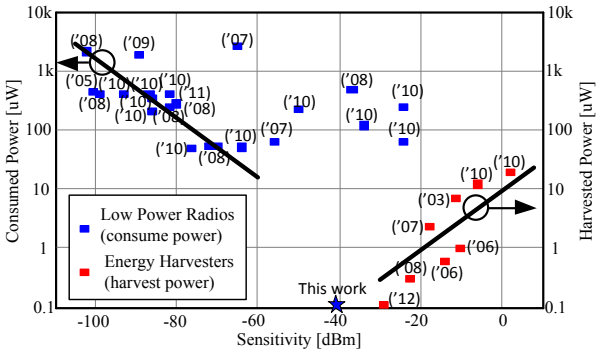

Figure 1. Survey of low power radios and energy harvesters from major publications (ISSCC, JSSC, VLSI, RFIC, TMTT, CICC)

Looking at the low power radio section, an empirical slope of -½ is apparent for radios with a sensitivity less than -60dBm. This slope is influenced by several parameters, such as the variation in data rate, architecture, and non-linearity present in the radios. The survey only covers ultra-low power receivers, common in BAN research; therefore, Bluetooth or Zigbee receivers with higher power will sit well above this line. A noticeable power floor around 50µW is present, caused by a minimum power requirement for achieving gain at RF.

In the energy-harvester section, an empirical slope of -½ is also apparent in the data for sensitivity higher than -30dBm. Below -30dBm, received voltages are not sufficient to fully commutate the rectifier stages, and power-harvesting efficiency drops sharply.

When plotted together in Figure 1, one can see a region below 50µW and between -60dBm to -30dBm where communication does not exist. Obviously to the left and above this region radios have been demonstrated and to the right the received power is high enough that rectification could be used to communicate with zero power. Our goal is to explore this region, near the intersection of the extrapolated trend lines by targeting a radio with a sensitivity of -40dBm and power consumption <1µW. In order to operate below the perceived 50µW power floor, no RF gain stages are used.

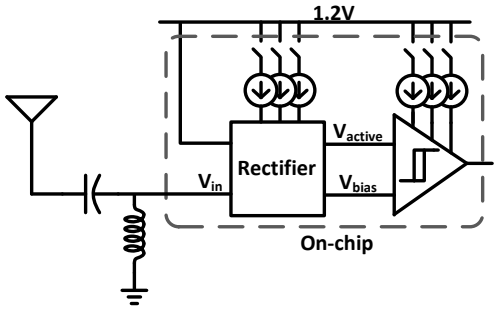

Figure 2. Wake up radio block diagram

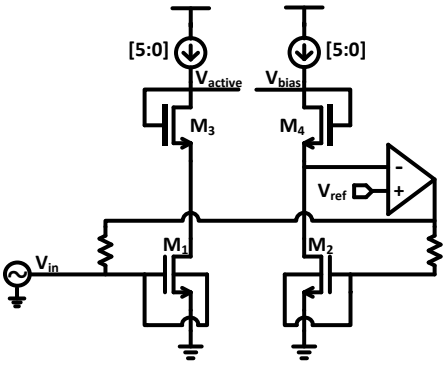

Figure 3. Rectifier Circuit

III. System and Circuit Design

The block diagram for the proposed low power wake up radio can be seen in Figure 2. It uses a single external power supply at 1.2V as well as an off-chip resonant tank at the RF input. Both process and mismatch are compensated through calibration, which is implemented using a scan chain controlled by an off-chip FPGA.

The signal is received at the antenna and power matched by the resonant tank before it reaches the input to the rectifier. The rectifier is made of an active circuit and a replica bias circuit. The active output (V_{active}) will decrease in the presence of an RF signal, while the replica bias output (V_{bias}) remains constant, acting as a bias point for the input to the comparator. The two signals feed into a hysteretic comparator. The digital output of the comparator is the output of the chip, which can be used by a BSN node's processor for synchronization.

A. Off-chip Resonant Tank

For a sensitivity of -40dBm, the input signal at the antenna will be around 2.2mV. An input signal to the rectifier is desired to be as large as possible to maximize the rectifier's conversion gain so a series capacitor and shunt inductor resonant tank is used at the input of the rectifier to boost the received voltage. Before implementing the resonant tank the circuit's measured input impedance is 0.7-j18.8, so a 1pF capacitor and 5.5nH inductor was used and increased the sensitivity of the wake-up radio by 12dB.

B. Self-biasing Rectifier

The rectifier in Figure 3, M_1, is a self-biased triple-well NMOS device in weak inversion, controlled by a binary-weighted 6-bit current DAC. The NMOS device is configured as a DTMOS (gate connected to body), which decreases its subthreshold slope, increasing its conversion gain [4]. The presence of a signal pulls the output low (V_{active}). Another NMOS device identical to the one mentioned is used as a replica bias, which provides a reference voltage for the comparator (V_{bias}). Diode-connected thick oxide devices (M_3 and M_4) are used to level shift the voltage at the drain of the rectifier to a voltage within the common-mode range of the comparator.

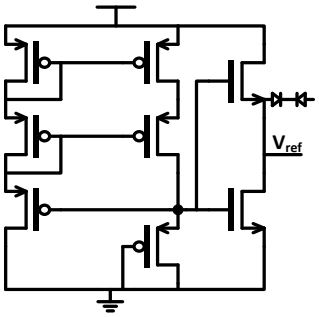

Figure 4. On-chip voltage reference

An active feedback amplifier with one input connected to a nominal voltage reference [5] equal to 2-3X the minimum overhead of the NMOS device is used to self-bias the replica which then provides a DC bias to the active rectifier. In the presence of an RF signal, the rectifier device quickly pulls down the drain voltage which then levels out as M_1 enters the linear region, allowing it to reset quickly when the signal disappears. The low power voltage reference, seen in Figure 4, was designed to have a reasonably stable voltage output at very low power levels.

The rectifier functions like an inverter. The pull-up portion of the inverter is the current DAC which is constantly pulling up on M_1. M_1 is the pull-down portion of the inverter and is biased by the feedback amplifier to hold the output between the two steady. When a signal is present, the exponential behavior of the weak inversion rectifier will cause the pull-down to become much stronger and pull the output low. Since the rectifier is

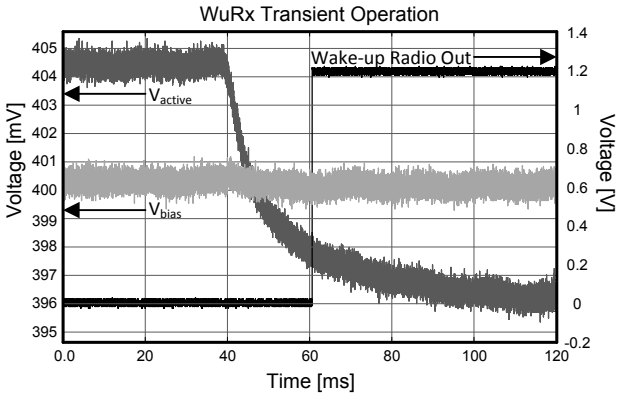

Figure 5: Active rectifier and replica bias waveforms with wake-up radio output

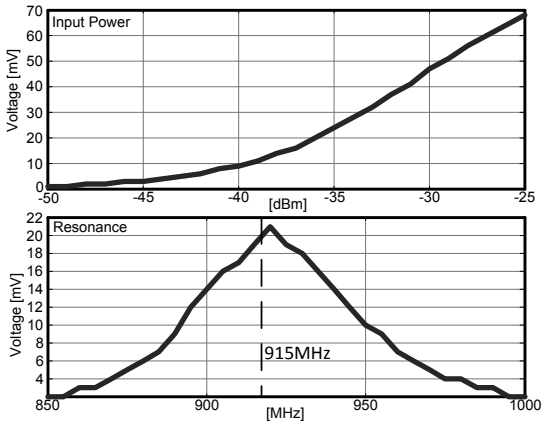

Figure 6: Output voltage at the comparator input as function of input power and frequency

biased so that the drain voltage is only 2-3X its minimum headroom, it very quickly levels out. At this point the output has fallen enough to toggle the comparator output. When the input signal is removed, the pull-up will restore the balance between it and the pull-down.

C. Hysteric Comparator

A hysteretic comparator with tunable asymmetry [6] is used to compare the output of the rectifier. It uses a 4-bit binary-weighted calibration scheme to determine the amount of hysteresis. Calibration is performed using parallel tail devices on each side of the comparator. Binary switching among the four devices on each side changes their effective width, and therefore the input offset. The common mode input voltage ranges from 300mV to 600mV and the hysteresis ranges from -31mV to +29mV. Power is controlled across process variation using a 7-bit binary-weighted current DAC, similar to the one used in the rectifier, and thick oxide devices are used to reduce power consumption and device leakage.

B. Mismatch

Mismatch is exaggerated in designs using devices in weak inversion so several steps have been taken to reduce the effects mismatch has on performance. Mismatch will be most prominent in the relative voltage levels at the output of the active rectifier and replica bias.

Nominal operation for our rectifier uses a single feedback amplifier, with its input connected to the bias device's drain voltage, to control gate biasing for both the active rectifier and replica bias. This will cause both devices to be biased to the same gate voltage and, without mismatch, would produce equal drain voltages. However, due to mismatch the drain voltages will differ and to compensate for this effect, the programmable hysteresis in the comparator can calibrate out the difference between the active and bias outputs.

If the offset between the output of the active and bias devices in the rectifier is significant enough, a second feedback amplifier is used so the active and replica bias devices can be independently biased. Each active feedback element will have the same on-chip voltage reference input to pull their drain voltages close. Since the voltage is shared between the active and bias rectifiers, exact PVT insensitive voltage levels are not required. The feedback amplifier has a slow enough response time to keep the bias level steady in the presence of the OOK input signal. The drawback to this approach is that it doubles the total power consumption from the feedback amplifiers and sensitivity is reduced.

D. Sleep Power Design

The wake up radio has been designed with a low-power sleep mode to support a duty-cycled wake-up strategy. This places extra emphasis on the importance of energy consumption in the sleep mode. To improve sleep mode energy, thick-oxide power gating devices were used throughout the design with above minimum lengths.

IV. Measurement Results

The low power wake up radio was fabricated in 0.13µm CMOS and operates under a single 1.2V power supply. The active area of the wake up radio is 156 x 190 μm^2 and can be seen in Figure 7. Without test circuits the wake up radio uses 5 IO pins.

A 915MHz signal with -41dBm sensitivity was connected directly to the receiver input and the signal output was monitored on an oscilloscope. The signal is OOK modulated at a data rate of 100kbps. Figure 5 shows the transient operation of the wake up radio running at 98nW total power. Communication using patch antennas

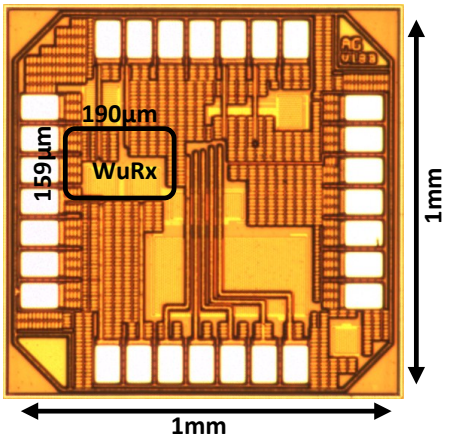

Figure 7. Die Photograph

was also verified at a distance of 4ft using a transmit power of 0dBm, which is roughly half the theoretical communication distance of 8.5ft based on the Friis equation.

Figure 6 shows the measured output voltage of the rectifier as a function of input amplitude and frequency. The top plot shows reduced output voltage amplitude at lower input sensitivity. With higher input, the conversion gain improves which allows for potential power savings. For example, at -30dBm, the power consumption of the wake-up radio can be reduced to 53nW. The bottom plot in Figure 6 shows output voltage vs. frequency due to the off-chip resonant tank. The data was taken with an input power of -36dBm and shows peak resonance at 920MHz, but sufficient performance a 915MHz.

Table 1 shows a power breakdown of the wake up radio under the same conditions as Figure 5. The entire radio consumed a total of 98nW with a measured sleep power of 11pW. The right side of the table shows the calibration setting resolution as well as the startup time from sleep for the on-chip voltage reference used in the feedback amplifier.

Table 2 shows a comparison with other low power

Table 1: Power Breakdown and Calibration Specs

	Power (nW)		Min	Max
Bias Circuits	20nW	Hysteresis Calibration	-31mV	+29mV
Rectifier	23nW	Hysteresis Resolution	2mV	
Replica Bias	23nW	Current DAC resolution	1.4nA	
Feedback Amplifiers	4nW	On-chip Voltage Ref startup time	110µs	
Comparator	28nW			
TOTAL	98nW	Sleep Power	11pW	

Table 2. Measured Receiver Performance and Summary

	This Work	[1]	[2]	[3]
Power	98nW	51uW	52uW	500uW
Frequency	915MHz	915MHz	2GHz	916.5MHz
Data-rate	100kbps	100kbps	100kbps	1Mbps
Energy/bit	0.98pJ/bit	510pJ/bit	520pJ/bit	500pJ/bit
Sensitivity	-41dBm	-75dBm	-72dBm	-37dBm
Die Area	0.03mm^2	0.36mm^2	0.1mm^2	1.82mm^2
VDD	1.2V	0.5V	0.5V	1.4V
Process	0.13µm CMOS	90nm CMOS	90nm CMOS	0.18µm CMOS

radios. It can be seen that reducing the sensitivity allows for much lower power radio design as well as more energy efficient communication. Sensitivity levels around -40dBm are acceptable for many applications in body area networks [7].

V. Conclusion

A low power wake up radio designed in 0.13µm CMOS was presented. By avoiding the need to generate transconductance at RF, we can reduce the power of the wake up radio beyond the surveyed 50µW power floor. Using this methodology a 98nW wake-up radio with a -41dBm sensitivity and 100kbps data rate was achieved.

Acknowledgement

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