A 10 mV-Input Boost Converter With Inductor Peak Current Control and Zero Detection for Thermoelectric and Solar Energy Harvesting With 220 mV Cold-Start and –14.5 dBm, 915 MHz RF Kick-Start

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Abstract—A boost converter for thermoelectric energy harvesting in 130 nm CMOS achieves energy harvesting from a 10 mV input, which allows wearable body sensors to continue operation with low thermal gradients. The design uses a peak inductor current control scheme and duty cycled, offset compensated comparators to maintain high efficiency across a broad range of input and output voltages. The measured efficiency ranges from 53% at V_1 = 20 mV to a peak efficiency of 83% at V_1 = 300 mV. A cold-start circuit starts the operation of the boost converter from 220 mV, and an RF kick-start circuits starts it from –14.5 dBm at 915 MHz RF power.

Index Terms—Boost converter, DC-DC converter, energy harvesting, low voltage, solar energy harvesting, thermal-electric, ultra-low power.

I. INTRODUCTION

ULTRA-LOW-POWER (ULP) wireless sensors for the emerging internet of things (IoT) often rely on harvested energy from ambient sources with small output voltages [1] and lower power. The power from a solar cell in indoor lighting can be only a few μW [2]. For wearable applications the thermal gradient between skin and air, especially under clothing, may only be a few °C, and the challenge of matching thermal impedances in the harvester packaging may leave thermoelectric generators (TEGs) with <1°C, which results in open circuit TEG outputs voltage of less than 30 mV. Recently several energy harvesting boost converters have been presented to harvest energy from lower voltage, lower power sources for ULP applications. A boost converter circuit that can harvest with allowable input voltage (V_i) down to 20 mV [3] achieves a maximum efficiency of 46% at 20 mV. It also needs an initial pre-charge voltage from an external source (for example, a battery) to kick-start the boost converter. Further, the design does not employ a maximum power point (MPP) tracking scheme to match the impedance of the energy harvester. A boost converter that can start up at 35 mV [4] with the help of a mechanical switch can harvest from 25 mV V_i. It achieves a peak end-to-end efficiency of 58%. A self-starting battery-charger IC [5] can startup from 330 mV and achieves an efficiency of 80% at 0.5 V V_i. To reduce the startup voltage of the boost converter, a transformer based startup mechanism is presented in [6]. It achieves a minimum startup voltage of 40 mV. However, use of the transformer increases the size of the system. Further, the re-use of the transformer as an inductor for boost conversion adversely affects the maximum achievable efficiency, which is 61% [6]. This paper focuses on the challenge of harvesting from lower V_i. Harvesting from low V_i faces several key challenges; low input power demands ultra-low power circuits for good efficiency. The inductor peak current (I_p) needs to be controlled properly for maximizing efficiency. The control circuits for the boost converter need to be controlled for mismatch which makes the small V_i hard to detect and use accurately. Mismatch can also cause significant variation in the peak inductor current (I_p), and accurate zero detection typically requires high current comparators. Further, the system needs a lower startup voltage.

This paper presents a boost converter capable of harvesting from V_i down to below 10 mV at efficiencies that are 7% higher than prior work [10]. A voltage-insensitive constant I_p control circuit, maximum power point (MPP) tracking, an integrated CMOS cold-start circuit from 220 mV, a parallel RF kick-start circuit that enables operation from a –14.5 dBm, 915 MHz RF signal, and the combination of offset compensation with duty cycled comparators enable these results and give efficiencies from 53% at a 20 mV V_i to 83% at 0.3 V V_i.
II. ARCHITECTURE OF THE BOOST CONVERTER

Fig. 1 shows the architecture and the timing diagram of the boost converter. It comprises a MPP tracking circuit, a cold-start circuit, a circuit to generate three phases of timing control, the conventional High Side (HS) and Low Side (LS) boost converter switches, and an RF kick-start circuit to startup from RF power. The boost converter can startup alternatively from the cold-start circuit which uses an oscillator and a voltage doubler circuit to cold-start from 220 mV. After startup, the boost converter operates in the normal mode where the boost converter makes use of a MPP tracking circuit to operate the converter at MPP. The boost control circuit generates three non-overlapping phases, φ₁, LS, and HS. In a conventional boost converter the switching cycle consists of LS and HS phases only. We add the extra phase, φ₂, for LS control and for offset compensation throughout the design. The φ₁ pulse width is set by a delay line. A peak inductor current control circuit is used to set the peak current, which maximizes the efficiency of the converter. The pulse width of the LS switch is set by the LS controller. A HS controller is used to control the HS switch to turn it off once the inductor current crosses zero during the high side charge transfer of the converter.

A. MPP Tracking and Control of the Boost Converter

The MPP of ambient harvesters such as solar cells and TEGs exists at fixed ratio (MPP coefficient, K) of the harvester’s open circuit voltage. The MPP of a solar cell exists at 73% to 80% of PV’s open circuit voltage [12], while for a TEG the MPP is at 50% of its open circuit voltage [11]. Since, the MPP varies with ambient conditions such as change in insolation levels or change in temperature, MPP tracking circuits are used to continuously track the MPP. In this work, we implement a constant voltage MPP tracking scheme [13] because of its suitability for low power applications. Fig. 2 shows the maximum power point tracking circuit for the energy harvester connecting to the boost converter. It consists of an MPP sampling circuit, a comparator C₁, and a clock generator. The MPP sampling circuit samples the ratio of open circuit voltage at \( V_1 \) and stores it on the cap. The clock generator generates a clock with a typical period of \( \sim 2.4 \) s, which is fast enough to track the slow changing ambient condition, and the leakage of the MPP capacitor \( C_M \).

Fig. 3(a) shows simulation of MPPT circuit with a fast MPP clock of 150 ms and a sampling pulse of 10 ms. When this pulse goes low, the boost converter is disabled, disabling the load at the output of the harvester which goes to its open circuit voltage. The MPP pulse is also used to close the switches \( S_1 \) and \( S_2 \), as shown in Fig. 2. The two resistors, \( R_1 \) and \( R_2 \) get connected to \( V_1 \), and the \( V_{MPP} \) node goes to the voltage \( R_1/(R_1 + R_2)*V_1 \), where \( R_1 \) and \( R_2 \) can be selected based on the MPP coefficient.

Fig. 3 shows the simulation result of the MPP tracking circuit. A comparator is used in a feedback loop to regulate \( V_1 \) and maintain it close to the MPP. This way the output voltage of the harvester is maintained at its MPP with a small ripple. The amount of ripple is a function of the capacitor \( C_1 \) connected at the output of the harvester. The ripple is made small by using a 5 \( \mu \)F capacitor at \( V_1 \). Further, the comparator regulates the input voltage \( V_1 \) and it needs to be continuous time and low power. We use a comparator with a quiescent current of 5 nA.

Fig. 3(b) shows the simulation of the MPP tracking scheme with a fast MPP clock with the open circuit voltage of the harvester varying from 300 mV to 200 mV in 100 ms.

III. LS TIMING CONTROL

Owing to the low output power of the ambient sources, it is more efficient to operate the boost converter in discontinuous conduction mode (DCM). Fig. 4 shows the circuit operation of LS and HS switching in a boost converter operating in DCM. In the LS switching, the inductor current rises from zero to a peak value (\( I_{\text{peak}} \)), which is discharged onto \( C_L \) in the HS phase. The efficiency of the boost converter is limited by the switching loss energy (\( E_{\text{SW}} \)) in the switches and control circuit, static
loss \((E_{ST})\) due to bias currents, and conduction loss \((E_{CN})\) in the resistance of the switches. The \(E_{ST}\) and \(E_{SW}\) are generally constants for a given architecture and fixed switch sizes, while the conduction loss depends on \(I_P\). The efficiency depends on \(I_P\) as the following analysis describes.

### A. Efficiency Dependence on Peak Inductor Current

The total energy loss in a boost converter can be given as

\[
E_L = E_{ST} + E_{SW} + E_{CN}. \tag{1}
\]

\(E_{CN}\) has two components, \(E_{CN,L}\) and \(E_{CN,H}\) for LS and HS conduction loss. For the LS switching, assuming that the switch resistance is small, we can write inductor current as

\[
\frac{dI}{dt} = V_I. \tag{2}
\]

For LS switching time \(T_{LS}\), the heat loss can be written as (assuming LS resistance is \(R_L\))

\[
E_{CN,L} = \int_0^{T_{LS}} i^2 R_L dt. \tag{3}
\]

Changing (3) to a current integral using (2),

\[
E_{CN,L} = \int_0^{T_{LS}} i^2 R_L \frac{L}{V_I} dt = \frac{LR_L I_P^3}{3V_I}. \tag{4}
\]

The total conduction loss is given by

\[
E_{CN} = E_{CN,L} + E_{CN,H} = \frac{L}{3} \left( \frac{R_H}{V_O - V_I} + \frac{R_L}{V_I} \right) I_P^3. \tag{6}
\]

Since \(V_I\) can be small for this design, \(R_L\) should also be small to minimize \(E_{CN}\). Further, for \(V_O \gg V_I\), \(E_{CN}\) can be given
Fig. 5. Efficiency variation of the peak inductor current ($I_P$) with $V_I$ shows that $I_P$ for maximum efficiency increases with $V_I$.

by (4). Since $0.5I_P^2P$ is the energy transferred in each cycle (assuming low losses), the efficiency losses ($\eta_L$) as a percent can be written as

$$\eta_L = \frac{E_L}{0.5I_P^2P} = \frac{E_{ST} + E_{SW}}{0.5I_P^2} + \frac{R_LI_P}{1.5V_I}.$$ (7)

$\eta_L$ represents the losses in the converter as a percent which needs to be minimized to maximize the efficiency ($\eta$) of the converter. $\eta_L$ has a minimum which can be obtained by differentiating (7) with respect to $I_P$ and the corresponding $I_P$ which maximizes efficiency is given by

$$I_{P_{max}} = \left[ \frac{6(E_{ST} + E_{SW})V_I}{LR_L} \right]^{\frac{1}{2}}.$$ (8)

Equation (8) also shows that $I_{P_{max}}$ decreases with $V_I$. The value of $I_P$ needs to be controlled as given by (8) with respect to $V_I$ to achieve the maximum efficiency in the converter. Fig. 5 shows the simulation result where the $I_P$ was varied for different $V_I$. The values for $E_{ST}$, $E_{SW}$, and $R_L$ are found from simulation to be 1.5 pJ, 99 pJ, and 0.269 $\Omega$ (with estimated layout parasitic including the inductor’s DCR). A 20 $\mu$H inductor is used for the simulation set-up. Fig. 5 shows that at higher values of $I_P$, $\eta$ decreases linearly, and at lower values of $I_P$, it rolls off quickly due to the quadratic dependence as shown in (7). Further, the maximum efficiency peak inductor current ($I_{P_{max}}$) was plotted as a function of $V_I$ and compared with the proposed equation (8). Fig. 6 shows that (8) predicts the optimized $I_{P_{max}}$ with less than 3% error.

B. LS Timing Control Circuit for $I_P$

In the preceding section, we showed that by controlling the peak inductor current, the efficiency of the boost converter can be maximized. In the conventional approach, the resistance of the switch (MOS transistor) is used to measure the $I_P$. The drop across the LS transistor $M_{LS}$, when the low-side is turned on, is the representation of $I_P$, and it is used to control $I_P$. However, this method is sensitive to mismatch and can result in 20%–40% error in the peak inductor current [15]. Another approach is to keep LS on for a fixed time [3], [4] to control the peak inductor current. This method is not expensive in terms of power. However, the efficiency can be reduced because the inductor current is not very well controlled with varying $V_I$ or $V_O$. Also, the process variation can result in a variation of the peak current, further impacting the efficiency of the converter. In this section we propose a low power control scheme to control the peak inductor current for the boost converter. We also propose digital control bits to control the process variation.

Fig. 7 shows the circuit that is used for generating peak inductor current for LS timing. Table I shows the configuration of the circuit in phase $\phi_1$ and $\phi_2$. The functioning of this circuit is explained with the help of the timing diagram shown in Fig. 8(a). During phase $\phi_1$, node $a$ is connected to $V_I$, the output.
of the energy harvester, $V_{C1,\text{LS}}$ is held to ground, and comparator C2 is disabled. The output of LS is set to ground. The transistor $M_{P1}$ is made weak, which sets the output voltage of node $b$ and is given by $V_{1} + V_{TM1}$, where $V_{TM1}$ is the threshold voltage of the transistor $M_{1}$. Weak $M_{P1}$ drives $M_{1}$ very close to its threshold voltage. In phase $\phi_2$, node $a$ is connected to ground, while the connections between $b$ and $c$ are removed. The transistor $M_{1}$ is designed to be in saturation and sets the current $I_{LS,\text{on}}$, which is given by

$$I_{LS,\text{on}} = k \times (V_{1} + V_{TM1} - V_{I, M1})$$

The current generated for LS control is made proportional to the square of the input voltage $V_{1}$. This current is mirrored to charge the capacitor $C_{LS}$. Once $\phi_2$ goes high, LS goes high, and the capacitor starts charging. Once the capacitor $C_{LS}$ crosses $V_{1}$, output of the comparator C1 goes low, which resets the D-flip-flop and brings LS to ground. Fig. 8(a) shows the timing diagram for the generation of LS. The timing of LS is given by

$$I_{LS,\text{off}} = \frac{C_{LS} \cdot dV}{dt}$$

as the capacitor charges from 0 to $V_{1}$ and using (9), we get

$$T_{ON,\text{LS}} = \frac{C_{LS}}{I_{LS,\text{off}}} = \frac{C_{LS}}{kV_{1}}.$$  

This is the time for which the inductor is kept on. It increases as $V_{1}$ decreases. Now, let us find out how the peak inductor current is obtained. Assuming negligible drop across $M_{LS}$, we can write the basic equation for inductor as

$$\frac{di}{dt} = V_{I}.$$ 

The inductor current changes from 0 to $I_{P}$ during the time LS is on.

$$\int_{0}^{T_{ON,\text{LS}}} \frac{di}{dt} = V_{I}T_{ON,\text{LS}} = \frac{C_{LS}}{kV_{1}}.$$  

Using (10), we get

$$I_{P} = \frac{C_{LS}}{kL}.$$  

Equation (11) gives the formula for peak inductor current. The expression shows that the $I_{P}$ is independent of $V_{1}$ and $V_{O}$ voltage. It depends on the value of the capacitance $C_{LS}$ and the inductor value $L$. By controlling the value of $C_{LS}$, peak inductor current can be set to a constant value, which targets the maximum efficiency, given by (8) and Fig. 5. The constant $k$ in the expression is a function of process and temperature. As a result, the peak inductor becomes a function of variation in process. The value of $I_{P}$ varies by 16% (21 mA to 25 mA) over a temperature range of 20°C to 60°C. Further, we also propose to address the variation using the capacitor $C_{LS}$. We use 6 bit binary control on the capacitor to address process variation. We perform the calibration of $I_{P}$ by observing $T_{ON,\text{LS}}$. The value of $T_{ON,\text{LS}}$ for a given $V_{1}$ is compared with a look-up table (LUT) for $T_{ON,\text{LS}}$ obtained for the $I_{P,\text{max}}$ of that $V_{1}$ given by (8). $C_{LS}$ is changed to set the $T_{ON,\text{LS}}$ given by the LUT to set $I_{P}$ for maximum efficiency. Fig. 8(b) shows the circuit diagram of the LS comparator C2 utilizing a two-stage error amplifier with offset compensation. In phase $\phi_2$, the offset of the comparator is compensated and stored on capacitor $C_{L2}$. The offset compensation technique is similar to the offset compensation in the HS comparator, which is discussed in the following section. In phase $\phi_2$, the comparison between $V_{1}$ and $V_{CLS}$ is performed. Fig. 9 shows the simulation result of $I_{P}$ in a 1000 point Monte-Carlo simulation with process and mismatch variation at 250 mV $V_{1}$. Simulation result shows a mean...
of 38.3 mA with a maximum of 70 mA and a minimum of 20 mA. Fig. 9 also shows that both the maximum and the minimum can be brought closer to the mean value of 38 mA by applying control bit of 0x31 for the minimum and 0x02 for the maximum \( I_P \) condition.

Equation (11) shows that \( I_P \) is independent of \( V_1 \). This is a first order derivation based on assumptions that the drop across LS switch \( M_{\text{LS}} \) is negligible compared to \( V_1 \). However, this assumption does not hold for lower values of \( V_1 \). Further, based on the derivation of (8), the value of \( I_P \) should decrease with \( V_1 \) for lower values of \( V_1 \). In our proposed circuit, \( I_P \) does decrease with \( V_1 \) due to the small voltage drop across \( M_{\text{LS}} \), which we ignored initially to derive (2). This dependence is not the dependence required by (8). However, it does help to increase efficiency at lower values of \( V_1 \). We measured the peak inductor current for different inductor values and their corresponding \( I_{\text{P max}} \) (by programming \( C_{\text{LS}} \)). Fig. 10 shows the measurement of \( I_P \) at different \( V_1 \) and \( V_0 \). Fig. 10(a) shows the measurement of \( I_P \) with \( V_1 \) while \( V_0 \) is held constant at 1 V, using a 22 \( \mu \)H inductor with a DCR of 70 \( \Omega \). The total LS resistance including board parasitic is close to 0.25 \( \Omega \). The inductor current will rise to 16 mA at 50 mV if the switch and inductor are ideal. Fig. 10(a) shows that inductor current rises to 14.5 mA at 50 mV. Fig. 10(a) also shows that \( I_P \) is within 15% of the value proposed by (8) at \( V_1 = 50 \) mV and <1% at \( V_1 = 150 \) mV or higher. Fig. 10(b) shows the measurement of \( I_P \) with \( V_0 \) and \( V_1 \) is constant at 100 mV. The value of \( I_P \) varies by \( \sim \)10% with the variation of \( V_0 \). Fig. 10(c) shows the measurement of \( I_P \) at different \( V_1 \) with \( L = 10 \mu \)H. The measurement shows less than 10% error at \( V_1 = 50 \) mV when compared to equation (8). The variation of \( I_P \) across process is addressed by digitally tuning \( C_{\text{LS}} \) as described in the preceding section. \( C_{\text{LS}} \) can also be tuned for lower \( V_1 \) operation as well to improve efficiency.

Further, the timing of LS is controlled by the comparator C2. The timing is given by capacitor \( C_{\text{LS}} \) charging from 0 to \( V_1 \).
using $I_{LS\text{ct}}$. When the comparator detects that $V_{\text{CLS}} > V_1$, it turns off the LS pulse. The offset in the comparator can introduce error in our required $I_F$ value and can impact the performance of the converter significantly, particularly at low $V_1$ values such as 10 mV. We compensate the offset of the comparator C2 in phase $\phi_2$ which helps enable charging at voltages measured down to 10 mV. Fig. 8(b) shows the schematic of the comparator C2. The details of the offset compensation technique are covered in Section IV. The delay of the comparator C2 can also affect the LS timing, so its performance needs to be high. We use a 3 $\mu$A comparator to achieve the required performance and it is turned on only during the switching cycle. This circuit consumes no static power since the comparator is on only during times of high power transfer and high $I_1$, making its power a component of the switching loss.

IV. HS TIMING CONTROL

Fig. 11 shows the circuit for generating the HS timing using the zero detection. Comparator C3 is used to compare the $V_X$ node with $V_O$. Once $V_X$ crosses $V_O$ and goes below it, the comparator output goes low and turns off the switch $M_{ES}$. Previous works on micro-power converters have considered comparator-based zero detection very high power [3], [4] and instead use a correction technique for zero crossing. In this work, we present the comparator based zero detection scheme as shown in Fig. 11. There are several challenges involved in designing zero detection comparator for a micro-power converters. First, the performance of the comparator needs to be very good. If the delay of the comparator is high, the exact timing of the HS control cannot be met. Second, the power consumption of the comparator needs to be small, as it will add to the loss in the boost converter. Finally, the mismatch between the devices in the comparator can result in high offset, which can alter the zero detection. This is particularly critical for harvesting from very low input voltage, as offset itself can be much higher than the input voltage $V_1$. Therefore, the offset due to mismatch needs to be cancelled. This work proposes a comparator that addresses these issues.

Fig. 12 shows the circuit diagram of the zero detection comparator. It uses a common gate amplifier, which is biased at $\sim 10 \mu$A of quiescent current. The use of a common gate amplifier provides very good performance. However, this comparator cannot be always on as the static power consumption will degrade the efficiency of the boost converter. The comparator is duty-cycled and is turned on only when the switching happens. Fig. 11 shows that every time LS goes low, the output of D-flip-flop goes high, which powers up the comparator. The comparator detects the zero crossing and signals high which is used to reset the flip-flop, which powers off the comparator after zero detection is performed. Comparator C3 is on only during the switching cycle, making its power consumption a component of the switching loss. The power overhead because of the zero-detect comparator is greatly reduced. It reduces efficiency by only 4% at $V_1 = 20$ mV and 0.4% at $V_1 = 0.3$ V, but its high on-current ($\sim 10 \mu$A) gives a fast response. While the performance and power issues are addressed as explained above, the circuit also addresses the offset issues. The offset in the
design is cancelled in phase $\phi_1$ of the switching cycle as follows. In $\phi_1$, nodes $d$ and $e$ are set at $V_O$ while $f$ is set at $V_{SS}$, and switch $T_1$ is turned on while $T_2$ is off. The feedback from node $g$ sets $V_{OFFSET}$ to remove offset in the comparator. If there is no offset in the design, $V_{OFFSET} = V_{REF}$. The measured comparator offset after compensation was $<1$ mV. Further, the feedback used for compensating the offset requires that the phase margin for the stable operation of the amplifier should be sufficient. This is addressed by properly choosing the size of $C_{OFFSET}$. The other comparators in the boost converter use a similar offset compensation circuit. After offset compensation, zero detection is performed in phase $\phi_2$.

Fig. 13 shows the 100 point mismatch (only the devices in the zero detection comparator is selected for mismatch) simulation result of the zero-detection comparator $C_3$. Fig. 13(a) shows that the offset in the comparator without the mismatch compensation technique shows a $3\sigma$ variation of $\pm 5$ mV. A 1 mV offset corresponds to a 1 mA difference in inductor turn-off current. Fig. 13(b) shows that the offset in the comparator can be brought down to less than 1 mV with the proposed offset compensation technique. Fig. 14 shows the 100 point mismatch (only zero detection comparator is selected for mismatch) simulation result of the efficiency variation of the boost converter at 10 mV $V_I$ and 1 V $V_O$. Fig. 14(a) shows that the efficiency of the boost converter without offset compensation in the zero detection. The minimum efficiency is 15% in this case. Fig. 14(b) shows that the minimum efficiency with offset-compensation is 27%. The offset compensation technique shows a $3\sigma$ improvement of 9% in the efficiency for the zero detection technique alone.

V. STARTUP CIRCUITS

In this work, we support two startup mechanisms. A cold-start circuit can startup the boost converter from $V_I > 220$ mV. It uses a ring oscillator (RO) that runs on $V_I$ to enable switching. Another startup mechanism is supported from RF. A 30-stage sub-threshold RF rectifier can charge from $14.5$ dBm RF input power at 915 MHz to kick-start the normal operation of the boost converter. We will now present the details of these circuits.

A. Cold-Start Circuit

Fig. 15 shows the cold-start circuit for the boost converter. It consists of a ring oscillator (RO) and a clock doubler circuit. When $V_O$ is below 550 mV, the POR signal is low, which enables the RO on $V_I$. The RO can oscillate for $V_I > 200$ mV and generate non-overlapping signals $p_1$ and $p_2$. Signals $p_1$ and
p$_2$ go to the clock doubler circuit, which generates LS_SU to control the startup switch $M_{SU}$. Phase $p_1$ and $p_2$ are used in the clock doubler circuit to generate signals that swing from 0 to 2V$_1$ (Fig. 15). The bottom plates of $C_1$ and $C_2$ are connected to the output of inverters driven by $p_1$ and $p_2$, and their top plates are driven by $L_{VT}$ nMOSs whose drains are connected to $V_T$ and gates to $p_1$ and $p_2$ respectively. The top plate of capacitors $C_1$ and $C_2$ will charge to $V_1$ in the absence of switching. The bottom plate of $C_1$ and $C_2$ swing from 0 to $V_1$ when switching, and the top plate swings ideally from $V_1$ to 2 $V_1$ as shown in Fig. 15. Next, we convert to signals with full 0 to 2 $V_1$ swing. When $p_1$ is high, $X_2$ is also high, so LS_SU is pulled down to ground. When $p_1$ is at 0, $X_2$ is at $V_1$ and $X_1$ is at 2 $V_1$. The pMOS transistor will turn on and pass the level to LS_SU, which ideally swings from 0 to 2 $V_1$ (in reality, the output voltage is below but close to 2 $V_1$ because of the switching losses involved). The increased swing is used for inductor switching to charge $V_O$. In this configuration the inductor current is not controlled and is restricted by the switch resistance. The HS control is disabled, and the circuit uses $M_{HS}$ in diode configuration to pass high. This switching path is not efficient, but it charges $V_O$ without adding load to it. Once $V_O$ reaches voltage greater than 550 mV, the POR signal goes high enabling the normal operation of the boost converter. The POR signal goes high and disables RO and pulls down the gate of MSU to ground, disabling the cold-start switching.

B. RF Kick-Start Circuit

RF kick-start circuit with RF switch.

The RF kick-start circuit provides a kick-start from RF energy and consists of a broadband RF rectifier and an RF switch, as shown in Fig. 16. The input sensitivity of the rectifier is $-32$ dBm with no load [18] and an RF matching network. In this boost converter design the off-chip RF matching network was not used to enable startup from different RF frequencies. Further, during startup, the $V_O$ voltage sees a load of 200 nA to power the bias and control circuits for the boost converter. The measured sensitivity of the rectifier at 915 MHz RF signal is $-14.5$ dBm with a 200 nA load at $V_O$. The rectifier's structure is the same as the Dickson multiplier, with the exception that all transistors operate in...
the sub-threshold regime. The rectifier needs to operate in the subthreshold region to harvest RF power from very low inputs and the output voltage. This subthreshold rectifier uses zero-threshold transistors and 30 stages to achieve sufficient RF gain.

An RF switch is required because the RF rectifier is used both for the RF kick-start and as an RF front-end of a low power radio. The RF switch is turned on during kick-start mode when output voltage $V_O$ is lower than POR threshold voltage and normal boost operation is disabled. Fig. 16 shows the circuit diagram of RF switch. During kick-start mode POR is low and $V_O$ is connected with Rect_Out. $V_O$ starts rising with the incoming RF signal. Once the voltage crosses 550 mV, POR goes high and the RF switch is turned off. The rectifier can be used for the RF front end now. The RF switch provides a ground shielding to prevent the noise from the boost converter to propagate into the rectifier output.

VI. MEASUREMENT RESULTS

The chip was fabricated in 130 nm bulk CMOS. Fig. 17 shows the implementation of the boost converter where it consumes 0.15 mm$^2$. A low power lower voltage bandgap reference circuit which can provide reference voltage from 0.5 V [17] $V_O$ is used for generating the reference voltage for the boost converter. The area of the bandgap reference circuit is 0.03 mm$^2$. The LS resistance, which is critical for efficiency at low voltages has a designed value of 0.3 Ω including layout and component parasitic. The value of the inductor used in our measurement set-up is 10 μH, the output capacitor at $V_{CAP}$ is greater than 100 μF, and the capacitor at the input of $V_1$ is 5 μF. The output of the boost converter will be used as a storage node for storing energy in a typical IoT application. A clamp circuit is used to clamp the output voltage of the converter. Fig. 18(a) and (b) shows the measurement of $V_X$ at the inductor current zero crossing. Node $V_X$ does not have overshoots or undershoots at the zero crossing which indicates near-ideal zero detection using our offset compensated ZD comparator. Fig. 18(c) shows measurement of boost converter operation at $V_1 = 10$ mV with a 5 μA load at the output. Fig. 19(a) shows the measurement of boost converter operation from cold start. In this measurement, $V_1$ was set at 250 mV for cold start. After cold start, $V_1$ is slowly decreased to 20 mV. The measurement shows operation at 20 mV. Fig. 19(b) shows the measurement of MPP operation at $V_1 = 50$ mV in the open circuit configuration with a 10 Ω source resistance. $V_1$ quickly reaches 25 mV, operating the converter at the source’s MPP. The minimum cold-start voltage was measured at 220 mV with an instantaneous power consumption of 308 μW during cold-start. The minimum measured operating $V_1$ is <10 mV. The tracking efficiency at 20 mV open circuit voltage and 5 Ω of series resistance is 92%, and it increases to 99% at 100 mV of open circuit voltage. The boost
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Fig. 19. (a) Boost converter operation from cold start to 250 mV to operation at 20 mV $V_I$. (b) MPP tracking of the boost converter circuit at an MPP of 25 mV using a source with an open circuit voltage of 50 mV and a source resistance 10 $\Omega$.

Fig. 20. Measurement of RF kick-start of the boost converter. (a) RF kick-start with a 915 MHz RF signal and an input power level at $-14.5$ dBm. (b) RF kick-start with a 2.45 GHz RF signal and an input power level at $-8.5$ dBm.

The converter circuit can supply a peak power of 22 mW at the output for a $V_I$ of 0.3 V. Fig. 20 shows the measurement of the RF kick-start circuit. In this set-up, $V_O$ was completely discharged, and $V_I$ was connected to 50 mV, and an output load of 5 $\text{M}\Omega$ is connected at $V_O$. Since $V_I$ is too low for cold-start, $V_O$ will not charge from $V_I$. Fig. 20(a) shows the measurement of RF kick-start when an RF signal of 915 MHz is applied at the RF$_{IN}$ (Fig. 16). $V_O$ goes to 550 mV with an input RF power of $-14.5$ dBm. Fig. 20(b) shows the result with a 2.45 GHz RF signal. At 2.45 GHz, an input RF power of $-8.5$ dBm or more is needed for kick-start operation. In our set-up, a matching network for the RF signal is not used, and so the sensitivity of RF signal for kick-start is lower. The kick-start circuit will startup at even lower input RF power if a matching network for the RF signal is used. Fig. 21 shows that efficiency of the boost converter ranges from 21% at $V_I = 10$ mV to 83% at $V_I = 0.3$ V and $V_O = 1.1$ V. We also measured the boost converter performance with a TEG (Laird 430857-500). The resistance of the part is 2 $\Omega$. We measured the boost converter in an application set-up where the TEG was put on a human hand with one side exposed to ambient, and it produced an open circuit voltage of...
40 mV. The functionality and performance of the boost converter was also tested with a photovoltaic cell with an open-circuit voltage of 540 mV. Table II compares this work with previously reported micro-power boost converters for low input voltages. Our work reports harvesting from the lowest input voltage at 10 mV, with an efficiency of 21%. Our static power consumption is 300 nW, and the circuits are designed in 130 nm. We support two startup methods. The cold-start does not require external assistance and starts operation from 220 mV, which is 110 mV lower than in [5]. Further, we also support startup using 915 MHz and 2.4 GHz RF signals.

### VII. CONCLUSION

A thermoelectric boost converter combines an LP control scheme with offset compensation and duty cycled comparators to enable energy harvesting from TEG/solar cell inputs as low as 10 mV, 50% lower than prior work. Controlling the LP allows the converter to sustain high efficiency across a broad V1 range, achieving 53% and 83% efficiency at 20 mV and 300 mV, respectively, which improves on prior designs. A cold-start circuit enables operation from 220 mV, 110 mV lower than previous work [5]. Further, the design supports constant voltage MPP tracking and startup from 915 MHz and 2.45 GHz RF signals. These features allow the converter to extend the operating window for thermal harvesting with low thermal gradients, which is ideal for body worn sensors.

### REFERENCES


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