Energy Efficient Pulsed-UWB CMOS Circuits and Systems

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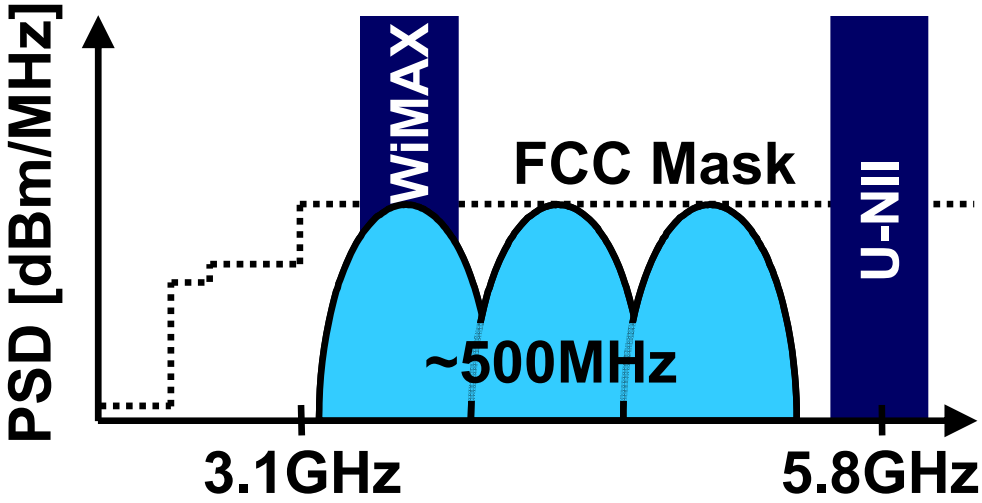
ICUWB 2007, Singapore

Outline

- Parallel baseband architecture enabling sub-Vth digital circuits
- Mostly digital transceiver chipset
  - Transmitter and receiver design
  - System demonstration
  - Results

System Challenges

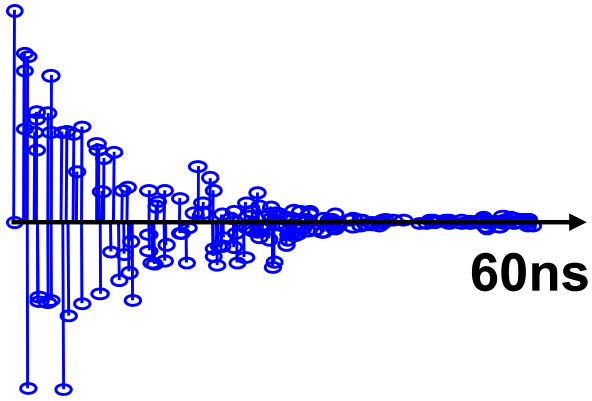
- Presence of strong in-band interferers



Sub-bands widely used

- Multipath and inter-symbol interference (ISI)

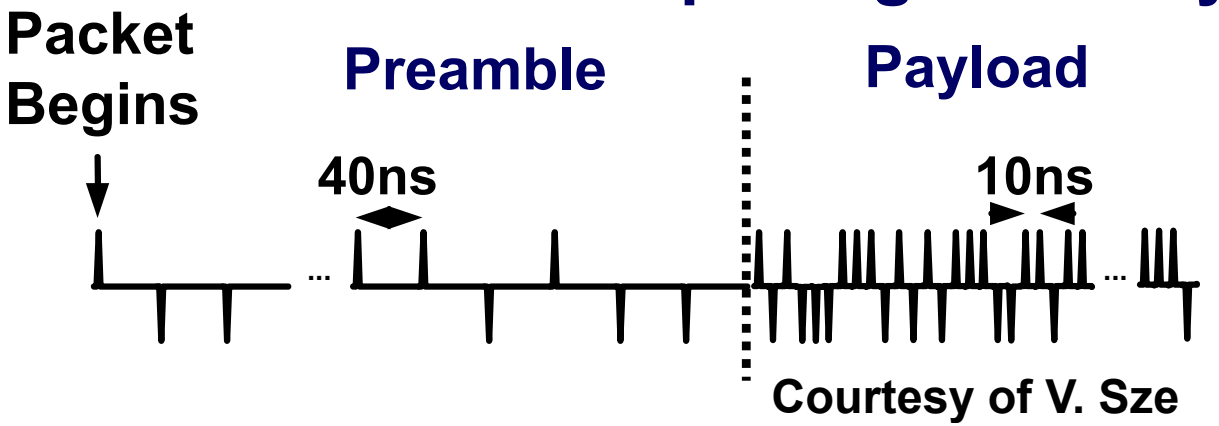
NLOS Channel Impulse Response



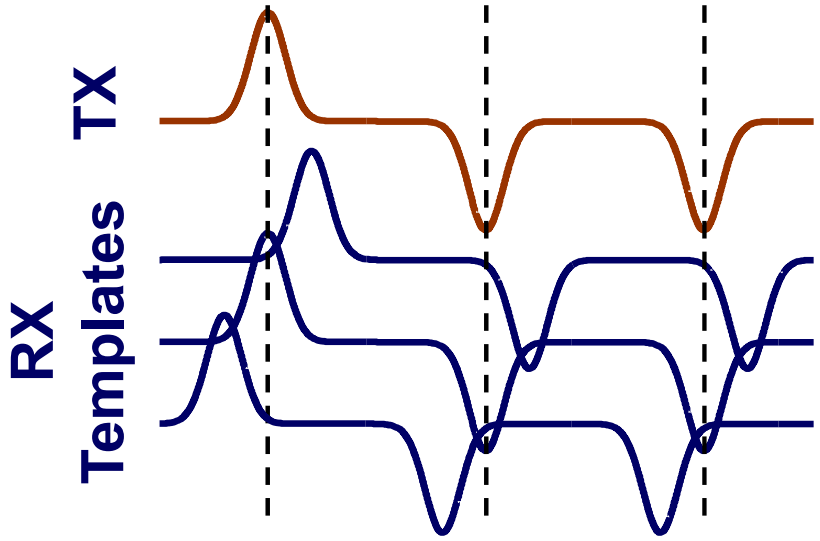
RMS Delays: 5 to 25ns

High Data Rate Synchronization

Example High Rate System



250MHz baseband pulse
Sample at 500MS/s (2ns)
40ns PRF in preample
► 20 samples / PRF



20 possible inter-pulse delays

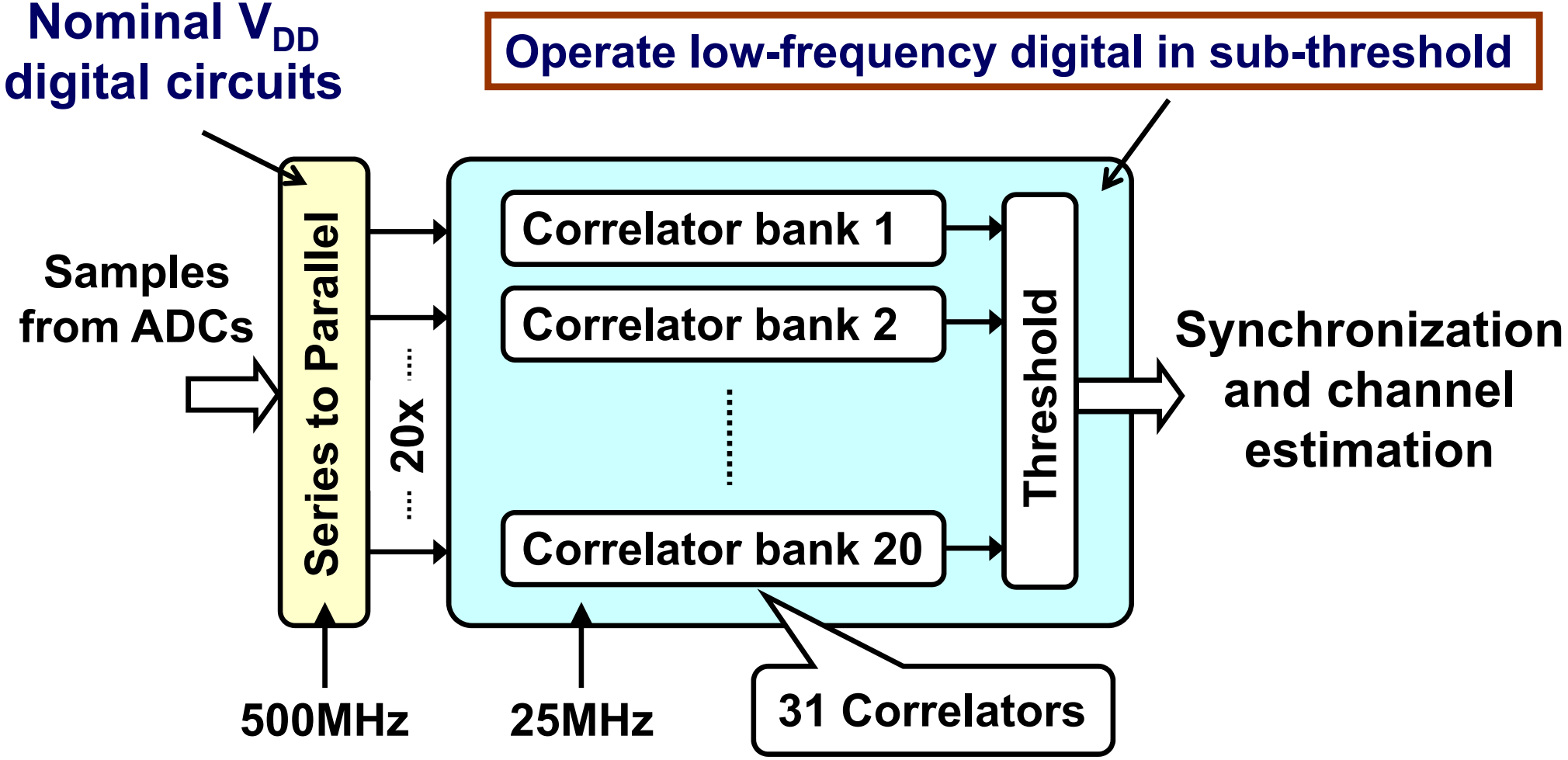
×

31 bit CDMA code

620 RX templates

Digital parallelism exploited for synchronization

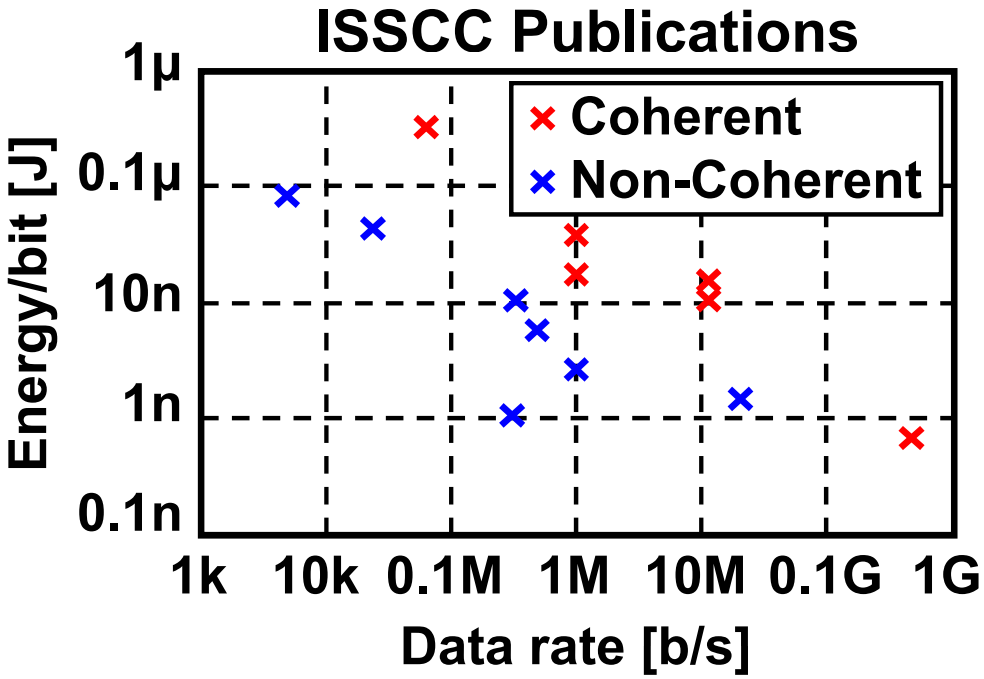
Massively Parallel Processing



Acquisition 7mW / Demodulation 1.7mW
20pJ/bit for a 4kb packet

[V. Sze, ISLPED 2007]

Low Data Rate Chipset

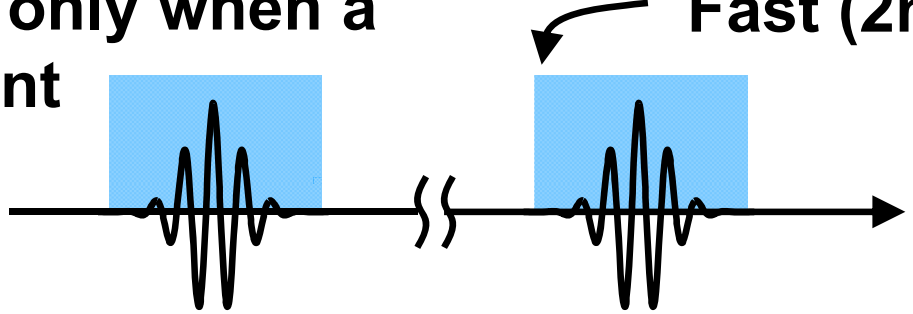


Receiver Trends:
- **Data rate▼, energy/bit▲**
- **Non-coherent 10x lower energy**

- **Pulsed-UWB signaling inherently duty-cycled**

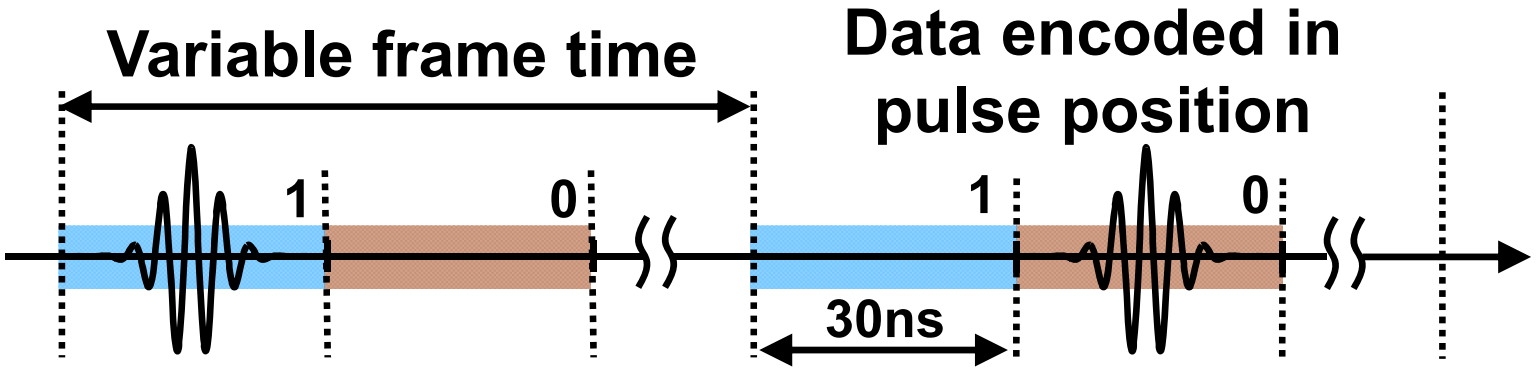
TX and RX on only when a pulse is present

Fast (2ns) turn-on time

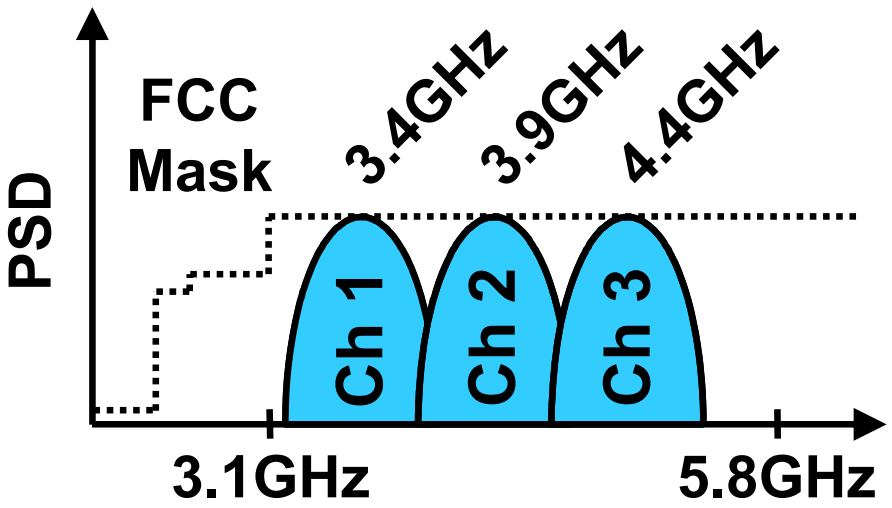


Scalable Signaling

- PPM signaling with non-coherent receiver



- Three channel frequency plan

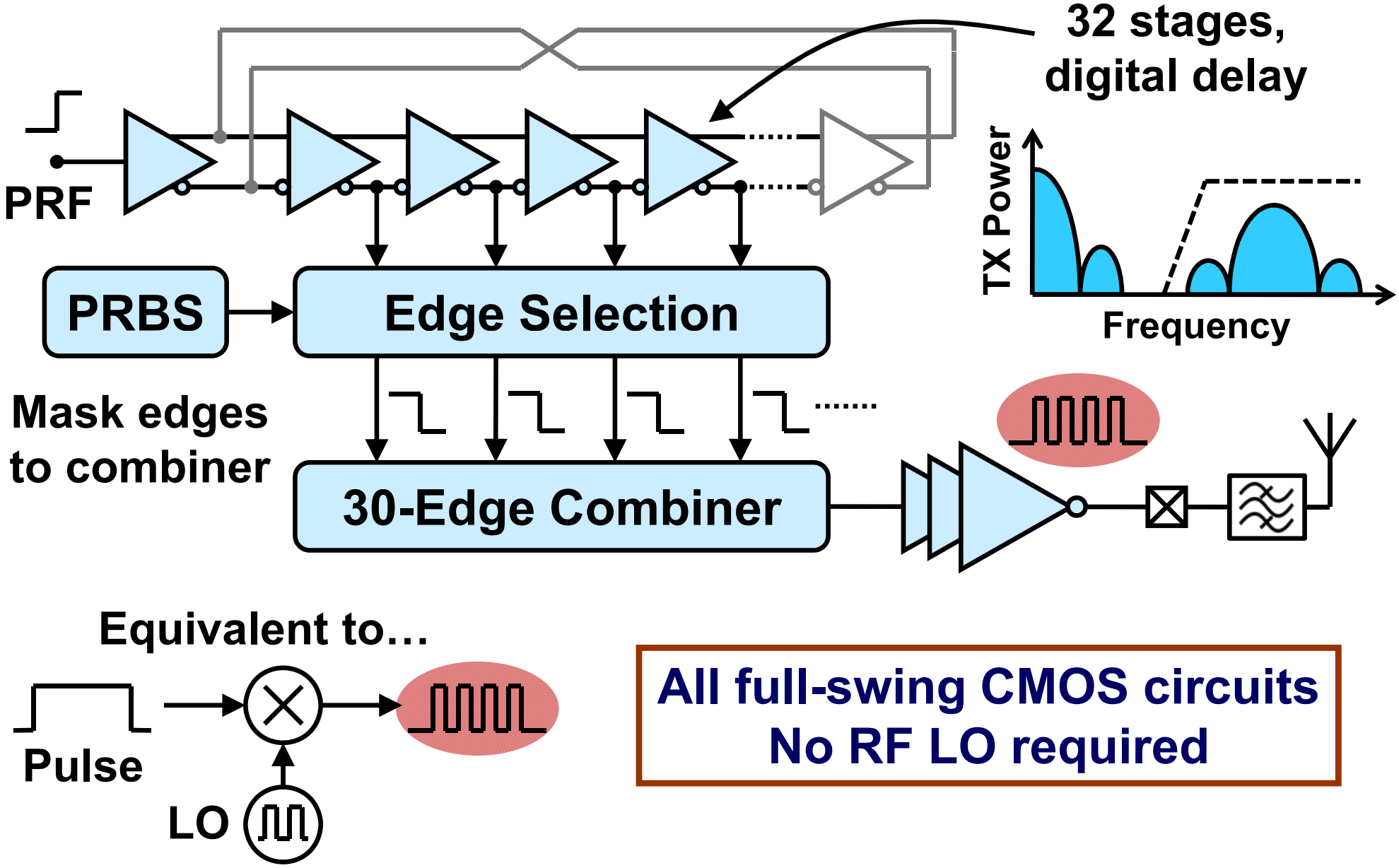


Center frequency: 6000ppm

Energy-detection receiver

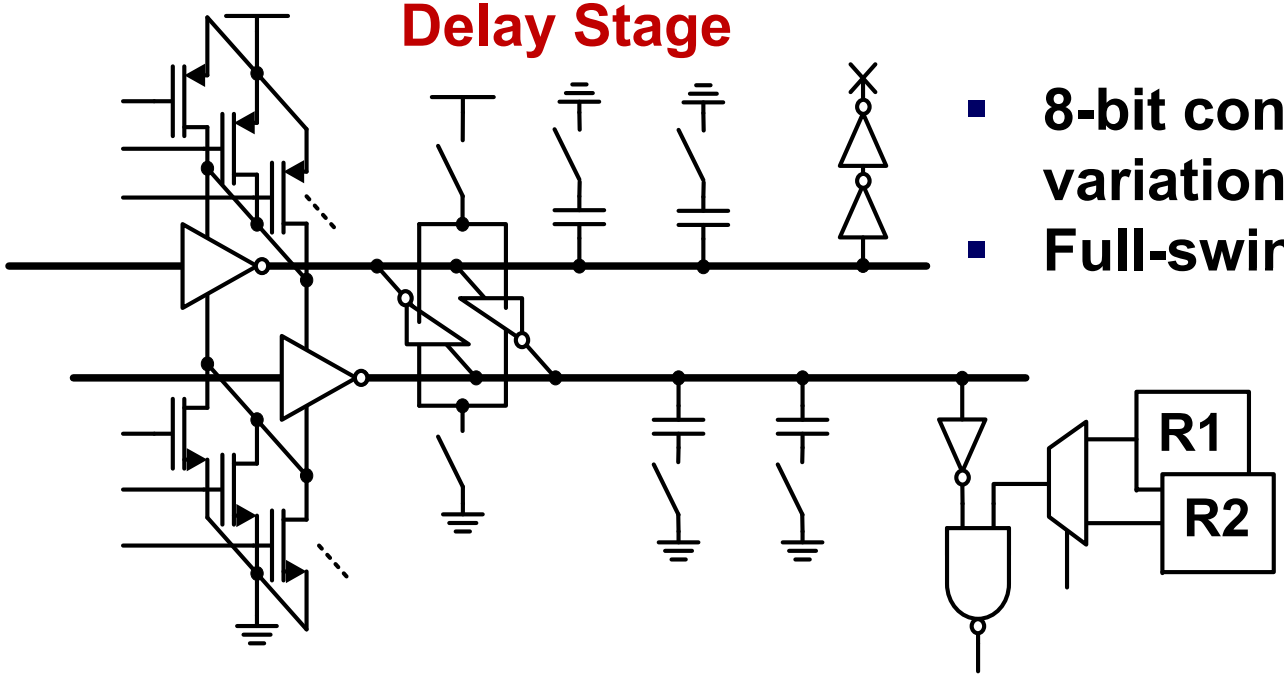
All-Digital Transmitter

Transmitter Block Diagram

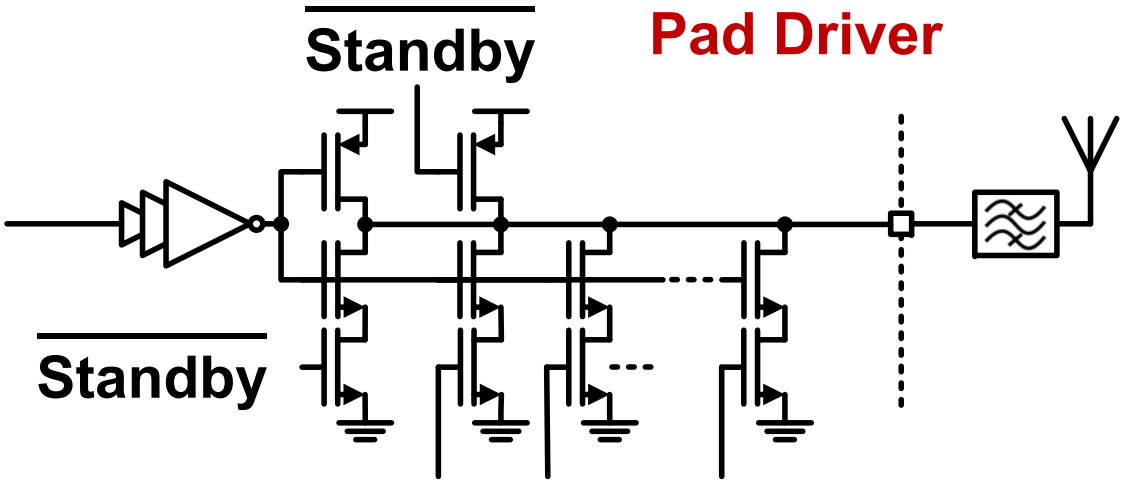


All full-swing CMOS circuits
No RF LO required

Delay Stage and Pad Driver



- 8-bit control for ±30% delay variation due to process
- Full-swing digital signals
- Edge selection logic

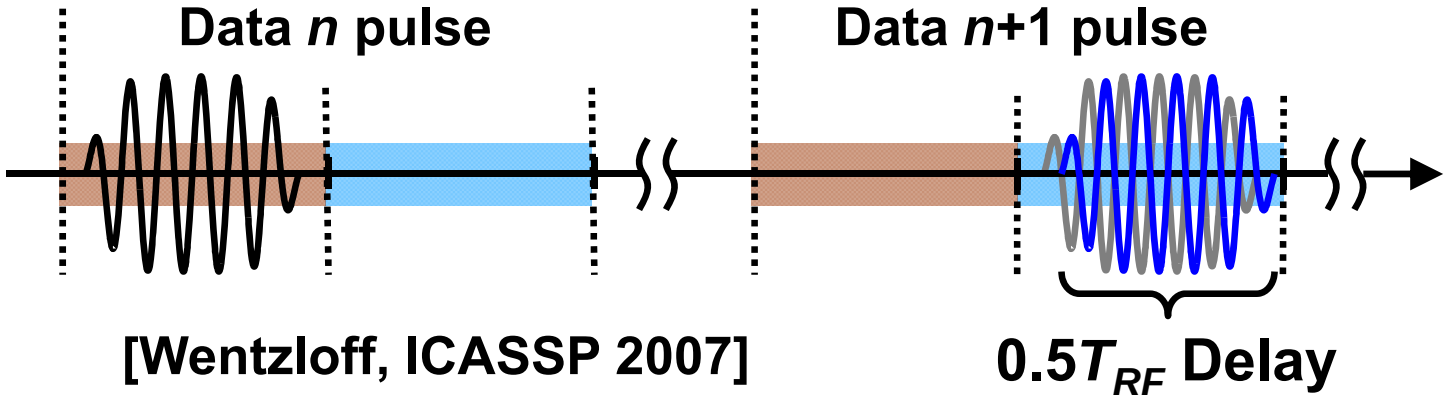


- Linear-in-dB gain setting
- Stacked NMOS for leakage control

27% efficiency

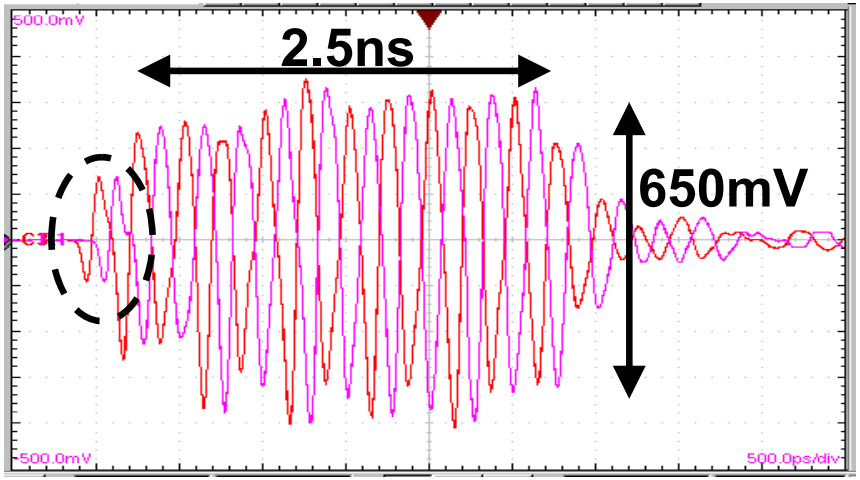
Delay-Based BPSK Scrambling

- **Architecture enables new signaling scheme**

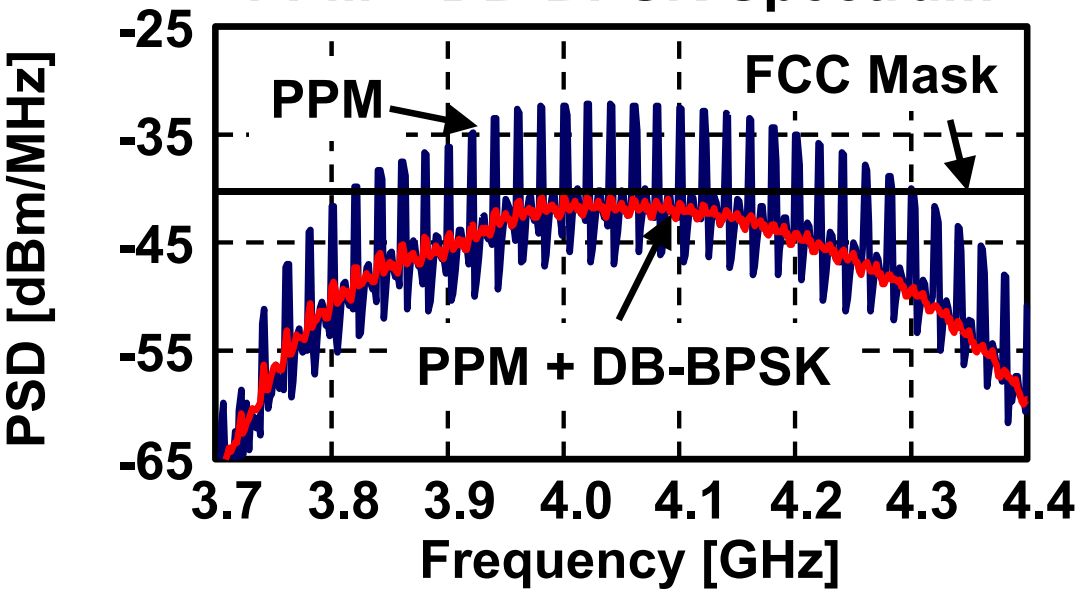


Emulates BPSK with minimal overhead

DB-BPSK Pulses

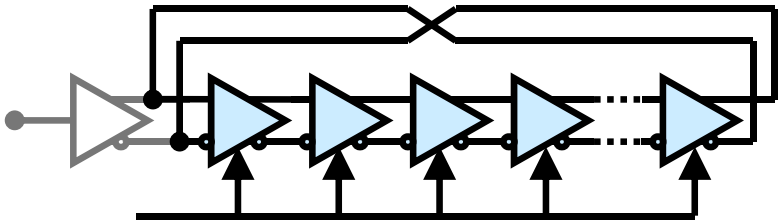


PPM + DB-BPSK Spectrum

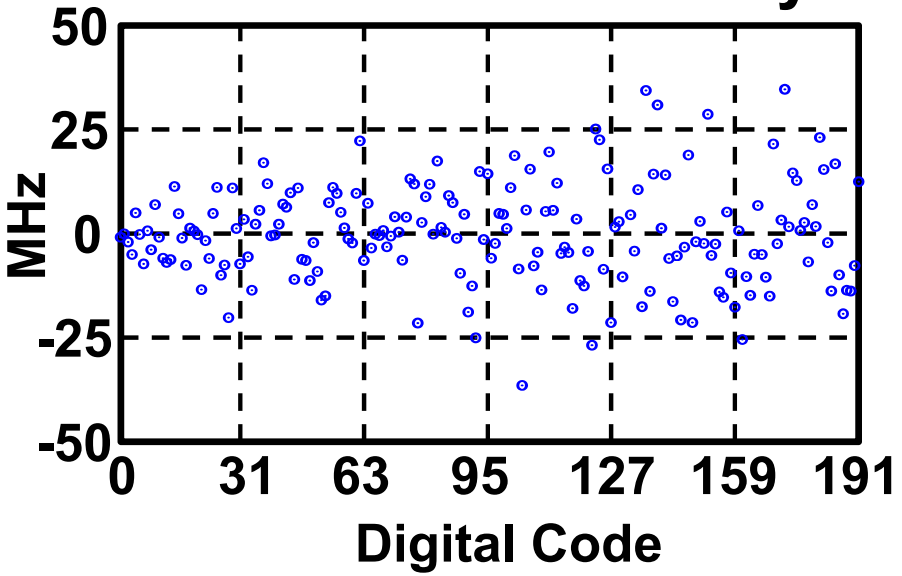


RF Calibration

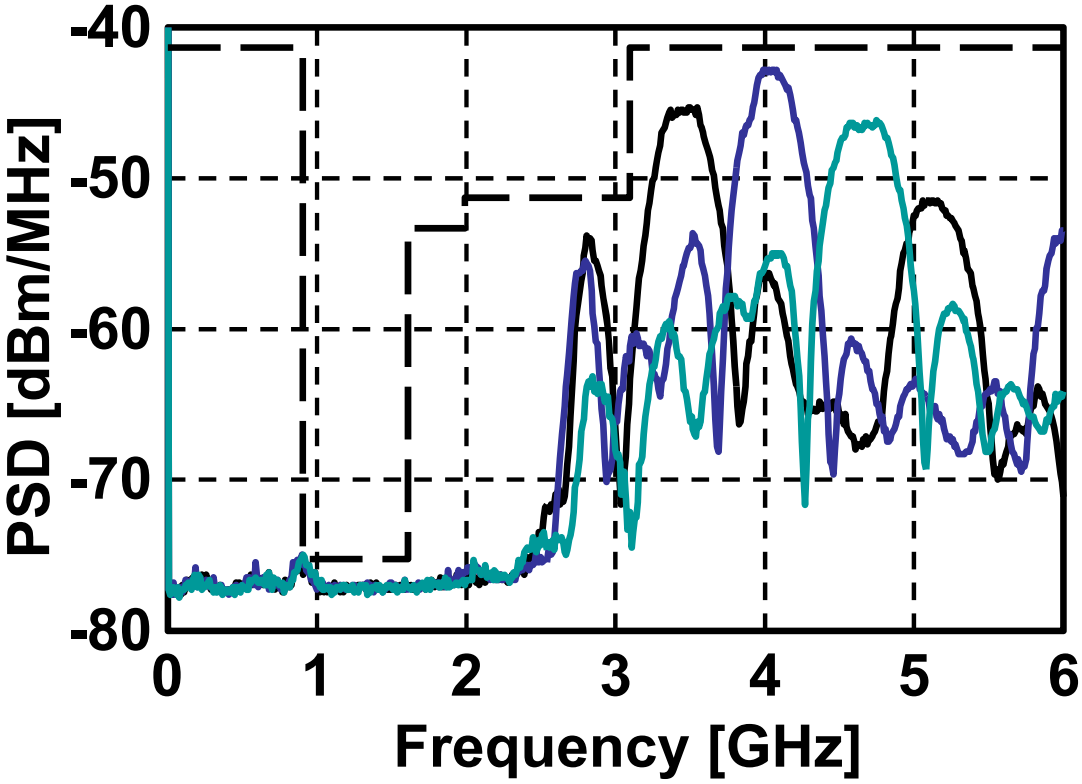
Calibrate delay in ring



Calibration Accuracy



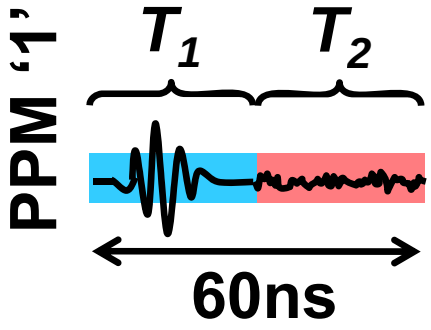
3-Channel Spectrum



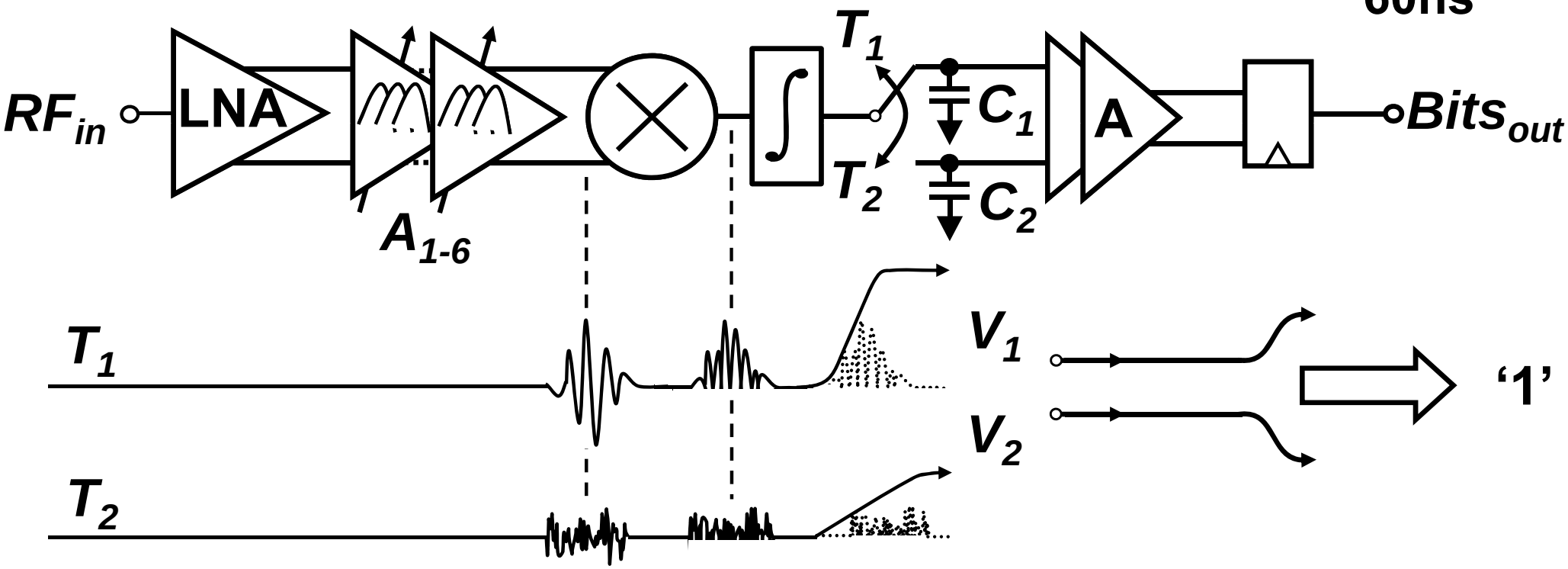
Digital calibration algorithm sets RF center frequency

Energy-Detection Receiver

- RF front-end performs channel-selection
- Energy detection by square-and-integrate

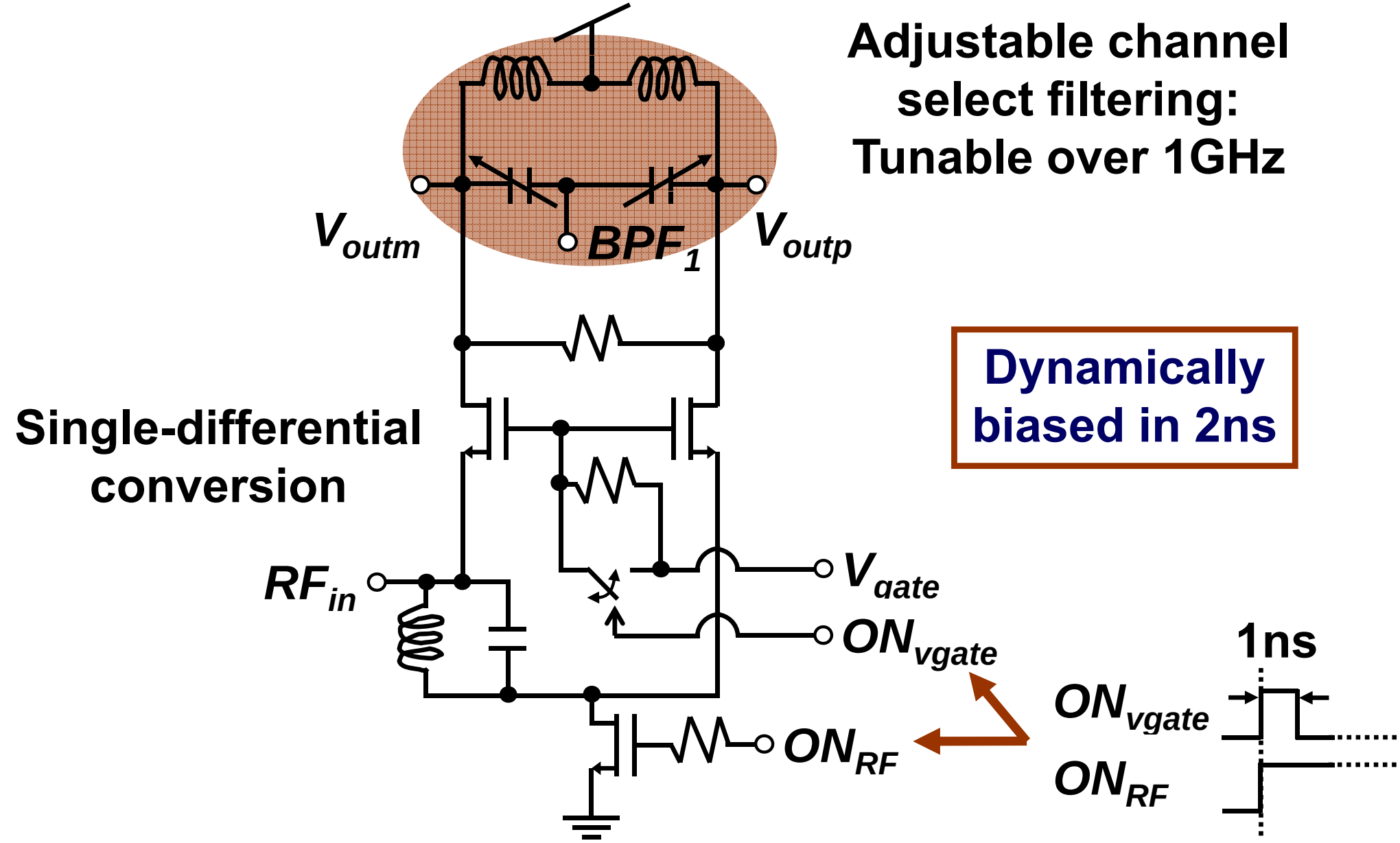


Low-voltage circuits, digital techniques

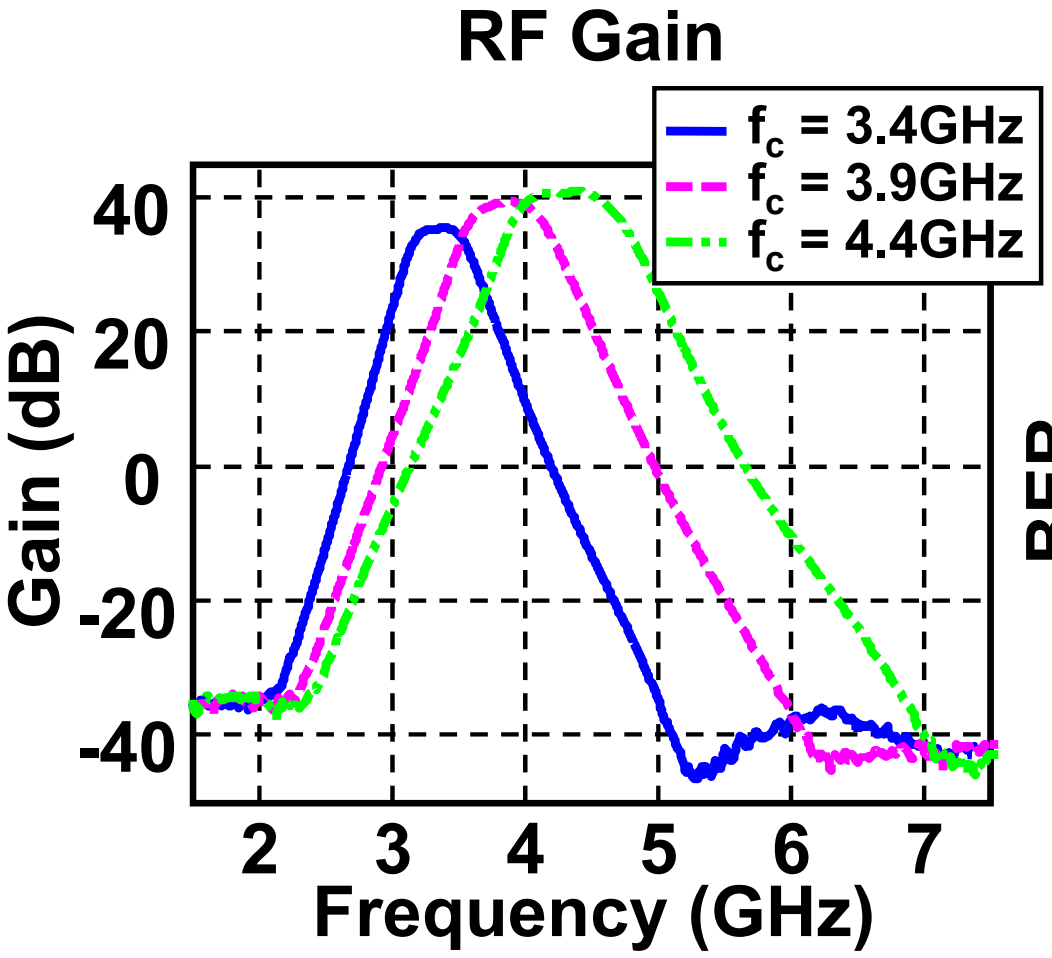


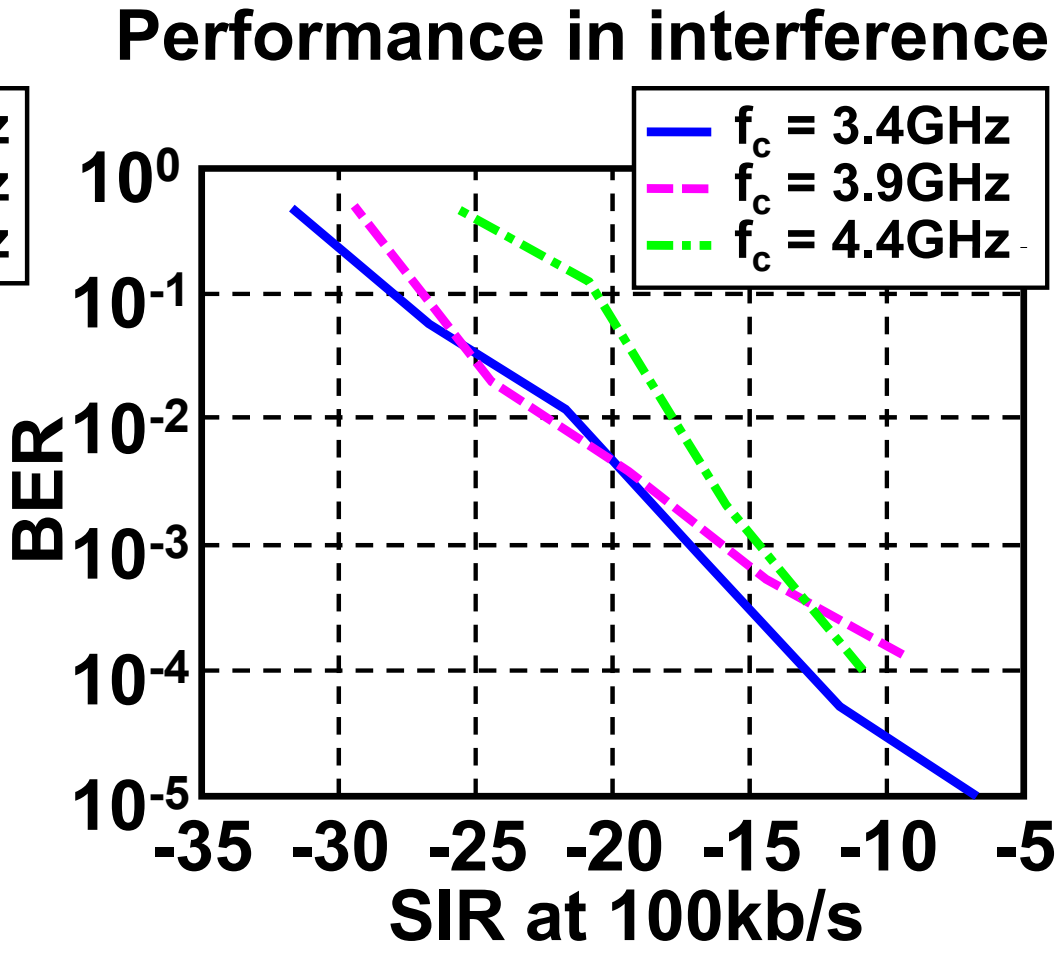
No RF oscillator required

0.5V-0.65V LNA


Adjustable channel select filtering: Tunable over 1GHz
V_{outm}
BPF_1
V_{outp}
Dynamically biased in 2ns
Single-differential conversion
RF_{in}
V_{gate}
ON_{vgate}
ON_{RF}
1ns
ON_{vgate}
ON_{RF}

Measurement Results



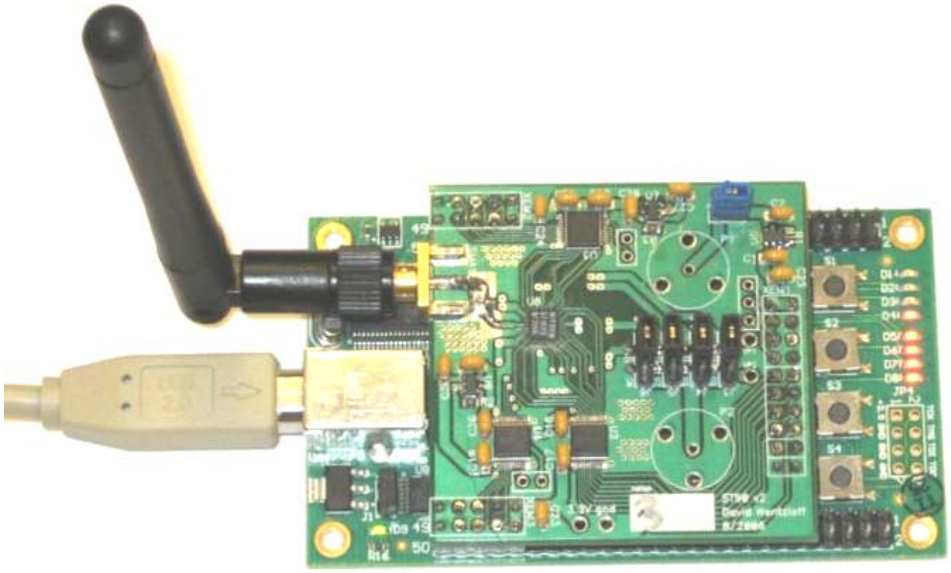


Out-of-band SIR: -15dBm at 2.45GHz, -20dBm at 5.45GHz

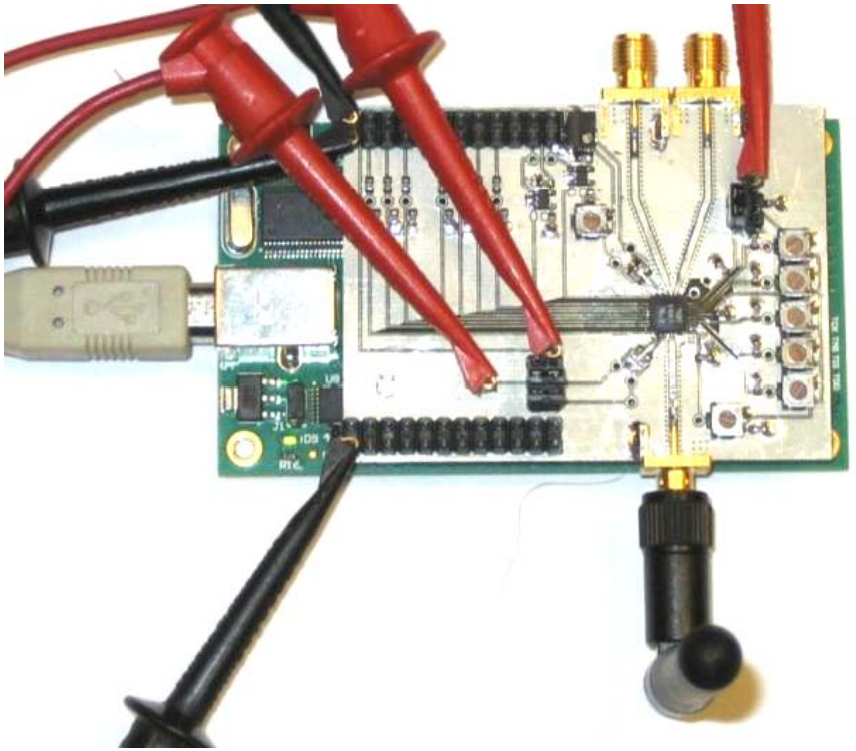
Wireless Nodes

- Demonstrated 16.7Mb/s wireless link
- Commercial FPGA boards with USB interface
- Streaming video by sending a sequence images

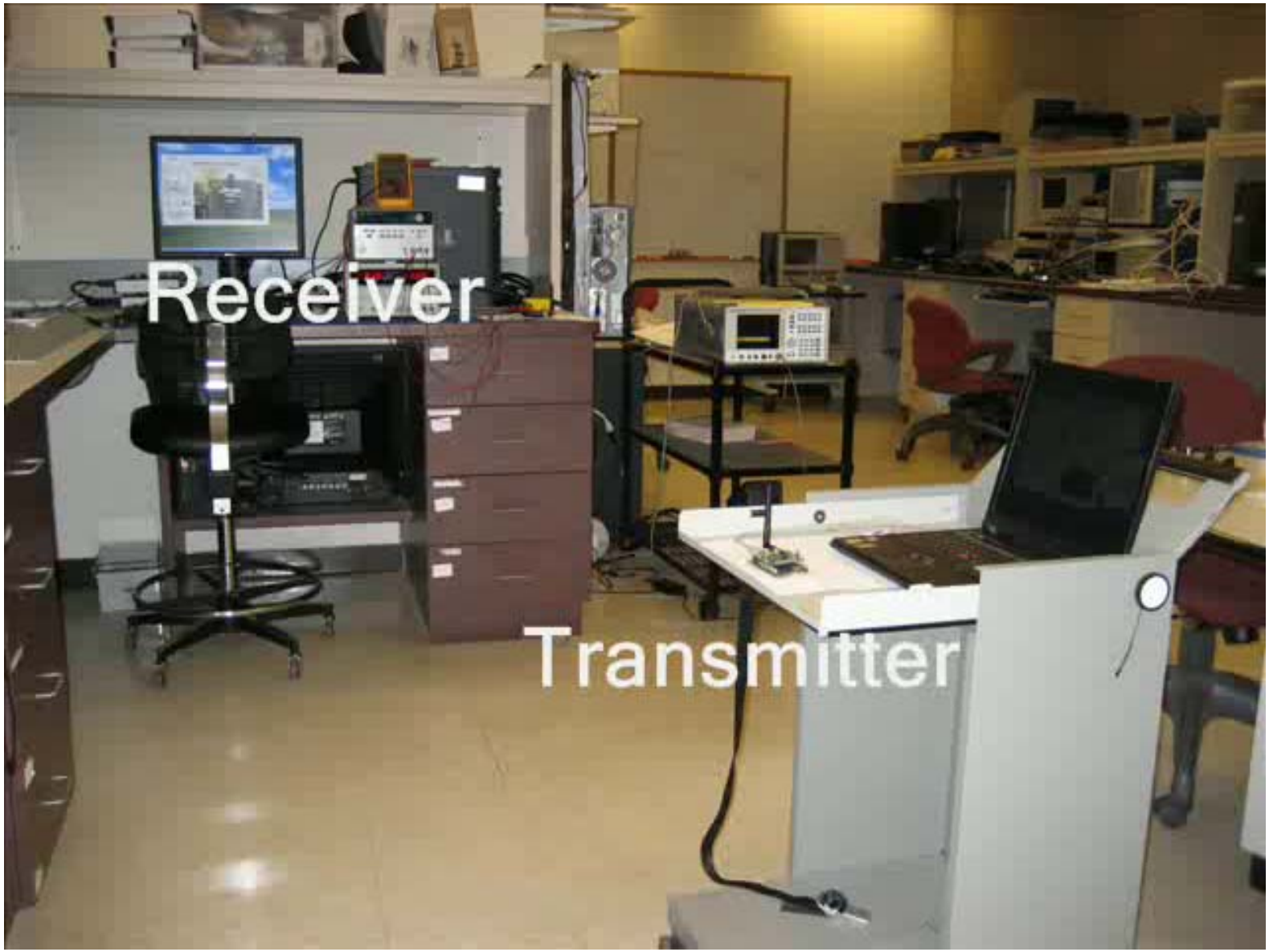
Transmitter



Receiver



Wireless Demonstration



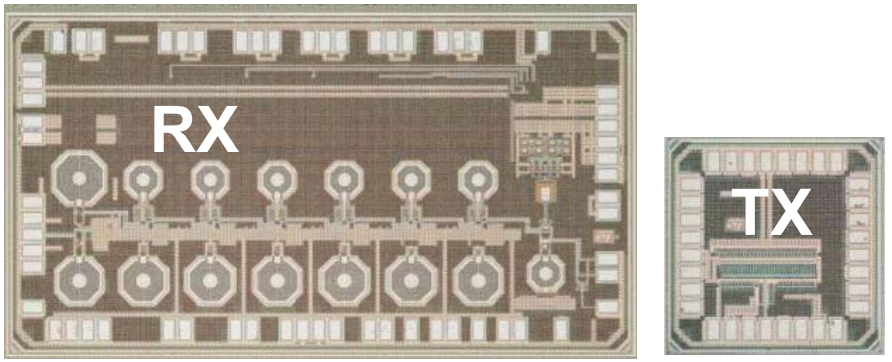
Conclusions

	Transmitter	Receiver
Die area	0.2x0.4mm^2	1.0x2.2mm^2
V_{DD}	1.0V	0.5-0.65V
Leakage	96μW	3.5μW
Power	0.72mW	41.8mW
Energy/bit (16.7Mb/s)	43pJ/bit	2.5nJ/bit

90nm CMOS

1mm

[F. Lee, ISSCC2007]



[D. Wentzloff, ISSCC2007]

- UWB signaling enables relaxed frequency tolerance ►CMOS integration
- Digital TX, non-coherent RX ► no RF oscillators
- Future directions: integrate TX and RX, eliminate off-chip filters, support for 802.15.4a

Acknowledgements – MARCO/DARPA Focus Center for Circuit & System Solutions (C2S2), National Science Foundation (NSF), and STMicroelectronics for chip fabrication