6.4 A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS

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Pulsed-UWB transceivers have the potential for ultra-low energy per bit operation since the signals are inherently duty-cycled. By eliminating components with long startup times such as a phase-locked loop, all the blocks in a pulsed-UWB transceiver can be disabled during the interval between pulses. In this paper, an *all-digital* transmitter with static logic and no bias currents is presented in which the energy is dissipated in switching events (i.e., CV^2) and by leakage currents (i.e., subthreshold leakage).

Typical pulsed-UWB systems operate in a single channel in the UWB band [1-3], which is shared spectrum with other UWB and narrowband users. System performance degrades in the presence of in-band interferers, which motivates the use of multiple channels for added diversity. This system uses 3 channels with center frequencies of 3.45, 4.05, and 4.65GHz, and each channel carries 550MHz wide pulses. This transmitter operates with a separate receiver IC that performs energy detection in the desired channel. Pulse-position modulation (PPM) is used with a pulse repetition frequency (PRF) range of 10kHz to 16.7MHz and a fixed PPM delay of 30ns.

A block diagram of the transmitter is shown in Fig. 6.4.1. Pulses are formed by combining a programmable number of equally delayed edges, similar in operation to a frequency multiplier. During pulsed operation, the last stage of the delay line feeding back to the input is disabled and the input to the delay line is a clock signal operating at the PRF. Depending on the data, the rising edge of this clock may be externally delayed by the PPM interval of 30ns. This clock propagates through the 32-stage differential delay line with a delay controlled by an 8b code, which generates a series of edges. The negative output of each cell is masked depending on a mask register value, thus only the selected edges are combined to form an RF pulse. The output edges of the first and last stages are not used. The 30 masked edges are combined using interleaved 15-edge combiners that toggle their outputs only on falling edges on any of their inputs [4]. Thus, pulses are generated only on the rising edge of the PRF signal. The outputs of the combiners are XORed and buffered by an inverter chain with variable gain. A timing diagram of the pulse generation is shown in Fig. 6.4.2. The resulting pulse has a center frequency determined by the delay per stage and a pulse width equal to an integer number of RF cycles determined by the number of edges selected. As the desired center frequency varies, so must the number of RF cycles to maintain a fixed pulse width. The required resolution of the delay control is determined by the RF frequency range and desired accuracy, as well as process variation. In simulations, the delay per stage varies by ±30% over process corners, which is factored into the total range. The center frequency accuracy can be relaxed to ±25MHz since the receiver performs self-mixing of the pulse. A resolution of 7b is sufficient to meet this specification, incorporating variation. An 8b value is implemented with overlapping codes for redundancy.

A schematic of a delay element is shown in Fig. 6.4.2. The delay is varied by current-starved inverters and a switched MIM capacitor bank. The 8b control value is divided into 6b for the binary-weighted current-starving networks and 2b for the binary-weighted MIM capacitor banks. The output of each delay stage is independently masked such that only a selected edge is combined to form the RF pulse. The mask bit is selected from one of two registers containing 30b programmable mask sets. The selected mask register may be changed on a per-pulse basis. This functionality is used to scramble the output spectrum, discussed below.

The delay line is calibrated off-line in a digital loop that determines the 8b code required for each center frequency. While calibrating, the initial buffer stage driving the delay line is disabled and the last stage is enabled (Fig. 6.4.1), configuring the delay line as a free-running ring oscillator. The frequency of the ring is digitally measured by counting the ring cycles for a fixed period of time. A successive-approximation search algorithm is used to determine the 8b delay code. For each capacitor bank setting, the algorithm cycles through the 6b current-starving code, while comparing the measured frequency to a predefined value. A full search requires 62µs, but the algorithm will stop early once the RF frequency is within range.

PPM signals are known to have spectral lines that are not present in BPSK systems [5]. Thus, a PPM transmitter may need to reduce its output power in order to remain FCC compliant. BPSK scrambling is typically used with PPM to spread these tones [1], but this is at the cost of added energy per pulse. BPSK scrambling is invisible to an energy detection receiver, since the received signal is squared. A delay-based BPSK (DB-BPSK) for scrambling pulses is proposed and is shown pictorially in Fig. 6.4.3. Instead of inverting the pulse, it is delayed by half of the RF period. If the pulse consists of more than 5 RF cycles, DB-BPSK has the same spectral properties in the main lobe as BPSK modulation. This is demonstrated in Fig. 6.4.3, comparing a PPM spectrum with and without DB-BPSK scrambling, where the tones are reduced by 10dB. DB-BPSK is implemented using the R0 and R1 mask registers shown in Fig. 6.4.2. The mask values in these two registers are offset from each other by 1 bit to implement the half-RF period delay. A PN sequence then selects which mask is used for each pulse.

A benefit of DB-BPSK phase scrambling is the simplification of the output amplifier, shown in Fig. 6.4.4, which is a chain of scaled inverters. The stacked devices in the final output stage reduce leakage current, and are used to implement a 3b linear-in-dB gain scaling. The spectrum for each gain setting is shown in Fig. 6.4.4 for a 4.05GHz pulse. The pulsed output of the inverter chain has spectral content at DC, therefore an off-chip band-select filter has been used to eliminate this.

The measured spectrum for the three channels with DB-BPSK scrambling enabled are superimposed in Fig. 6.4.5. The chip is fabricated in a 90nm CMOS process and consumes a fixed 96µW due to leakage currents. The active energy added while pulsing is 37pJ/pulse, independent of the PRF. At 10Mb/s, the total energy consumption (active and leakage) is 47pJ/bit. The transmitter is capable of generating pulses up to a PRF of 50MHz. BD-BPSK pulses at 4.05GHz are shown in Fig. 6.4.6, demonstrating the effective inversion from a half-RF period delay. A die micrograph is shown in Fig. 6.4.7.

Acknowledgements:
This work is funded by the MARCO/DARPA Focus Center for Circuit & System Solutions (C2S2) and the National Science Foundation (NSF) under Grant ANI-0335256. We thank STMicroelectronics for chip fabrication.

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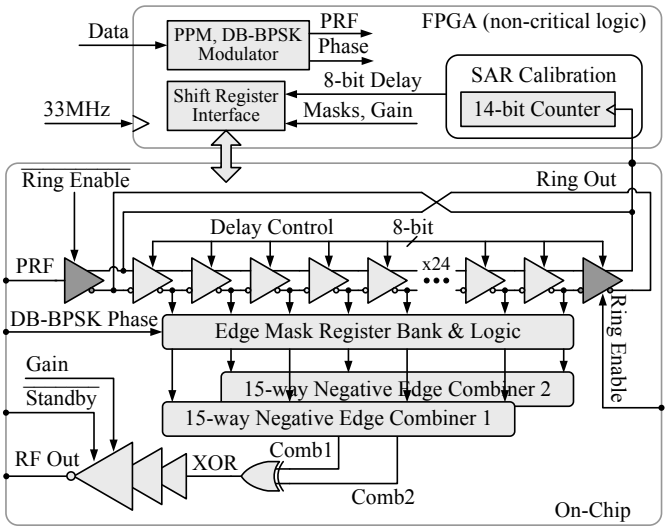


Figure 6.4.1: Block diagram of the transmitter with external calibration control.

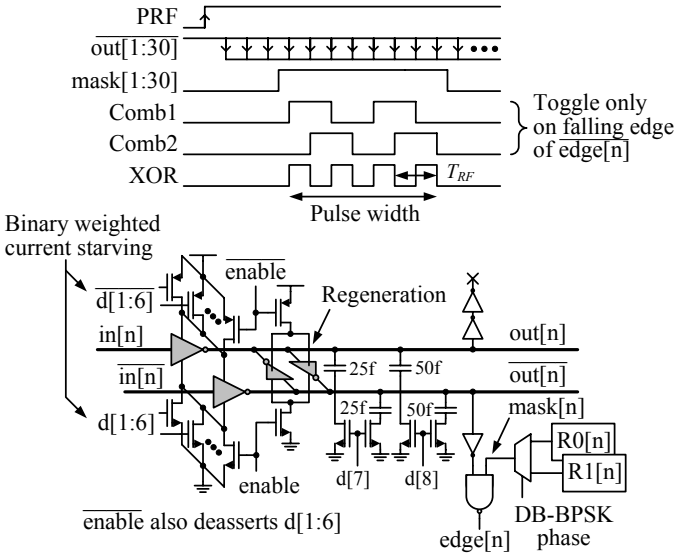


Figure 6.4.2: Schematic of a delay cell with independent masking of the output edge.

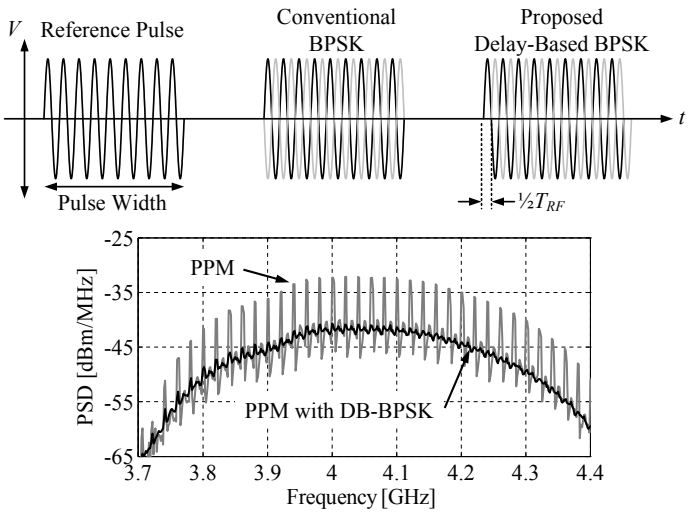


Figure 6.4.3: Conceptual drawing of delay-based BPSK (DB-BPSK) compared to conventional BPSK, and measured spectrum comparing DB-BPSK and PPM.

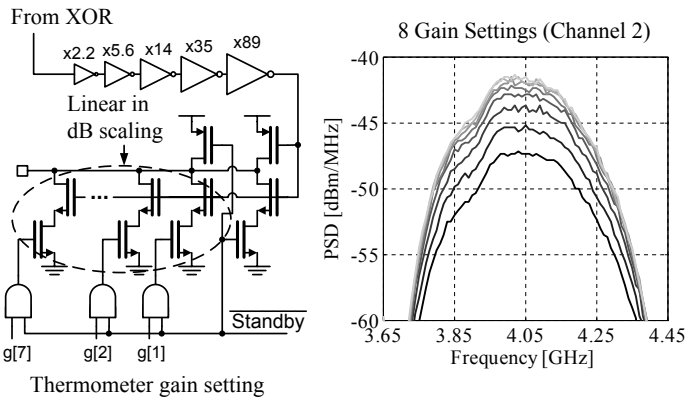


Figure 6.4.4: Schematic of the output buffer with linear-in-dB gain settings and standby mode for leakage reduction.

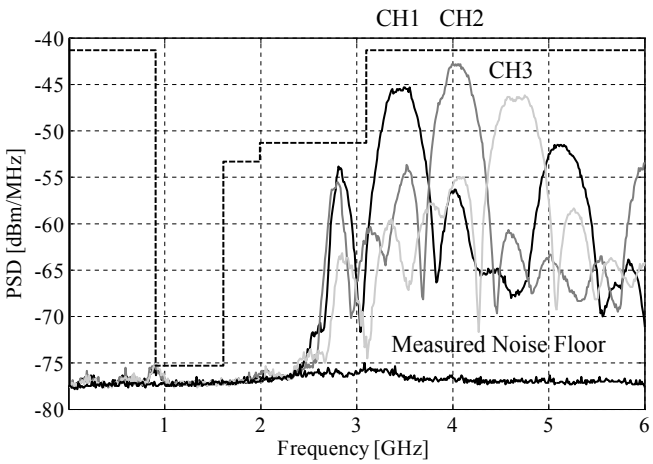
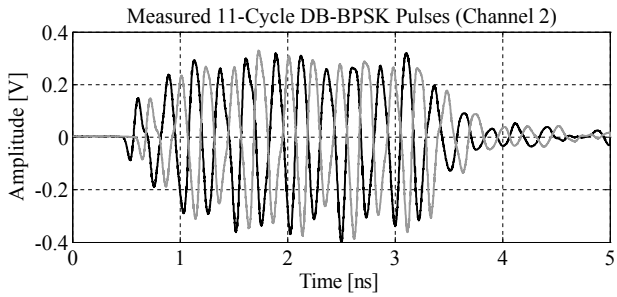


Figure 6.4.5: Superimposed measured output spectrum in each channel at a 10MHz PRF with DB-BPSK scrambling turned on.



Process	90nm CMOS
Die Area	0.2x0.4mm^2
Modulation	PPM
Scrambling	DB-BPSK
PRF Range	10kHz to 16.7MHz

Supply	1V
Standby Power	96µW
Active E/pulse	37pJ/pulse
Energy/pulse over PRF range	9.6nJ/pulse to 43pJ/pulse

Figure 6.4.6: Measured 4.05GHz pulses after off-chip high-pass filtering and transmitter performance summary table.

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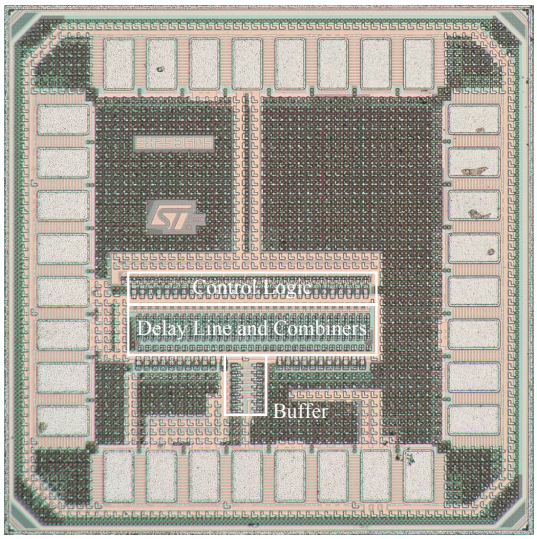

Figure 6.4.7: 90nm CMOS UWB transmitter die micrograph.

