Design Considerations for Next Generation Wireless Power Aware Microsensor Nodes

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Emerging Microsensor Applications

Industrial Plants and Power Line Monitoring
(courtesy ABB)

Operating Room of the Future
(courtesy John Guttag)

Target Tracking & Detection
(Courtesy of ARL)

Location Awareness
(Courtesy of Mark Smith, HP)

NASA/JPL sensorwebs

Websign
## Sensor System Requirements

### Predictable Constraints

<table>
<thead>
<tr>
<th>Application Characteristics</th>
<th>Typical Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>bps to kbps</td>
</tr>
<tr>
<td>Spatial Density</td>
<td>0.1-10 nodes/m²</td>
</tr>
<tr>
<td>Transmission Distance</td>
<td>10 – 100m</td>
</tr>
<tr>
<td>Extended Lifetime</td>
<td>5 years</td>
</tr>
<tr>
<td>Small Size</td>
<td>1 “AA” battery</td>
</tr>
</tbody>
</table>

### Unpredictable Diversity

- **Network roles:** relay, sensor, aggregator
- **Environment:** event and signal statistics
- **User/Application:** required latency, quality

**Application-specific designs** provide energy efficient point solutions

**Power-aware designs** adapt energy consumption to operating conditions
Low-Rate Digital Computation

$I_{\text{leakage}} \propto 10^{(-V_T/S)}$

Energy Harvesting

MAC and Protocols

Energy-Scalable Algorithms

RF Innovations

API and Control

Power Aware Microsensor Networks
First Generation Wireless Microsensor

Sensor:
- Mic.
- Amp
- Low-Pass Filter
- ADC
- Battery

Processor:
- Static RAM
- Flash ROM
- Control
- FIFO
- Clock Recovery
- Shifter
- DC/DC Converter
- Processor
- FIFO

Radio:
- Radio IC
- Antenna
- Power Amp.
- 206MHz StrongARM
- 2.4GHz ISM band

Implemented on an FPGA

4-channel acoustic
- **Active Power Management**: DVS, variable ECC and packet size, variable transmit power, agile algorithms
OS-Controlled Power Down Modes

Data collection: 1024 samples at 1kSPS
(Processor alternates between idle/active)

LOB Calculation
(Processor active full-time)

Data transmission
(Radio transmitter active)

Sleep
(All systems power down)

Power (mW)

Time (s)

Processor Idle:
low = idle
high = active

Processor Sleep:
low = sleep
high = active or idle
Dynamic Voltage Scaling

Digitally adjustable DC-DC converter powers SA-1110 core

µOS selects appropriate clock frequency based on workload and latency constraints
Leakage: Low Duty Cycle Concern

Leakage Dominates Switching Energy for Low Duty Cycles – “Off” State-centric Optimization

\[ I_{\text{leakage}} \propto 10^{-\frac{V_T}{S}} \]
- Fine-grain shutdown through regulators and bias control
- Variable 6-level PA allows efficient transmission for 10m to 100m
Energy = \( P_{\text{tx_electronics}} \left( T_{\text{transmit}} + T_{\text{start}} \right) + P_{\text{out}} T_{\text{transmit}} \)

- Significant loss in energy efficiency for small packet sizes

**Startup Costs are Fundamental – Innovative Circuits and Protocols Required**
Next Generation Sensor Nodes

Sensor System-on-a-Chip

- Compact Form Factor \((mm^3 – cm^3)\)
- Low Rate Radio link \((10-100kbs)\)
- System Power < 100\(\mu\)W

Energy Source and Regulation

- Sensor & A/D
- Sensor Specific Cores (FFT, Matched Filters, etc.)
- Low-End Sensor DSP Processor
- Protocol Processor (Baseband and MAC)
- RF Transceiver

Network API/Simulation

Region of Observation Base Station

- How to simulate 1000’s nodes?

Ultra-Wideband Radio

- High-speed & Low-power Time Domain Processing
- Police Train
- Simulink

Energy Processing

- How to Scavenge 100\(\mu\)W?

Ultra Low-Voltage Digital Circuits

- Design for 100mV Supply

Mixed-Signal Design

- How to Integrate RF & Digital?
Energy Scavenging: Vibration-to-Electric Energy

10\mu W from generator possible

MEMS Generator

Controller
“Software” Energy Dissipation is Dominated by Overhead and NOT by Useful Work
Leakage Mitigation Using MTCMOS

Device Sizing is a Major Concern in Multiple Threshold CMOS
Look at A=0 and B=1.
Sneak Leakage!!
Power Aware Architectures

Single butterfly architecture
(4 multipliers, 6 adders)

Control Logic

Twiddle Address

Twiddle ROM

R/W

A

B

W

Data Address

X

Y

Data Memory

Butterfly structure

FFT Computation

Power Scalable Multiplier
(modified Baugh-Wooley)

W

X=A+BW

Y=A-BW

Power Scalable Memory

Address (write/read)

data (write)

128x32

128x32

64x32

64x32

32x32

32x32

16x32

16x32

16x32

16x32

Control Logic

128x32

64x32

32x32

16x32

Adder used only in 16-bit mode
Adder used in 8-bit and 16-bit mode

Data (read)

8-bit feed through X{15:8}

input gating

Y{15:0}

X{15:0}

Z{15:0}
First Generation Power Aware FFT

Technology Parameters

- $0.18 \mu m$ process
- $2.1mm \times 3mm$
- $V_{T0n} = 0.45V$, $V_{T0p} = -0.44V$
- $V_{dd} = 1.8V$

Measured energy dissipation

<table>
<thead>
<tr>
<th>Points</th>
<th>8-bit</th>
<th>16-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>128 pt.</td>
<td>46 nJ</td>
<td>81 nJ</td>
</tr>
<tr>
<td>256 pt.</td>
<td>121 nJ</td>
<td>216 nJ</td>
</tr>
<tr>
<td>512 pt.</td>
<td>304 nJ</td>
<td>564 nJ</td>
</tr>
</tbody>
</table>

Power programmable from 128pts to 512pts and 8 bits and 16 bits
Energy Efficiency of Digital Computation

FFT Computation

Single butterfly architecture (4 multipliers, 6 adders)

Control Logic
Twiddle Address
Data Memory
Twiddle ROM
R/W
W
A
B
X=A+BW
Y=A-BW
Butterfly structure

Exploit Sub-threshold Operation for Sensor Circuits
Adaptive $V_{DD}/V_T$ Architecture

Circuit to be biased to optimum $V_{DD}/V_T$ point

- Lookup Table
- Power Converter
- Matched Delay Line
- Phase Detector
- N/P Body Bias Generator

[MAC, 166 kHz clock, Data]

[Miyazaki, ISSCC '02]
New Energy Metrics in DSM Interconnect

\[ \lambda = \frac{C_I}{C_L} = 3 \]

```
<table>
<thead>
<tr>
<th># of transitions of cost E</th>
<th>Standard model</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>30</td>
</tr>
<tr>
<td>1</td>
<td>20</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>
```

```
<table>
<thead>
<tr>
<th># of transitions of cost E</th>
<th>Sub-micron model</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>18</td>
</tr>
<tr>
<td>1</td>
<td>16</td>
</tr>
<tr>
<td>2</td>
<td>14</td>
</tr>
<tr>
<td>3</td>
<td>12</td>
</tr>
</tbody>
</table>
```

Input Data (n bits) → Encoder → Extended Bus (n+a lines) → Decoder → Recovered Data

Minimizing Transition Activity is not the Right approach to Minimize Power
Computation vs. Communication

- Computation: 1nJ/op (μ-Processor) and Communication (@10m): 150nJ/bit
- @10 m: ~150 instructions/transmitted bit on a low-power processor
- @10m: > 1Million instructions/transmitted bit using dedicated hardware

Compute, Don’t Communicate
Fast Startup Transmitter

Data $\rightarrow$ LPF

$\text{PFD}$

$\text{Variable loop filter}$

$\text{Variable loop filter}$

$\frac{f_{\text{ref}}}{N}$, $\frac{f_{\text{ref}}}{N+1}$

$\Sigma-\Delta$

channel

$E/\text{bit} = 10\text{nJ/bit}$

Fixed loop bandwidth

Variable loop bandwidth
New Opportunities: “Digital” UWB Radio

- Minimal Front-end components: leverage low-power digital circuits
- 3-4 bits A/D sufficient  (Newaskar, Blazquez, Chandrakasan, SIPS ‘02)
Multihop and the Characteristic Distance

**Direct Transmission**

\[ E = \alpha_1 + \alpha_2 D^2 \]

- Tx & Rx Radio Electronics
- Attenuation, power amp
- Path loss exponent

**Multihop Transmission**

\[ E = h \left[ \alpha_1 + \alpha_2 \left( \frac{D}{h} \right)^2 \right] \]

- Number of hops
- Per-hop distance

**Characteristic Distance for Multihop Transmission**

\[ \min E = 2\alpha_1 \frac{D}{d_{\text{char}}} \]

where \[ d_{\text{char}} = \sqrt{\frac{\alpha_1}{\alpha_2}} \]
Multi-Hop Routing Analysis

- Take advantage of dense sensor networks by using several shorter hops to transmit long distances.
- Plot of total power used to transmit a given distance for 1, 2, 3, and 4 hops:
  - Large power step in each trace from turning on external PA.
  - Trace out lowest curve for energy efficiency (i.e. use 3 hops @ 1000 m).
- Multi-hop routing is more energy efficient for this particular radio:
  - Adds overhead to the protocol.
  - Adds latency to the network.

![Diagram showing multi-hop routing with 1, 2, and 3 hops, and a direct hop.]
Power Aware API: performance of communication defined and exposed as a basis for trade-offs

- `set_max_energy(Energy energy)`
- `set_max_latency(Time latency)`
- `set_min_reliability(Prob probReception)`
- `set_range(int nearestNodes, Node[] who, float meters)`

**Quality of communication defined along four axes:**

<table>
<thead>
<tr>
<th>Concern</th>
<th>Metric</th>
</tr>
</thead>
<tbody>
<tr>
<td>“To whom?”</td>
<td>Range (m)</td>
</tr>
<tr>
<td>“How soon?”</td>
<td>Latency (ms)</td>
</tr>
<tr>
<td>“How reliably?”</td>
<td>Reliability (BER)</td>
</tr>
<tr>
<td>“How much energy?”</td>
<td>Energy (µJ)</td>
</tr>
</tbody>
</table>
Energy scales gracefully with communication quality
Conclusions

- Exciting new applications enabled by a network of low-power wireless sensing devices
- Power Aware Design Methodology supersedes Energy Efficient Design
- *Slower is Better* – exploit sub-threshold operation as fastest switching speed is not needed
- *Communication-centric design*
  - Energy per operation (mW/MIPS) will scale with technology
  - Communication costs (nJ/bit) will not scale at the same rate