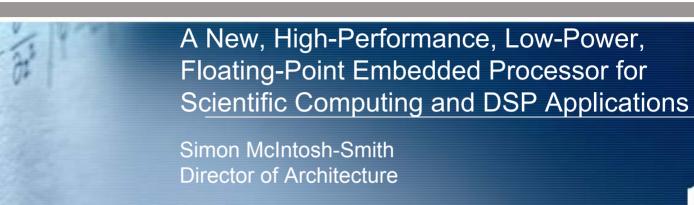
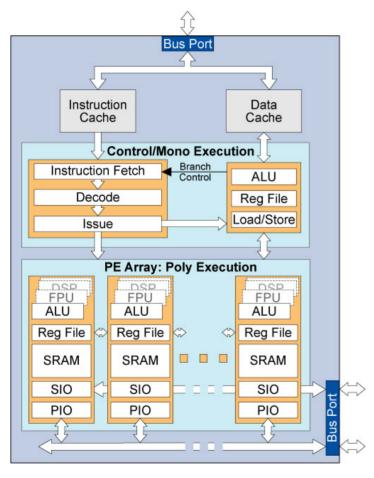
# ClearSpeed / Advance



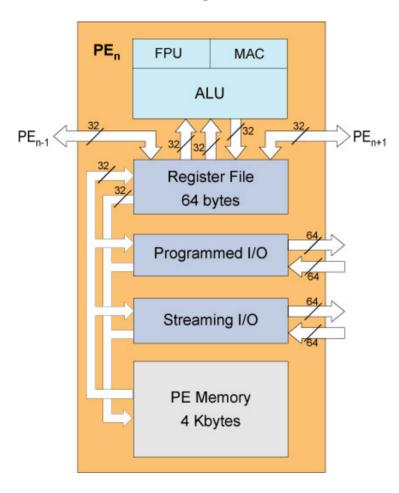
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### Multi-Threaded Array Processing Architecture



- Multi-Threaded Array Processor
  - Fully programmable in C
  - Hardware multi-threading
  - Extensible instruction set
- Scalable internal parallelism
  - Array of processing elements (PEs)
  - Compute, bandwidth scale together
  - From 10s to 1,000s of PEs
  - Built-in PE redundancy
- High performance, low power
  - ~10 GFLOPS/watt
- Multiple high-speed I/O channels

#### **Processing Elements**

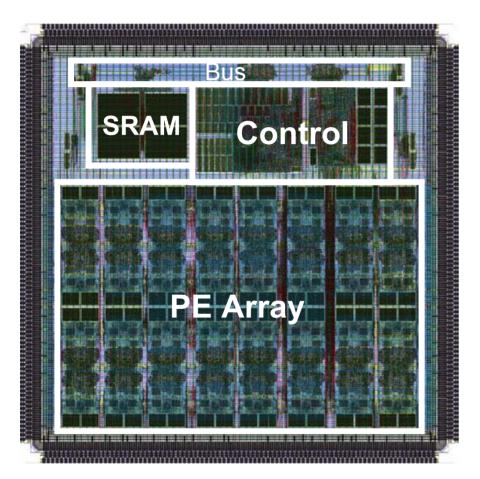


- PEs are highly optimised execution units
  - ALU, MAC, FPU

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- High-bandwidth, multiport register file
- High bandwidth per PE DMA (PIO, SIO)
- Closely coupled SRAM for data
- 64 PEs at 200MHz
  - 25.6 GFLOPS
  - 51.2 Gbyte/s bandwidth to PE memory
  - 12,800 MIPS
- Supports multiple data types
  - 8, 16, 24, 32-bit, ... fixed-point arithmetic
  - 32-bit IEEE floating-point arithmetic

# CS301 Up Close

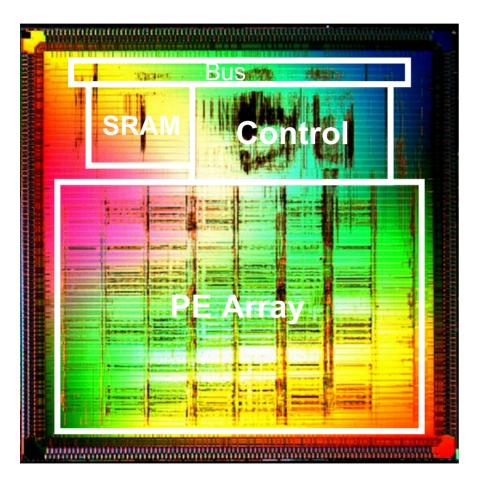


- Multi-Threaded Array Processor
  - 25.6 GFLOPS
  - 3W worst-case, 2W typical
  - 200MHz

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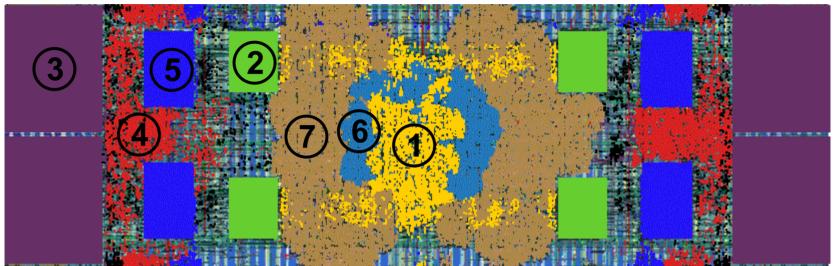
- 64 PEs, 4 Kbytes each
- ClearConnect bus
  - 64-bit full duplex
  - 1.6 Gbyte/s each direction
  - 2x 0.8-Gbyte/s bridge ports
- Scratchpad memory
  - 128 Kbytes of SRAM
- Availability
  - Sampling Q4 2003

# CS301 Up Close



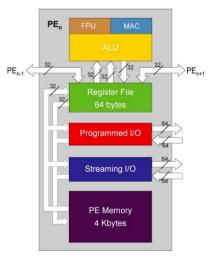
- Multi-Threaded Array Processor
  - 25.6 GFLOPS
  - 3W worst-case, 2W typical
  - 200MHz
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  - 64-bit full duplex
  - 1.6 Gbyte/s each direction
  - 2x 0.8-Gbyte/s bridge ports
- Scratchpad memory
  - 128 Kbytes of SRAM
- Availability
  - Sampling Q4 2003

# 4 PEs - Array Building Block



- 1. ALUs
- 2. Register files
- 3. PE memories

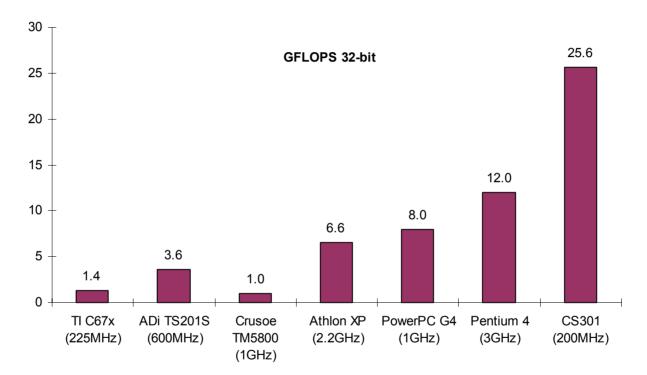
- 4. PIO
- 5. SIO
- 6. Integer MACs
- 7. FPUs



\* Captured using Magma's Blast Fusion®

#### CS301 Facts and Figures

- IBM 0.13µ FSG process, 8-layer metal (copper)
- Standard cell library, fully synthesized design
- 8.5 x 8.5mm active logic area 72mm<sup>2</sup>
- 41 million transistors (32% logic, 68% memory)
- 1.2V core, 2.5V I/O (3.3V tolerant)
- 343 signal pins (235 mission mode, 108 diagnostic)
- Plastic PBGA package

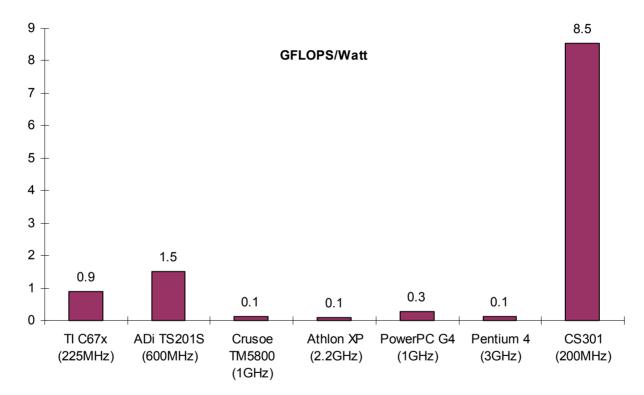


## Peak GFLOP Comparison

CS301 can accelerate, amongst others:

High-performance computing tasks in PC and blade server systems Embedded DSP applications

## **GFLOPS** Per Watt Comparison



CS301's high performance and low power enables: New levels of density in PC and blade server systems New levels of performance in embedded DSP applications.

Sources: vendor websites





- Lockheed Martin has benchmarked two applications with optimised code supplied by WorldScape Defence on the CS301 cycle-accurate simulator:
- A 1024-point, complex, floating-point FFT, 8 FFTs performed in parallel
- Pulse compression: an FFT, a complex multiply by a stored reference FFT, and an IFFT, with 8 pulse compressions performed in parallel

Processor	Clock	Power	FFT/sec /Watt	Pulse Compressions /sec/Watt		
PowerPC 7410	400 MHz	8.3W	8.3W 3,052			
ClearSpeed CS301	200 MHz	2.0W*	56,870	24,980		
Improvement			18.6 X	31.9 X		

\* Measured on gate level sim with Magma's Blast Rail

#### ClearSpeed

#### **Development Environment**

Software Development Kit (SDK)

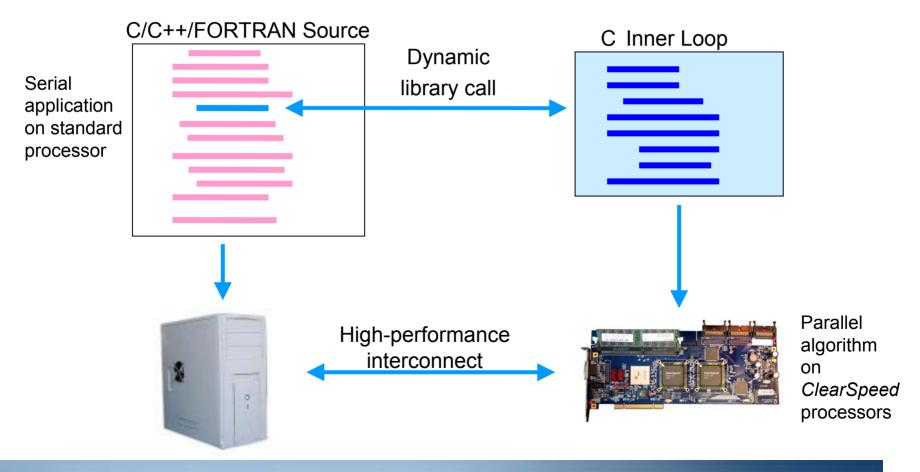
- C compiler, assembler, libraries, visual debugger, etc.
- Instruction-set and cycle-accurate simulators
- Available for Windows, Linux, and Solaris
- Development boards, early silicon available from Q4 2003

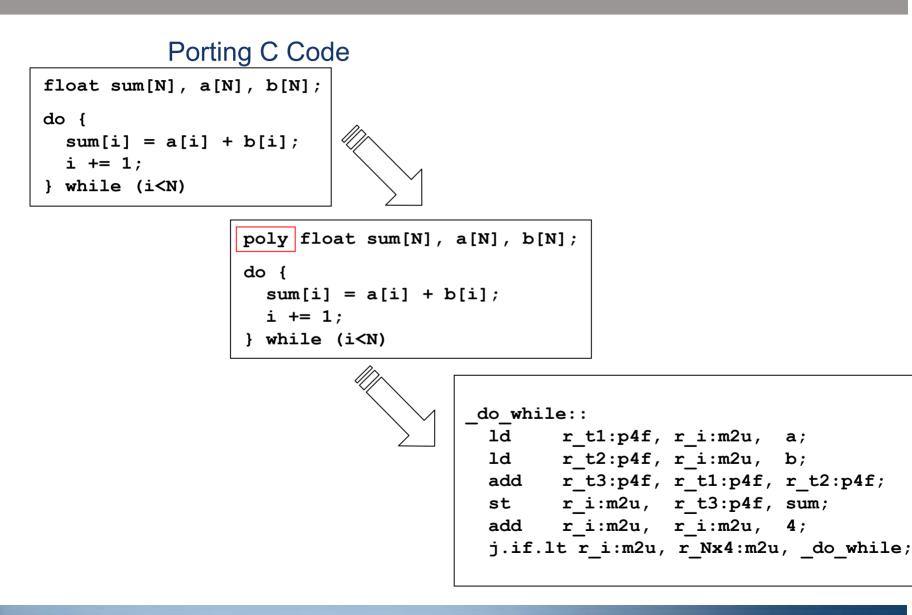
Application development support

- Reference source code for various applications
- Consult directly with *ClearSpeed's* experts
- Consultancy and optimised code from *ClearSpeed's* partners

### **Accelerated Applications**

*ClearSpeed's* co-processor technology is designed to accelerate the *inner loops* of compute-intensive algorithms.





# ClearSpeed Debugger

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	and beed beed beed beed beed	-		egeter rame	Register value						
and verver	Justice data 1.251		190	10.4	0000007e	Address	Label	Op code.	Argt	Arg2	Anjis
Viewer 15	#define STEP: ((HAO) - HIN) / HUNCOLS) // Increment for each screen coordinate		944		deatheef	00010520		H.	24p4	4 m2 + Do.	
r viewer 16	sdefine STEPY (CHACY - HINY) / NUMBONS)		948		deadbeef	00013524	9 8	#	4:n2	+ 0x50	24:p4
17	fidefine \$23 150 // Haz maker of iterations		9112		deadbeef	00010520	8 8	*	0.m4	+ 0.09	0.m4
Vewer 10	The second	1	19.10		deadbeef	0001352C	1 8	mana inve.	0x2554		
20	// Define a function to test the termination condition for a given (x, y) coordinate.	1	PR20		00000000 (0000000)	00010500		TE EFF	0.m2	D.m.D	
21	27	1 2	828		DEDEDEDED	00013524		mana inte.			
72	/* Evaluate the termination condition in parallel */	11 - 3	832		+0000000	00010530		TE EFF	10.m2	D.m.D	
23	poly int terminate(poly float x, poly float y) (	1	830		3000000	00010530	22	add	0.782	D.m2	0:40
24	return (x*x + y*y + 4.0f);	1	19-80		149333333	00013540	<u> </u>	addc	2782	2.92	0
26		1 d	0.44		Lef00000	00013544	<u> </u>	numina.			
27	//	1 2	0.00		moren	00010540		add	4:n2	4 m2	0.782
24	// The main part of the work is done in the function calcres() which evaluates the result a	Here	desired.	- bata see	PEserber	0001054C		j.lu	tus .	Di-20 #3	
2.9	37					00010550		LN.	\$2.16	Di@001	
20	poly char calcresiance float s, poly float y, aces int resi (	Tree	-1	4 2	0 0	000 0000		aub	0.m2	Dind	0.40
31.	poly char result; // Different result on each FE poly int turnedon; // Each FE doer a different number of iterations	100				00013550		nde namina.	2782	2.02	0
21	int 1: // but they all go round the same loop	1			ana katan d	00010550		num inn.	4/82	4 m2	0.782
24	poly float ty; // Intermediate values for each FE	D	10	20	30 40 5	00013564	-	IN IN	4/m2 0/m4	A Put	+ 0x29
36	poly float scale, yealc;					00013564		TRAV	29 p2	D:p2	+ 10020
34						00013550		Dire .	20 pc 30 p2	2:92	
37	/* Bet the scale cumulative value to its initial value */ scale = x;					00013570		#		+ Dod0	21 p4
22	<pre>/* Set the yealc cumulative value to its initial value */</pre>	100		U.S.		00010574		14	20.24	4 m2 + Dx	21.04
40	yealc + y:	Enabl	. State and	Status Register	Pairflegitat FairMano	00010570		nun inn.		4.10.7 00.	
44		1000		E. C. Starter	CARD CONTRACT	00012570		0/52	20 p2	D:m2	
42	result = D:		Matas store	1 *	Attant	90012590		num ing.			
43	/* Initialise flag to control iterations */ turnedon = 1;	100	Hitsgan	1	A State of the sta	00012594		0.000	22 p2	D:m2	
47         of the final           48         rejurts will           49         for (i * 0) i *           50         /* Ouly com           51         if trumwing           52         /* Ouly com           53         if trumwing           54         /*/           55         if           56         else i           57         i           58         else i           59         /*/           61         real           62         i           63         i           64         i           65         else i           66         i           67         i           68         else i           69         //           60         i           61         recum result           62         i//           63         i//           64         i           65         i//           66         i//           67         i//           68         i//           69         i//           60         i// <th><pre>/* But the values for the matt iteration */ tr = stall * scale - proje = ypais * yrais + s; yrais * 2.01 * scale * yrais + y; '' '' '' '' '' '' '' '' '' '' '' '' ''</pre></th> <th>ľ</th> <th>Amber of co 5 3 Amber of ro 5 3 4 4 4 5 0 0 0 0 0 0 0 0 0 0 0 0 0</th> <th>13 17 21 m5 13 17 21</th> <th>25 29 30 37 41 25 29 30 37 41 25 20 20 40 45 73 52 50 46 40 40 17 64 30 40 18 60 40 19 60 40 10 60 10 60 100 100 100 100 10000000000</th> <th>45 48 5</th> <th></th> <th></th> <th>Church alba 28 4 23342483 57 23342483 57 23444455555555557575555555757555557575757</th> <th>**************************************</th> <th></th>	<pre>/* But the values for the matt iteration */ tr = stall * scale - proje = ypais * yrais + s; yrais * 2.01 * scale * yrais + y; '' '' '' '' '' '' '' '' '' '' '' '' ''</pre>	ľ	Amber of co 5 3 Amber of ro 5 3 4 4 4 5 0 0 0 0 0 0 0 0 0 0 0 0 0	13 17 21 m5 13 17 21	25 29 30 37 41 25 29 30 37 41 25 20 20 40 45 73 52 50 46 40 40 17 64 30 40 18 60 40 19 60 40 10 60 10 60 100 100 100 100 10000000000	45 48 5			Church alba 28 4 23342483 57 23342483 57 23444455555555557575555555757555557575757	**************************************	
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# Systems Integration Examples



Laptop plug-in accelerator



#### PC plug-in accelerator



Coprocessors in a PC server\*



Coprocessors in a blade server\*

\* Images courtesy of Angstrom Microsystems

### ClearSpeed CS301 Summary

*ClearSpeed's* CS301 fully programmable accelerator delivers compelling floating-point performance and performance per watt.

- 25.6 GFLOPS
- 3W worst-case, 2W typical
- 8.5 GFLOPS/watt
- 3.2 Gbyte/s off-chip bandwidth
- Gluelessly daisy-chain multiple devices for higher performance
- Program in C with a familiar, simple programming model
- Sampling Q4 2003