

Kai-hui Chang

M.S. Thesis: A Compiled-Code Technique for RTL Designs

- Developed a compiled-code RTL Verilog simulator based on an interpreted version.

Honors

Second Place – ICCAD Cadathlon (the most prestigious competition in EDA), 2006.

First Place – IEEE IWLS Programming Challenge, 2006.

National Taiwan University Presidential Award, four times, 1995-1999.

Affiliations

Association for Computing Machinery (ACM).

Institute of Electrical and Electronics Engineers (IEEE).

Professional Service

Organizer of the SVT student reading group at the University of Michigan, 2006-2007.

Reviewer for journals: *IEEE Trans. on CAD*, *ACM Trans. on Design Automation*, *IEEE Trans. on VLSI*

Reviewer for conferences: *ACM/IEEE Intl. Conf. on Computer-Aided Design (ICCAD)*, *IEEE/ACM Design Automation & Test in Europe (DATE)*, *ACM/IEEE Asia and South Pacific Design Automation Conference (ASPDAC)*

Selected Publications

(The complete list of publications is available at <http://www.eecs.umich.edu/~changkh>)

Functional Verification and Automatic Debugging

1. **K. H. Chang**, I. L. Markov and V. Bertacco, “Fixing Design Errors with Counterexamples and Resynthesis”, to appear in *IEEE Trans. on Computer-Aided Design (TCAD)*, 2008
2. **K. H. Chang**, I. L. Markov, and V. Bertacco, “Automating Post-Silicon Debugging and Repair”, to appear in *Proc. Int'l Conf. Computer-Aided Design (ICCAD)*, Nov. 2007
3. **K. H. Chang**, I. Wagner, V. Bertacco, and I. L. Markov, “Automatic Error Diagnosis and Correction for RTL Designs”, *ACM/IEEE Int'l Workshop on Logic and Synthesis (IWLS)*, San Diego, CA, May 2007, pp. 106-113.
4. **K. H. Chang**, D. A. Papa, I. L. Markov and V. Bertacco, “InVerS: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization”, *Proc. Int'l Symp. on Quality Electronic Design (ISQED)*, San Jose, CA, Mar. 2007, pp. 487-492.
5. **K. H. Chang**, V. Bertacco and I. L. Markov, “Simulation-based Bug Trace Minimization with BMC-based Refinement”, *IEEE Trans. on Computer-Aided Design (TCAD)*, Vol. 26, NO. 1, Jan. 2007, pp. 152-165
6. **K. H. Chang**, W. T. Tu, Y. J. Yeh, and S. Y. Kuo, “A Temporal Assertion Extension to Verilog,” *Proc. International Symposium on Automated Technology for Verification and Analysis (ATVA04)*, Oct. 2004, Taipei, Taiwan, LNCS 3299, pp 499-504

Physical Synthesis

7. **K. H. Chang**, I. L. Markov and V. Bertacco, “Post-Placement Rewiring by Exhaustive Search For Functional Symmetries”, *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol. 12, No. 3, Article 32, Aug. 2007
8. **K. H. Chang**, I. L. Markov and V. Bertacco, “Safe Delay Optimization for Physical Synthesis”, *Proc. Asia and South Pacific Design Automation Conf. (ASPDAC)*, Yokohama, Japan, Jan. 2007, pp. 628-633
9. **K. H. Chang**, I. L. Markov and V. Bertacco, “Post-Placement Rewiring and Rebuffering by Exhaustive Search For Functional Symmetries”, *Proc. Int'l Conf. Computer-Aided Design (ICCAD)*, Nov. 2005, pp. 56-63

Parallel Simulation

10. **K. H. Chang et al.**, “Automatic Partitioner for Behavior Level Distributed Logic Simulation”, *Proc. Int'l Conf. Formal Techniques for Networked and Distributed Systems (FORTE)*, Oct. 2005, Taipei, Taiwan, LNCS 3731, pp 525-528
11. **K. H. Chang et al.**, “Techniques to Reduce Synchronization in Distributed Parallel Logic Simulation”, *Proc. IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS'04)*, Cambridge, MA, Nov. 2004.