A Two-Temperature Technique for PECVD Deposition of Silicon Dioxide

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Abstract—**A new technique has been developed and analyzed for plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide films which yields lower interface trap densities. First, a thin cap layer is deposited at a low temperature and the film is subjected to an *in-situ* hydrogen plasma treatment. Then the temperature is raised to the final value and the deposition continued to the desired thickness.**

RECENT trends in scaled MOSFET fabrication have stimulated interest in low-temperature silicon processing. One goal is to obtain deposited films that form trap-free interfaces and have good dielectric properties such as breakdown field. In addition, insulators on III–V semiconductors such as GaAs and InP exhibit a trade-off where low deposition temperatures form better interfaces but at the expense of film quality [1]. Higher deposition temperatures yield good dielectric properties but have increased interface trap densities (D_{it}), as well as promoting surface evaporation of the column V element. Usually, a compromise temperature is chosen for operation. A new technique has been developed using two deposition temperatures, a low temperature for the interface formation and a higher temperature for the bulk of the film. During the temperature ramp, the sample can be subjected to a variety of *in-situ* plasma and unexcited treatments. Hydrogen was chosen for the treatments to simulate the effect of a standard MOS post-metallization anneal. This technique was tested on silicon wafers since the well-behaved $Si-SiO_2$ interface makes trap densities easier to measure.

The plasma-enhanced chemical vapor deposition (PECVD) system utilized here is a parallel-plate SEMI Group model MPB 1000 operating at 13.56 MHz. It is a direct plasma configuration with the wafers exposed to the plasma. The samples used were n- and p-type (100) silicon wafers doped to 1–3-Ω · cm resistivities. After RCA cleaning, the wafers were promptly loaded into the PECVD chamber and the deposition process begun immediately. An SiO_2 recipe has been developed based on Batey and Tierney's publication [2] using high N_2O-to-SiH_4 ratios (130), high deposition pressure (400 mT), low RF power (30 W), and helium dilution of the reactants. Table I shows the refractive indices of the nominally 1000-Å films, as measured on a Gaertner L117 ellipsometer at a wavelength of 6328 Å. After deposition, the front was sputtered with Al and patterned to provide squares 500 μm on a side for CV testing. Al was then sputtered onto the back side of the wafers. The final processing step consisted of a 300°C film anneal in forming gas for 60 min. CV and $I-V$ measurements were performed and the interface trap distributions were calculated using the low-frequency [3] and high-frequency–low-frequency methods [4].

The control wafers (sample a) consisted of a standard uninterrupted deposition at 300°C. This yielded midgap D_{it}'s in the high 10^{10} range for both the n-type and p-type wafers. The next wafers (sample b) consisted of the same films followed by an *in-situ* H_2 plasma post-treatment. These yielded midgap D_{it}'s in the mid 10^{10} range, showing improvement over the control samples and demonstrating the effectiveness of an H_2 plasma in D_{it} reduction.

The next set of samples consisted of several variations of the two-temperature technique. The first set (sample c) consisted of 250 Å deposited at 300°C and the remaining 750 Å deposited at 350°C, with a low-power hydrogen plasma during the temperature ramp. The midgap D_{it}'s were again in the mid 10^{10} range but slightly lower than for the post-treated samples. With a 250°C initial temperature (sample d) the midgap D_{it}'s were higher than the previous result. This is because for silicon wafers, best results are obtained with a higher deposition temperature, contrary to the results obtained with III–V's [5]. The trends are reversed because silicon does not suffer from incongruent evaporation or the degrading effects of native oxides, as GaAs and InP do at elevated temperatures. It is expected that this technique on III–V's will be best with a lower temperature for the initial cap layer.

Several more variations on the two-temperature theme were then tested on n-type wafers. With a 100-Å initial cap layer for the 300–350°C films (sample e), the D_{it} improved to the low 10^{10} range. This is to be expected, as a thinner layer allows more effective hydrogen diffusion to the interface for trap-site annihilation. Fig. 1 shows typical $C-V$ and D_{it} curves for this process. Another alteration of the 300–350°C system was examined, where now the hydrogen plasma was replaced with an unexcited hydrogen flow (sample f). The initial thickness for these samples was the original 250 Å. The D_{it} for this set of wafers was again in the low to mid 10^{10} range. There seems to be a trade-off here, with the plasma providing more free hydrogen atoms yet causing more film damage due to ion bombardment and UV exposure. The last set of wafers consisted of 250 Å deposited at 300°C followed by a 10-min H_2 plasma and the remainder of

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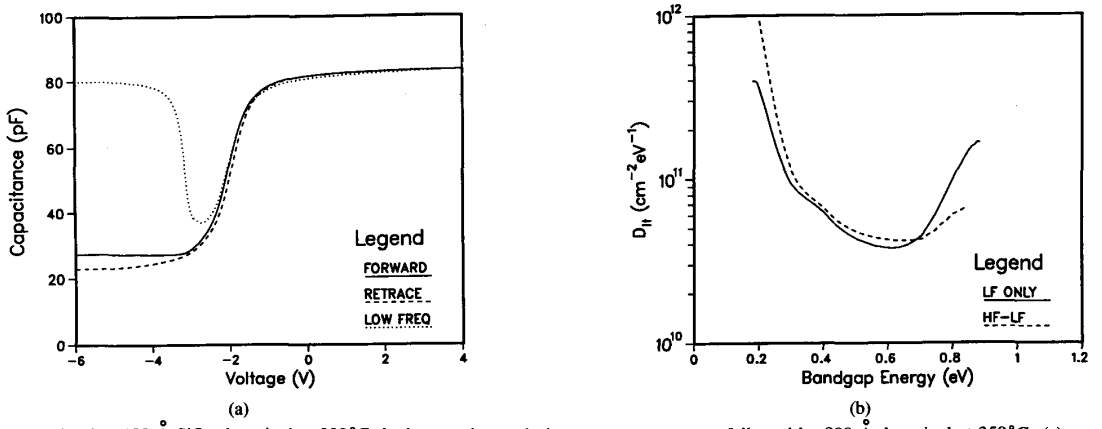

Fig. 1. 100-Å SiO_2 deposited at 300°C, hydrogen plasma during temperature ramp, followed by 900 Å deposited at 350°C: (a) high- and low-frequency *CV* curves and (b) interface trap density.

TABLE I
FILM DEPOSITION PARAMETERS AND MEASURED CHARACTERISTICS

Sample	Temp (Init-Final) °C	Cap Layer Å	Hydrogen	n_f	LF D_{it} 10^{10} $cm^{-2} \cdot eV^{-1}$	HF-LF D_{it} 10^{10} $cm^{-2} \cdot eV^{-1}$	N_{fc} 10^{11} cm^{-2}	E_{BR} 10^6 V/cm
a (n)	300	—	—	1.459	8.8	9.8	2.3	8.7
b (n)	300	—	post-dep	1.461	6.6	6.8	1.8	8.6
c (n)	300-350	250	yes	1.464	4.9	5.4	1.9	8.5
d (n)	250-350	250	yes	1.461	7.1	7.1	2.2	8.6
e (n)	300-350	100	yes	1.465	3.4	4.0	2.9	9.1
f (n)	300-350	250	unexcited	1.464	3.2	5.4	4.6	8.9
g (n)	300-300	250	yes	1.467	4.3	4.7	1.4	8.8
a (p)	300	—	—	1.463	7.4	8.0	2.2	—
b (p)	300	—	post-dep	1.466	5.4	6.7	2.4	—
c (p)	300-350	250	yes	1.467	4.3	5.3	2.7	—
d (p)	250-350	250	yes	1.463	5.5	6.0	2.8	—

the film all done at 300°C (sample g). These also showed good results with midgap trap densities in the low to mid 10^{10} range. Comparing this with sample b, the post-treated wafers, shows that interrupting the deposition for sample treatment is better than post-deposition treatment, due to more effective low-temperature diffusion through a thinner film. Table I lists the deposition conditions of each sample and summarizes the D_{it} data, along with the fixed charge densities N_{fc}. There is little correlation between the fixed charge densities and the interface trap minima.

The breakdown field on n-type wafers, also shown in Table I, was approximately 8.7×10^6 V/cm, which is quite good for plasma-deposited films. There was no temperature dependence of breakdown field, indicating good overall dielectric quality of these particular films. The n-type wafers were also subjected to bias-temperature testing where they were first heated under a bias of −5 V at 200°C for 5 min. The flat-band voltage V_{fb} shifted by 0.1 V in the negative direction, indicating slight bias temperature instabilities. The wafers were reheated for 5 min at 200°C, but this time under a bias of +5 V. V_{fb} moved 1 V in the negative direction, corresponding to a mobile ion charge density of 2×10^{11} cm^{-2}.

In conclusion, it has been shown that interrupting the deposition for *in-situ* sample treatment can be used to lower the interface trap density. Several variations were examined and it was seen that a thin cap layer is best, along with higher initial temperature. A variety of hydrogen treatments are shown to effectively reduce the trap density from that of a standard one-temperature deposition. The midgap trap densities obtained are among the best achieved with a direct PECVD system.

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