

Ilya Wagner

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RESEARCH STATEMENT

My primary research interest is in verification of digital hardware. In particular, I am very passionate about guaranteeing functional correctness of microprocessors and microcontrollers. In my research I developed a comprehensive solution for validation of modern multi-core processors that encompasses all phases of the life-cycle of these devices. The solution leverages machine-learning techniques to self-tune test generation and to discover corner case errors in architectural and micro-architectural processor designs. Furthermore, since some bugs can still escape the verification process, this technique enables efficient patching of microprocessors even after they are deployed in the field. In addition to verification, I am also interested in trusted hardware design and approaches to ensure functional correctness and security of commercial processors even in presence of escaped errors.

SUMMARY OF ACCOMPLISHMENTS

Research: Published several research papers on the subjects of microprocessor verification, logic design and hardware security in top international journals and conferences, such as Design Automation Conference, Design Automation & Test in Europe, IEEE Transactions on Computer-Aided Design, etc. Received Best Paper Award at the International Conference on Computer Design, 2008. Inventor on two patent applications in the field of processor verification and logic design. Department nominee for the University of Michigan Distinguished Dissertation Award (final decision pending).

Teaching: Graduate student instructor for EECS 370, Introduction to Computer Organization. EECS 370 is one of the largest undergraduate courses in the department (~130 students) and covers ALU design, pipelines, caches and other computer architecture topics. Led discussion sessions and office hours, supervised course projects and delivered several lectures. Conducted guest lectures in EECS 578 – a graduate-level digital hardware verification course. Tutored undergraduate students on programming and mathematics. Organized the work of the Michigan Mars Rover Student Project, a multi-disciplinary volunteer student team for research in the field of space exploration.

EDUCATION

September 2004 – December 2008 Department of Electrical Engineering and Computer Science, College of Engineering, University of Michigan

Degree: Ph.D. in Computer Science & Engineering

Advisor: Prof. Valeria Bertacco (valeria@umich.edu),

Dissertation title: An Effective Verification Solution for Modern Microprocessors

Abstract: Over the past four decades microprocessors have come to be a vital and inseparable part of the modern lifestyle. However, due to the complexity of these circuits, they often reach the consumer market insufficiently verified and containing subtle errors. In my work I develop a

novel verification framework targeting specifically today's complex microprocessors and spanning all phases of the processor life-cycle, from pre-silicon verification to post-silicon validation, to in-the-field hardware patching.

September 2004 – May 2006 Department of Electrical Engineering and Computer Science, College of Engineering, University of Michigan

Degree: M.S.E. in Computer Science & Engineering, Summa Cum Laude
GPA: 8.41/9.00 [A+=9.0, A=8.0, A-=7.0]

August 2002 – May 2004 Department of Electrical Engineering and Computer Science, College of Engineering, University of Michigan

Degree: B.S.E. in Computer Engineering, Summa Cum Laude
GPA: 3.96/4.00 [A+=4.0, A=4.0, A-=3.7]

July 2000 – Aug. 2002 Department of Computer and Electrical Engineering, College of Engineering, University of Michigan-Dearborn

Major: Computer Engineering and Engineering Mathematics
GPA: 4.00/4.00 [A+=4.0, A=4.0, A-=3.7]

PROFESSIONAL EXPERIENCE

December 2008 – Present **Post-doctoral Researcher**
Department of CSE, University of Michigan, Ann Arbor, MI

Supervisor: Valeria Bertacco

- Researched approaches for post-silicon functional validation of multi-core processors
- Researched techniques for trusted processor design and reliable hardware

June 2004 – December 2008 **Graduate Student Research Assistant**
Department of CSE, University of Michigan, Ann Arbor, MI

Advisor: Valeria Bertacco

- Researched approaches to self-guiding pre-silicon hardware verification systems
- Created a random-directed test generator system for DLX and Alpha processors in Verilog, VERA and C/C++ languages.
- Developed a processor bug test suit for benchmarking of verification approaches (<http://bug.eecs.umich.edu>)
- Researched high-speed post-silicon validation techniques for modern processors
- Researched reliable hardware and field repairable control logic for microprocessors

June 2007 – September 2007 **Graduate Technical Intern**
Intel Corporation Validation Research Lab, Jones Farms Campus, Hillsboro, OR

Supervisor: Brian A. Moore

- Worked within a group of 30 designers and validation engineers in three countries (USA, Germany, India) on Rock Creek validation environment and methodologies

- Investigated approaches to tera-scale multi-core chip validation
- Worked on system-level validation of a multi-core chip prototype
- Developed system-level test plans, assembly and SystemVerilog tests and assertions, bug tracking tools, and system-level debugging utilities for chip prototype

June 2003 – May 2007

Team member/ President (2005-2006)

Michigan Mars Rover Student Project (www.umrover.org), Ann Arbor, MI

- Coordinated work of a group of approximately 20 graduate and undergraduate students.
- Co-authored a white paper submitted to NASA in 2004 titled “Surface Mobility Technology Development: Pressurized Mars Rovers”
- Co-authored research on “Universal Chassis for Modular Ground Vehicles” (2nd place in NASA/USRA RASC-AL Forum 2005)
- Participated in projects concerning rover radiation shielding, mobility system evaluation, sample collection system evaluation and airlock design

May 2001 – June 2003

Web Developer and Lab Assistant

Department of ECE, University of Michigan, Dearborn

- Developed Flash applets for CD-ROM and web-page for a freshmen engineering course
- Created interactive tutorials covering Microsoft Windows GUI, Matlab and C++ programming and basics of mechanical engineering

PUBLICATIONS

Ilya Wagner and Valeria Bertacco. “Caspar: Hardware Patching for Multi-core Processors”. IEEE/EDAA Design, Automation and Test in Europe, Nice, France, April 2009.

Andrew DeOrio, Ilya Wagner and Valeria Bertacco. “Dacota: Post-silicon validation of the memory subsystem in multi-core designs”. IEEE International Symposium on High Performance Computer Architecture, Raleigh, North Carolina, February 2009.

Joseph Greathouse, Ilya Wagner, David Ramos, Gautam Bhatnagar, Todd Austin, Valeria Bertacco and Seth Pettie. “Testudo: Heavyweight Security Analysis via Statistical Sampling”. IEEE/ACM International Symposium on Microarchitecture, Lake Como, Italy, November 2008.

Ilya Wagner and Valeria Bertacco. “Reversi: Post-Silicon Validation System for Modern Microprocessors”. **Best paper award.** IEEE International Conference on Computer Design, Lake Tahoe, California, October 2008.

Ilya Wagner and Valeria Bertacco. “MCjammer: Adaptive Verification for Multi-core Designs”. IEEE/EDAA Design, Automation and Test in Europe, Munich, Germany, March 2008.

Ilya Wagner, Valeria Bertacco, Todd Austin. “Using Field-Repairable Control Logic to Correct Design Errors in Microprocessors”. IEEE Transactions on Computer-Aided Design, February 2008

Kai-Hui Chang, Ilya Wagner, Valeria Bertacco, Igor Markov, “Automatic Error Diagnosis and Correction for RTL Designs”. IEEE High Level Design Validation and Test Workshop, Irvine, California, November 2007.

Ilya Wagner, Valeria Bertacco. “MCjammer: An Adaptive Verification Tool for Multi-core and Multi-processor Designs”. IEEE/SIGDA International Workshop on Logic and Synthesis, San Diego, California, May 2007.

Kai-Hui Chang, Ilya Wagner, Valeria Bertacco, Igor Markov. “Automatic Error Diagnosis and Correction for RTL Designs”. IEEE/SIGDA International Workshop on Logic and Synthesis, San Diego, California, May 2007.

Ilya Wagner, Valeria Bertacco, Todd Austin. “Microprocessor Verification via Feedback-Adjusted Markov Models”. IEEE Transactions on Computer-Aided Design, June 2007

Ilya Wagner, Valeria Bertacco. “Engineering Trust with Semantic Guardians”. IEEE/EDAA Design, Automation and Test in Europe, Nice, France, April 2007

Ilya Wagner, Valeria Bertacco, Todd Austin. “Shielding Against Design Flaws with Field Repairable Control Logic”, IEEE/ACM Design Automation Conference, San Francisco, California, July 2006.

Ilya Wagner, Valeria Bertacco, Todd Austin. “Depth-Driven Verification of Simultaneous Interfaces”. IEEE Asian-South Pacific Design Automation Conference, Yokohama, Japan, January 2006.

Ilya Wagner, Valeria Bertacco, Todd Austin. “StressTest: An Automatic Approach to Test Generation Via Activity Monitors”, IEEE/ACM Design Automation Conference. Anaheim, California, June 2005.

Halil Hamut, Christine Kryscio, Kristen Montz, Eric Nytko, Anna Paulson, Jarrod Rivotuso, Chad Rowland, Frantisek Sobolic, Matthew Van Kirk, Ilya Wagner. “Universal Chassis for Modular Ground Vehicles”. NASA/USRA Revolutionary Aerospace Systems Concepts-Academic Linkage Forum (RASC-AL), Coco Beach, Florida, May 2005.

Chad Rowland, Anna Paulson, Ilya Wagner, William Green, James Beyer. “Surface Mobility Technology Development: Pressurized Mars Rovers,” Technical report. University of Michigan, 2004.

Jim Beyer, Matt Van Kirk, Tom Lau, Eric Nytko, Christian Passow, Fritz Passow, Boyang Tang, Ilya Wagner. “Sampling Systems Evaluation Software”. Technical report. University of Michigan 2004.

Anton VanderWyst, Ilya Wagner, Reza Farsain. “Olympus Radiation Shielding”. Technical report. University of Michigan 2003.

PATENT APPLICATIONS

Ilya Wagner, Valeria Bertacco, Todd Austin. “Field-Repairable Control Logic”. Application Serial No. 60/951,564 Filed: July 24, 2007.

Kai-Hui Chang, Ilya Wagner, Valeria Bertacco, Igor Markov. “Automatic Error Diagnosis and Correction for RTL Designs”. Application Serial No. 60/940,290 Filed: May 24, 2007.

INVITED PRESENTATIONS

“Engineering Trust with Semantic Guardians”. Plenary presentation, Gigascale Systems Research Center Annual Symposium, San Jose, California, September 2008.

“Engineering Trust with Semantic Guardians”. Workshop on Post-Silicon Validation collocated with IEEE/ACM Design Automation Conference, Anaheim, California, June 2008.

“Buggy Chip? No problem!”. Prospective student welcome day, Department of Computer Science and Engineering, University of Michigan, Ann Arbor, Michigan, March 2008.

“Shielding Against Design Flaws with Field-Repairable Control Logic”. Formal verification group meeting, Jones Farms campus, Intel Corporation, Hillsboro, Oregon, August 2007.

“StressTest: An Automatic Approach to Test Generation Via Activity Monitors”. Student presentation, Gigascale Systems Research Center Annual Symposium, Anaheim, California, June 2005.

TEACHING EXPERIENCE

March 2008

Guest Lecturer

EECS 578 Computer-Aided Design Verification of Digital Systems

- EECS 578 is graduate-level course in hardware verification, usually attended by approximately 25 students.
- The course covers several topics about functional verification of combinational and sequential circuits, different classes and sources of design errors, functional and temporal modeling of digital systems, simulation and formal verification techniques.
- Presented research on processor control logic patching and trusted hardware design

January 2006 – May 2006

Graduate Student Instructor/Guest Lecturer

EECS 370 Introduction to Computer Organization

Department of EECS, University of Michigan-Ann Arbor

- EECS 370 is one of the largest junior-level undergraduate courses in the EECS department (130+ students).
- The course covers basic concepts of computer organization and hardware. Throughout the course students are asked to develop datapath and control for multiple processor designs. The course also overviews pipelining, caches, virtual memory, input/output.

- Conducted two hourly discussions sessions per week (approximately 30 students in each) and office hours (3-5 hrs week) on overview of theoretical course material, homework, and course projects.
- Maintained four course projects, including website, on-line discussion board and auto-grader system
- Wrote and graded midterms and final exam questions

September 2002 – June 2003 Web Developer and Lab Assistant.

Department of ECE, University of Michigan-Dearborn

- Organized work of several teams of freshmen developing LEGO “Mindstorms” robots and related control software
- Conducted tutoring sessions with students covering HTML, Matlab and C++ programming

May 2001 – June 2002 Mathematica Lab Assistant/Tutor

Department of Mathematics, College of Arts, Sciences, and Letters,
University of Michigan-Dearborn

- Lab instructor for Calculus and Differential Equations courses
- Tutored students on Mathematica software and basics of MacOS X

SERVICE AND OUTREACH

Reviewer for IEEE Transactions on Computer Aided Design (2007-present), Design Automation Conference (2005-present), Design Automation and Test in Europe Conference (2005-present), Formal Methods in Computer Aided Design Conference (2006-present), International Conference on Computer Aided Design (2006-present), International Workshop on Logic and Synthesis (2007-present).

Book proposal reviews for John Wiley & Sons (2007), Taylor and Francis Group (2007)

Organized multiple outreach events for the Michigan Mars Rover Team, educating the general public about Mars exploration. Organized and supervised a semester-long design contest for high school students (2005-2007).

Conducted one-on-one meeting and panel talks for prospective graduate students of the CSE Department (2006-2008).

PROFESSIONAL AND HONOR SOCIETIES

The Order of The Engineer member

IEEE Student member

Tau Beta Pi member

Pi Mu Epsilon National Mathematics Honor Society member (chapter secretary 2002)

HONORS

International Conference on Computer Design Best Paper Award (2008)
Computer Science and Engineering Honors Competition First Place Award (2007)
Michigan Space Grant Consortium Fellowship (2005)
Mildred Weed Goodrich Fellow (2004)
Recognized as Senior Scholar by EECS Department, University of Michigan (2004)
National Dean's List (2000 - 2004)
University Honors (2002 - 2004)
University of Michigan James B. Angell Scholar (2003, 2004)
College of Engineering Dean's List (2002 - 2004)
O'Connor Transfer Scholarship (2002)
Chancellor's Scholarship (2000 - 2001)
Michigan Competitive Scholarship (2000)

U.S. CITIZEN