PLANAR GaAs DIODES FOR THz FREQUENCY MIXING APPLICATIONS

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I. Introduction

For many scientific applications in the terahertz frequency range, heterodyne reception is the only technique which exhibits the necessary combination of high spectral resolution, large instantaneous bandwidth and excellent sensitivity. A key component in these receivers is the non-linear resistive mixer element. In general, the mixer element should have high intrinsic speed, the sharpest possible non-linearity, low parasitic element values, low intrinsic noise and impedance levels which can be easily matched to the RF circuit. However, no single device exhibits all of these properties and some tradeoffs are necessary [1].

The GaAs Schottky barrier diode is the most widely used mixer element at submillimeter wavelengths. These diodes are commonly used in the temperature range from 300 K to 10 K and have demonstrated excellent performance from below 100 GHz to over 3 THz [2,3]. The closest competitor for Schottky diodes is the SIS element which has demonstrated record sensitivities at millimeter and long-submillimeter wavelengths [4,5,6]. However, SIS devices are not yet competitive at terahertz frequencies and present superconductor mixer elements require cryogenic cooling which increases the cost and size of the receiver system.

Schottky barrier diodes for terahertz applications are typically fabricated as a micron to sub-micron circular anode metallization on GaAs which is contacted with a sharp wire (whisker). This structure has the benefits of the simplicity of the fabrication of the diode chip, the minimal shunt capacitance of the whisker contact and the ability of the whisker wire to couple energy to the diode. However, whisker-contacted diodes are costly to assemble and difficult to qualify for space applications. Also, complex receiver systems which require many diodes are difficult to assemble [7,8].

The objective of this paper is to discuss the advantages of planar Schottky diodes for high frequency receiver applications and to summarize the problems of advancing the planar technology to the terahertz frequency range. Section II will discuss the structure, fabrication and performance of state-of-the-art planar Schottky diodes. In Section III the problems of designing and fabricating planar diodes for terahertz frequency operation are discussed along with a number of viable solutions. Section IV summarizes the need for futher research and cooperation between diode designers and RF engineers.

II. Planar Mixer Diodes

Planar Schottky barrier diodes have been developed by numerous laboratories over the past ten years [9,10,11,12]. This effort has resulted in many benefits. Not only has the troublesome and somewhat fragile whisker contact been eliminated, but receivers which require two or more individual diode chips, such as balanced mixers, are much easier to assemble. Single chips with two or more diodes in a fixed configuration, such as an antiparallel diode pair, are easy to fabricate and the extension of the diode contact pads to form a planar antenna has been demonstrated. Future work should allow additional receiver components such as filters, oscillators and amplifiers to be integrated with the diode.

The surface channel planar diode, shown in Figs. 1 and 2, has been developed for use at both millimeter and submillimeter wavelengths [9,13]. The chip substrate is semi-insulating GaAs. The epitaxial GaAs structure consists of a thin n-type layer on top of a thick, heavily doped n+ buffer layer. The anode is formed on the n-type GaAs with SiO_2 providing passivation and insulation. An ohmic cathode pad is formed on one end of the chip in close proximity to the anode. The anode is connected to a bonding pad by means of a narrow finger. A trench is formed beneath the finger and completely across the width of the chip to isolate the anode contact pad from the cathode. The isolation trench can be etched deeply into the semi-insulating substrate and the wall of this trench can be positioned very close to the anode. These two features combine with the inherent air-bridge to reduce the shunt capacitance between the contact pads and the shunt capacitance from the contact finger to the conductive GaAs of the cathode. This structure produces lower shunt capacitance than other designs which rely on mesa or proton isolation.

The major fabrication steps of the surface channel structure are illustrated in Fig. 3. Starting with the GaAs wafer (1), a layer of silicon dioxide is deposited using chemical vapor deposition from silane and oxygen (2). The ohmic contact region is patterned, the SiO_2 and n-GaAs are removed and the ohmic contact metallization is deposited and alloyed (3). An opening for the anode is patterned and etched into the SiO_2, leaving a thin layer of oxide to protect the GaAs until the anode metallization can be deposited. The remaining oxide in the anode well is removed with buffered hydrofluoric acid and platinum and gold are electroplated to form the diode and fill the oxide well (4). A thin layer of chromium and gold is deposited over the entire wafer by sputtering. Photoresist is applied and patterned and gold is plated into the opening to form the anode contact pad and finger. The resist is removed and the sputter deposited gold and chromium surrounding the anode contact pad and finger are

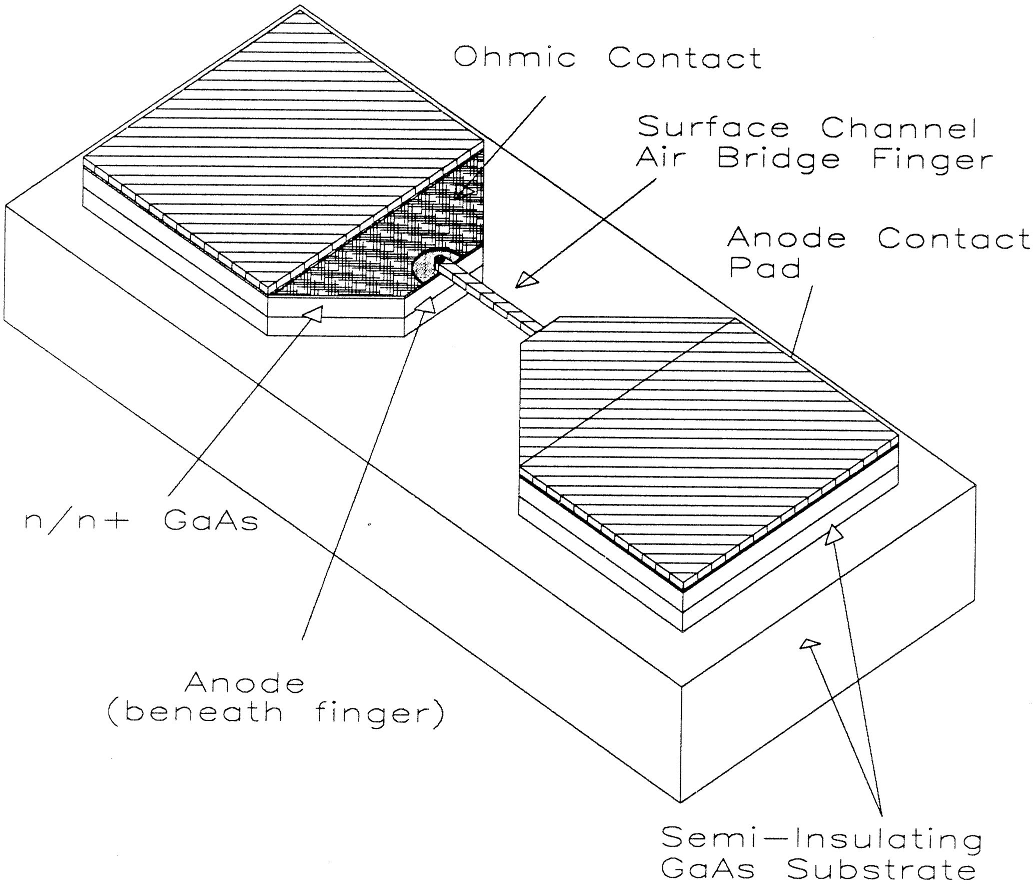

Figure 1. *Surface Channel Planar Diode Structure*

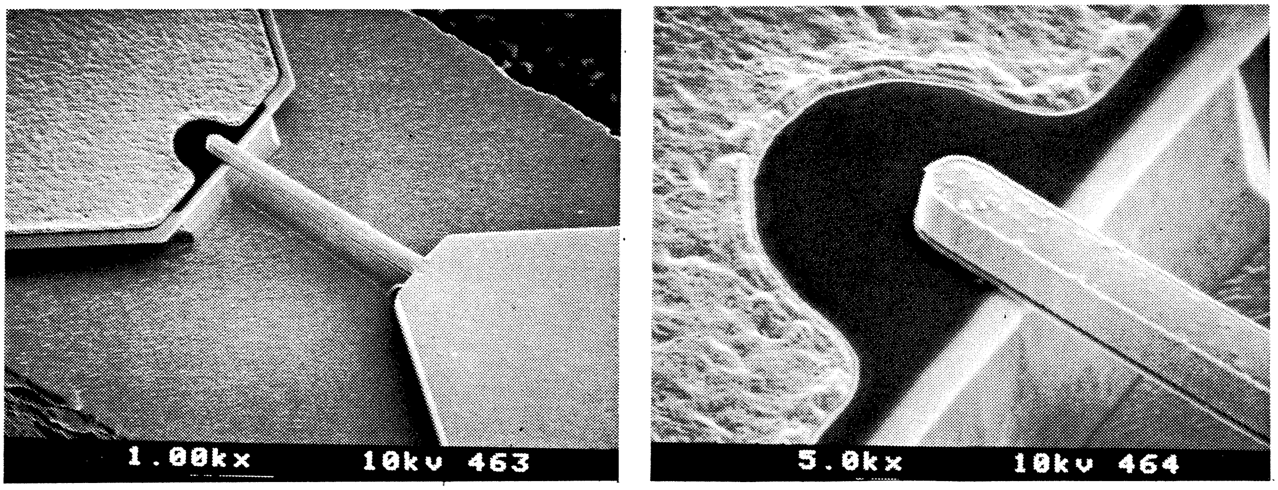

Figure 2. *SEM Photographs of a Surface Channel Planar Diode*

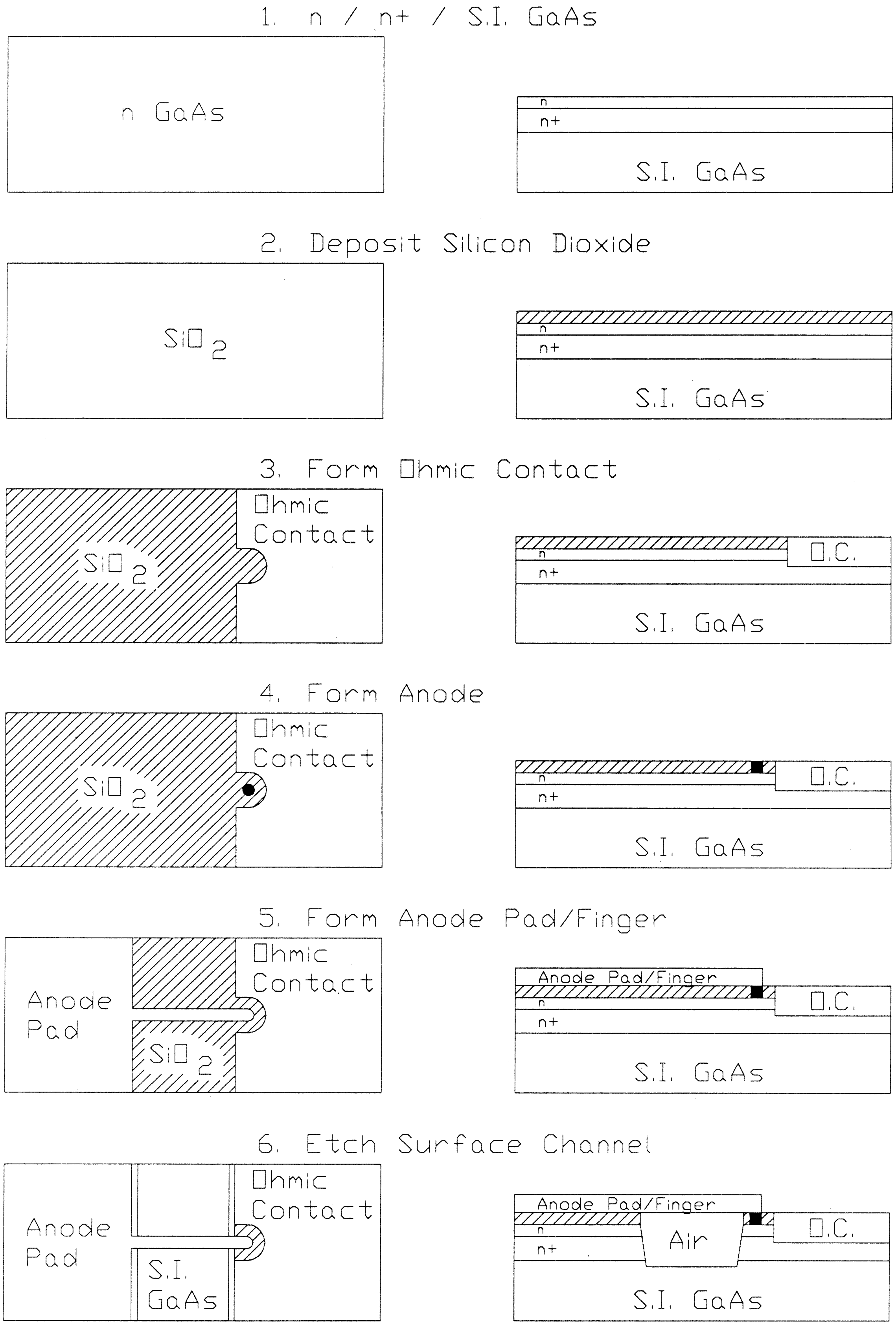

Figure 3. *Surface Channel Diode Fabrication Sequence*

etched away (5). Finally, the surface channel is patterned with photoresist and the SiO_2 and GaAs are etched to form the isolating trench (6).

This fabrication sequence offers several advantages compared to other configurations: (1) expensive and troublesome proton bombardment is not required, (2) planarization is unnecessary, and (3) the wafer surface is nearly flat for the critical steps of anode formation and anode-to-finger alignment.

SEM photographs of two surface channel diode chips are shown in Figs. 4 and 5. The SC2T1 single anode chip is about 125 x 375 x 75 microns. This device has a total capacitance of about 14 fF, zero-bias junction capacitance of 2.5 fF and series resistance of 12-15 Ω. This gives a figure-of-merit cutoff frequency of 4.2 THz for the junction. The SC2T1 has been tested in a room temperature mixer at 345 GHz with a mixer noise temperature of 1,370 K (DSB) and a conversion loss of 9.5 dB (SSB) [14]. This is comparable to the best whisker-contacted diode results. The SC1T4 chip is an antiparallel diode pair for subharmonic pumping. It is only 80 x 180 x 50 microns. These chips have a

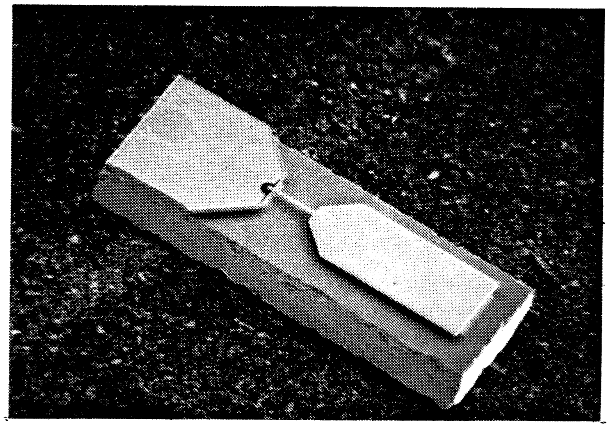

Figure 4. *SC2T1 Planar Diode Chip*

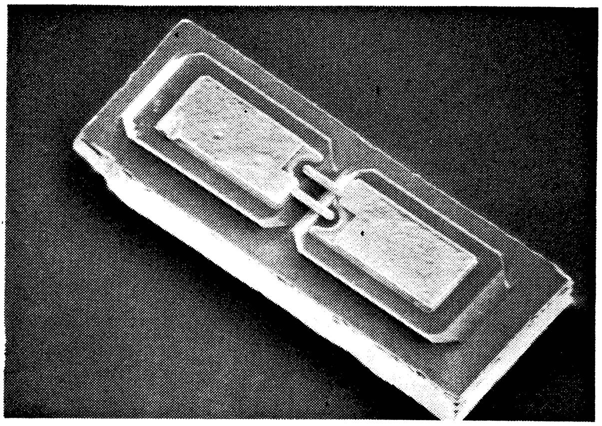

Figure 5. *SC1T4 Planar Antiparallel Diode Pair*

total capacitance of about 16 fF, zero-bias junction capacitance of 3 fF per anode and series resistance of 7-9 Ω. This diode has been successfully used in a room temperature mixer at 205 GHz with a mixer noise temperature of 800 K (DSB) and a conversion loss of 4.4 dB (DSB) using an LO of approximately 100 GHz [15]. This result is better than has been previously reported for antiparallel subharmonic mixers of either planar or whisker-contacted design.

A dual anode planar diode chip for balanced mixer operation is shown in Fig. 6. This chip was developed in collaboration with Aerojet General, Electronic Systems Division under the direction of Robert Haas. This configuration allows individual DC bias of each diode. This device has excellent DC electrical characteristics and is being evaluated in a 100 GHz mixer.

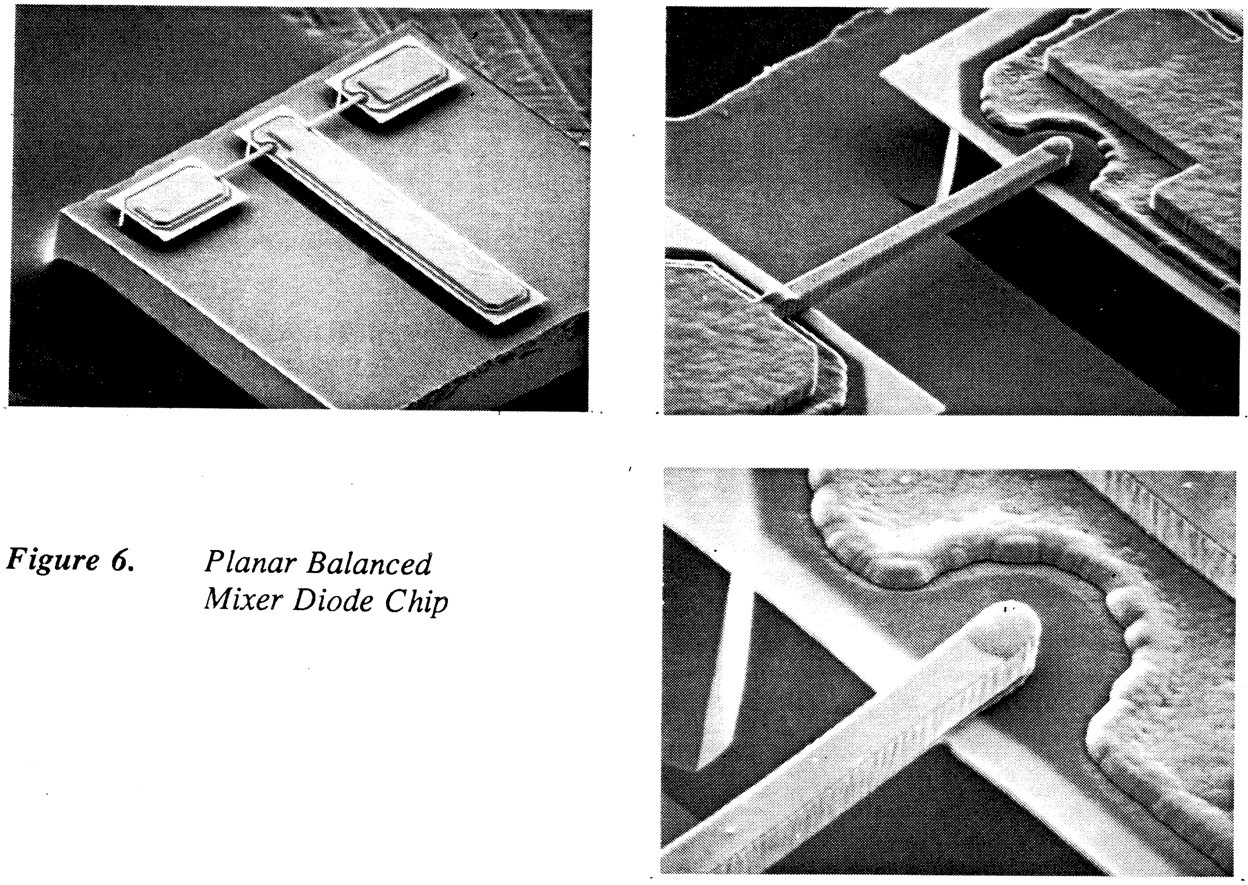

Figure 6. *Planar Balanced Mixer Diode Chip*

III. Planar Diodes for THz Frequency Applications

The surface channel diode structure must be optimized for terahertz operation. These improvements reflect the fundamental need to reduce the R_sC_{j0} product, minimize shunt capacitance, and to efficiently couple energy into the diode. These optimization issues are addressed in the following subsections:

A. *Reduction of Anode Diameter*

Theory and experimental results with whisker-contacted diodes have shown that very small anodes combined with higher active layer doping are necessary for good performance in the THz range [16]. Whisker-contacted diode chips have been fabricated at UVa with anodes as small as 0.25 microns using direct write electron beam lithography and reactive ion etching [17]. Planar diodes have been fabricated at UVa with 0.5 micron diameter anodes using optical lithography and reactive ion etching. We are also investigating a novel Electroplate Window Shrink (EWS) technique. In this method, circular openings are etched through a thin (0.1 micron) metal layer which overlies silicon dioxide, using UV lithography and wet or dry etch methods. Metal is then electroplated onto this thin conductive layer. Since the plating proceeds laterally as well as vertically, the diameter of the openings is reduced. These reduced-diameter windows are then used as a non-eroding mask to RIE etch the silicon dioxide. Etched wells less than 0.2 microns in diameter have been formed in this manner.

It should be realized that the main issue is not just the fundamental task of forming small anode wells, but also the problems of uniformity and control of anode size. The UVa anode formation process depends on leaving a thin layer of SiO_2 of known thickness in the bottom of the anode wells after RIE. This protective layer is removed by etching with buffered hydofluoric acid just prior to anode formation. Underetching of this remaining oxide results in open circuits or high resistance. Overetching can result in high C_{j0} and in some cases, excessive diode noise [18]. Unlike whisker-contacted diode chips which can be etched and plated on a chip-by-chip basis, all planar diode anodes on a wafer are formed simultaneously. This obviously places very tight limits on dielectric thickness, thickness uniformity and etch rate calibration.

For these reasons, it would be most helpful to have a very thin RIE etch stop layer to protect the GaAs. This etch stop layer would relax the requirements for oxide thickness and uniformity and allow reasonable overetching during RIE without the risk of damage or contamination of the junction area. Schemes which utilize mutiple layers of different dielectrics could, in principle, satisfy this need. A very thin layer (100-500 Å) of silicon dioxide could first be deposited onto the GaAs. This would be followed with a thicker layer of another dielectric, such as silicon nitride, polyimide or boron-doped silicon dioxide. This thick layer could be patterned and selectively etched (possibly with a dielectric or metal mask) so that the underlying thin layer of oxide acts as an RIE etch stop. Research in this important fabrication area will provide improved control of anode diameter and the reliable production of sub-half micron planar diode anodes.

B. Optimization of Chip Geometry

The dimensions and layout of planar diode chips must be optimized for terahertz frequency applications. The volume of the chip must be reduced to minimize the field disturbing effect of high dielectric constant GaAs and to allow the devices to fit into the smaller waveguides which are required at higher frequencies. The geometry of the planar diode must be improved to minimize shunt capacitance.

Shunt capacitance in the planar diode structure can be separated into two primary components: capacitance from the anode contact finger and pad-to-pad capacitance through the high dielectric constant substrate. Finger capacitance will be reduced by several means. The width of the contact finger can be reduced from the current value of about 2.5 microns to 1 micron. Improved mask design, alignment and surface channel etch control will allow the surface channel wall to be etched as close as possible to the anode. A thick (1 micron) dielectric, perhaps a polyimide, would further reduce finger capacitance.

Pad-to-pad shunt capacitance can be reduced by decreasing pad area, increasing pad separation, increasing the surface channel depth and/or reducing substrate thickness. Our present technology produces chips which are 50 microns thick with pads which are 30 x 60 microns and a surface channel depth of 10 microns. For the lowest possible pad-to-pad capacitance, the GaAs substrate can be removed. This has been demonstrated in a procedure that replaces the GaAs with quartz, as shown in Fig. 7 [19]. The quartz substrate can be permanent or it can be removed once the chip is bonded to a circuit as shown in Fig. 8.

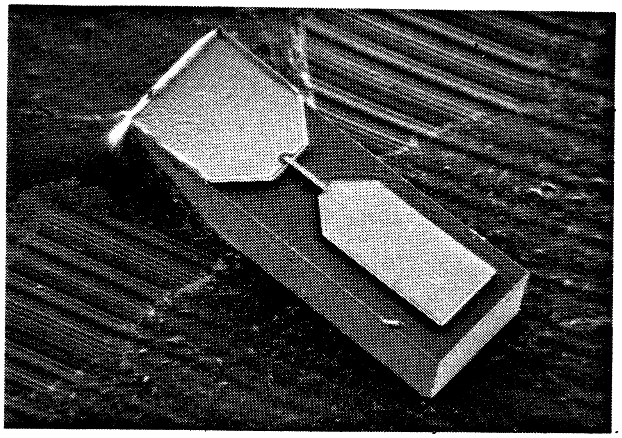

Figure 7. *Surface Channel Diode Chip with Quartz Substrate*

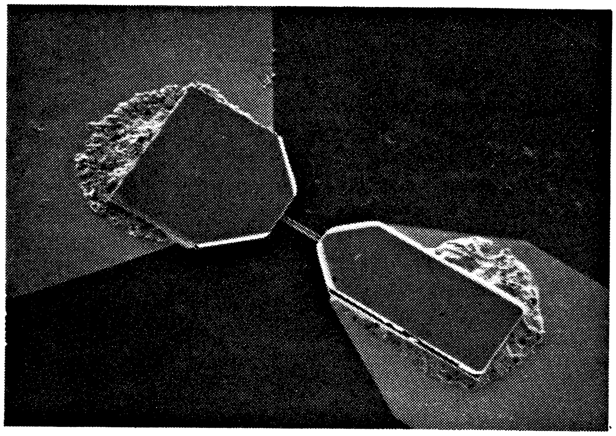

Figure 8. *Surface Channel Diode Chip with Quartz Substrate Removed After Bonding*

The effect of finger length on planar diode performance is an important issue, particularly for waveguide mixers. Longer fingers result in reduced pad-to-pad capacitance but increased finger inductance. A new mask set has been fabricated which will provide small area, antiparallel planar diodes with finger lengths from 10 microns to 50 microns in 10 micron steps on the same wafer. This mask was designed in collaboration with Peter Seigel of JPL and the devices will be RF tested at JPL in a waveguide mixer at frequencies as high as 600 GHz.

Very short contact fingers are required in integrated antenna designs. Surface channel formation is very difficult when the contact finger is under 10 microns in length. Research is underway to characterize a combination of chlorine-based reactive ion etching and wet chemical etching processes to form the surface channel isolation trench with these short contact fingers. The new mask sets for both the small area antiparallel chips and the log periodic antenna designs include levels for this new process.

C. Minimization of Ohmic Contact Resistance

Ohmic contact resistance contributes to diode series resistance and thus reduces cutoff frequency. As contact pad dimensions shrink, ohmic contact resistance increases. This is of particular importance in the case of integrated antenna devices where the pad geometry is dictated by the antenna design. Specific contact resistance can be improved by using a very highly doped buffer layer and through the use of a more advanced ohmic contact technology. For example, ohmic contacts to an n^{++} InGaAs layer are reported to have specific contact resistivity as low as 10^{-7} Ω-cm^2, a factor of 50 to 100 better than our present ohmic contacts.

This would be most beneficial for planar THz antenna structures which require small pad geometries near the anode.

D. *Integration of Antenna Structures*

The problem of efficient energy coupling to the planar diode is exacerbated at higher frequencies where the wavelength begins to approach the size of the chip. For whisker-contacted diodes, the whisker itself is used as the antenna element and mixers with a long whisker (4λ) positioned parallel to the axis of a corner cube have demonstrated excellent performance at frequencies as high as 4 THz [3].

Another approach for planar diodes is to integrate an antenna, in the form of a bow-tie or log periodic shape onto the chip [20]. The fabrication is straightforward, with the antenna being an extension of the anode and cathode pads and the radiation can be coupled to the antenna through the substrate (GaAs or quartz). An integrated bowtie antenna-diode is shown in Fig. 9. It is 700 x 1000 x 50 microns thick with a 0.5 micron anode and an 8 micron finger length. Preliminary RF testing with unoptimized coupling produced video response of 10 V/W.

Optimization of the integrated antenna will require close interaction between diode designers and RF engineers. As a first step towards this goal, a mask set for the fabrication of log periodic antenna-diodes has been designed in cooperation with Gabriel Rebeiz of the University of Michigan and devices will be fabricated in the near future. With proper diode design and good coupling of energy to the antenna and the diode, it is hoped that RF performance will exceed that of the best whisker-contacted diodes.

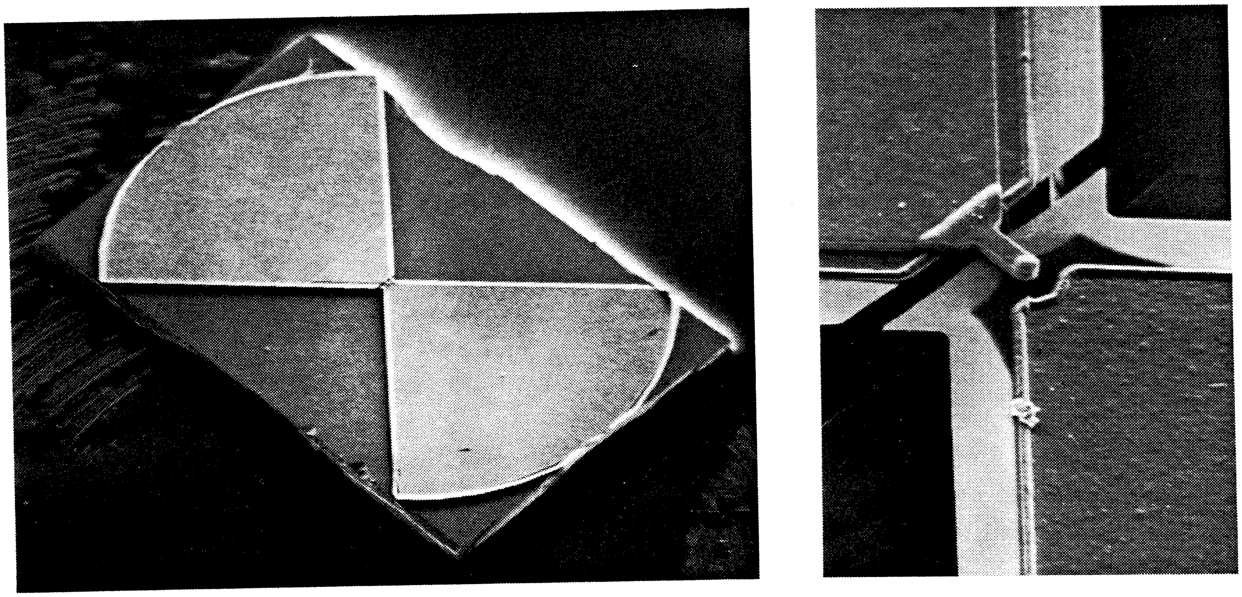

Figure 9. *Integrated Bowtie Antenna-Diode*

IV. Discussion

Development of the planar mixer diode was driven by the need for a rugged device which is inherently simple and easy to assemble in a mixer. However, the tradeoffs for this structural ruggedness and simplicity are a more complex and expensive fabrication procedure, and a more complex chip geometry with larger shunt capacitance. The RF circuit must be redesigned to efficiently couple energy to the diode. In spite of these changes, planar GaAs Schottky barrier diodes have demonstrated performance in the millimeter wavelength range equal to or better than that of the best whisker-contacted diodes.

Successful operation of planar diodes at THz frequencies will require several improvements in the diode chip including reduced anode diameter, improved control of anode diameter, smaller chip dimensions to reduce shunt capacitance, and reduced ohmic contact resistance. These concerns are being addressed through research of novel structures and fabrication methods. Successful application of planar diodes in the THz frequency range will also require optimization of the embedding circuitry and improved methods of coupling energy to the diode. Research is underway to apply novel antenna designs to this problem and to begin to test high performance planar diodes in waveguide assemblies and to test integrated antennas in open structure mixers. The success of this effort will be hastened by very close interaction and cooperation between diode designers and RF engineers.

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