PLANAR GaAs SCHOTTKY DIODE FABRICATION: PROGRESS AND CHALLENGES

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I. Introduction

Schottky barrier diodes for high frequency mixer applications are usually made by forming a honey-comb array of circular metal anodes on n-type GaAs. One of these micron to sub-micron sized anodes is contacted with a sharpened wire (whisker) and a large-area backside ohmic contact completes the device. This structure is relatively simple to fabricate and it benefits from the very low shunt capacitance presented by the whisker. However, production of high quality whisker contacts is technically demanding and multiple diode arrangements are difficult to implement. Also, electrical and mechanical qualification of whisker-contacted diodes for use in space is expensive and time consuming [1,2].

Planar or whiskerless diodes were developed to overcome the problems and limitations of whisker-contacted devices. High quality planar GaAs Schottky barrier diodes from this and other laboratories have demonstrated excellent RF performance at millimeter wavelengths [3,4,5,6]. These devices are replacing whisker-contacted diodes in many applications and some have been qualified for use in space systems. This change is driven by the need to reduce the time required for mixer assembly and qualification and to simplify the fabrication of multiple diode receivers. There are a variety of more advanced mixer designs which incorporate multiple diodes and promise improved performance. Although such designs are virtually impossible to implement with whisker-contacted diodes, they are relatively easy to achieve with planar technology.

The purpose of this paper is to discuss recent diode fabrication progress at the University of Virginia and to explain the major obstacles in fabricating planar diodes for operation at submillimeter wavelengths. In Section II we discuss the structure and fabrication of the surface channel diode and in section III we summarize the latest diode fabrication results. In section IV we examine the major challenges for planar diode fabrication and possible solutions to these problems. Section V presents a new planarization technology which will greatly improve the isolation of planar structures and ultimately lead to lower shunt capacitance and greater freedom in the design of these devices.

II. Planar Diode Structure and Fabrication

Planar Schottky diodes fabricated at the University of Virginia utilize the surface channel structure as illustrated in Fig. 1 [3,7]. The cathode pad is an ohmic contact formed on the highly doped n-type GaAs (n^+ buffer layer). The anode pad may also be an ohmic contact or it may be a non-ohmic metallization on GaAs or on a silicon dioxide layer above the GaAs. A single circular Schottky barrier diode is formed near the ohmic contact pad. The forward electron current path is from the ohmic contact metallization through the n^+ buffer layer to the n-type GaAs below

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the anode. From here, the electrons are emitted into the anode metal, travel along the finger and into the anode contact pad. The semi-insulating substrate and the surface channel ensure that all conduction current passes through the Schottky contact. The parasitic elements are actually more complex than illustrated and, furthermore, they are distributed. The circuit nodes for shunt capacitance are deliberately omitted to emphasize this unknown distribution. This simplified circuit is, however, most useful for discussion of chip design.

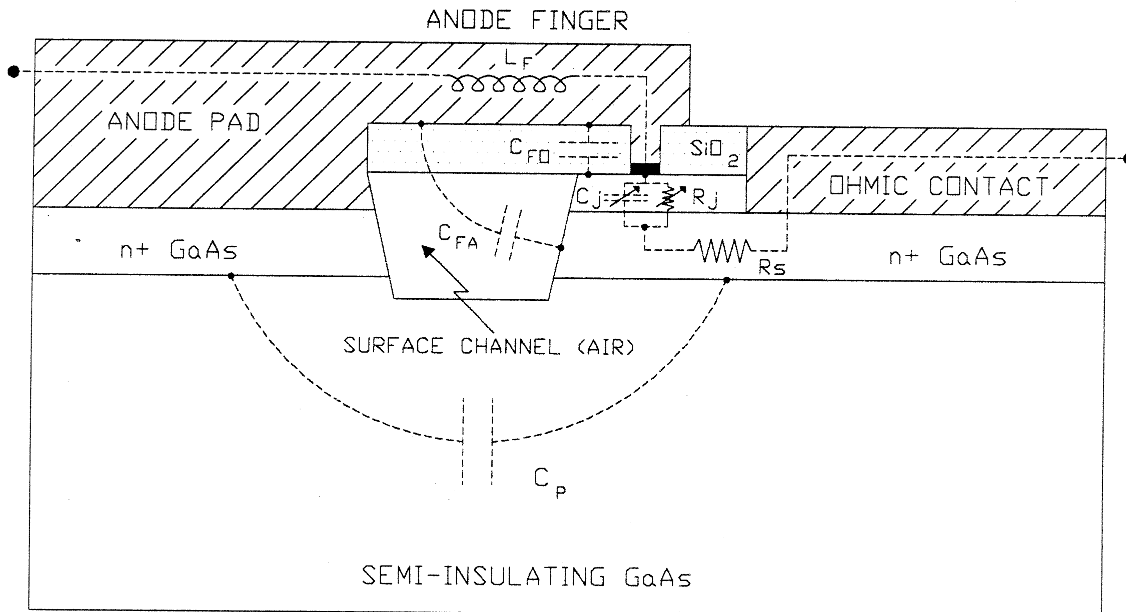

Figure 1. Surface Channel Planar Diode Structure With Major Circuit Elements

Shunt capacitance limits the cutoff frequency and bandwidth of any mixer [8]. Shunt capacitance for the surface channel structure can be divided into three major parts: (1) C_P, pad-to-pad capacitance, primarily through the high dielectric constant GaAs substrate; (2) C_{FO}, the parallel plate capacitance from the portion of the finger which overlies conductive GaAs, with SiO_2 as the dielectric; and (3) C_{FA}, the capacitance from the air-bridged portion of the finger to the cathode. The surface channel geometry produces diode chips with low shunt capacitance compared to either proton bombarded or mesa structures. Large scale models and numerical analysis indicate that pad-to-pad capacitance is reduced by increasing the depth of the trench and by producing trench sidewalls which have vertical or retrograde slope [9, 10]. Also, a contact finger which is surrounded by air for most of its length will exhibit lower parasitic capacitance than one which has high dielectric constant GaAs on one side (proton isolated). Futhermore, surface channel mask design and the fabrication process allow the surface channel (trench) wall to be positioned within one micron of the anode to minimize finger overlay capacitance.

The fabrication sequence of the surface channel planar diode offers additional benefits compared to other diode structures. The ohmic contact, anode and anode contact pad and finger are formed before the isolation trench. The highly planar surface which is available for these critical steps is conducive to high resolution lithography. By orienting the anode contact finger

in the [011] direction and using orientation dependent wet chemical etching, a trench as illustrated in Fig. 2 is formed. Undercut towards the anode is minimal. The bottom surface of the trench is flat with no remnant of the finger. The sidewall of the trench is also flat, even beneath the finger. The trench forms with essentially the same geometry as would be produced without the finger. This surprising result occurs when the channel etch depth and finger length are large compared to the width of the finger. In this case, the orientation dependent nature of the wet etch dominates the process.

Such a perfect trench could not be formed using an isotropic dry etch process of the type suggested by Hur [11]. Isotropic etchants used to undercut the finger require deeper etching and require a much greater initial mask offset from the anode location. A large mask offset limits the minimum length of the finger and causes greater variation in finger overlay capacitance due to inevitable local variation in lateral etch rate.

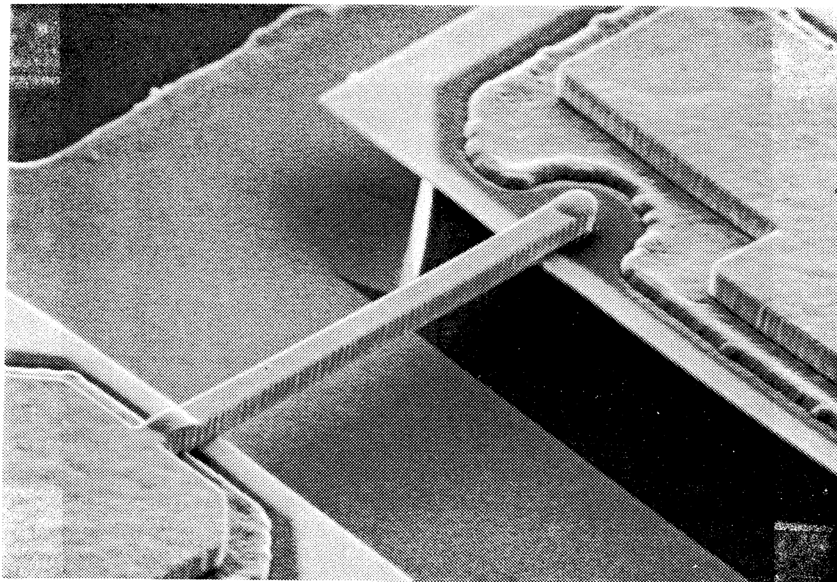

Figure 2. SD2T5 Surface Channel Planar Diode

A variety of planar mixer diodes have been produced at the University of Virginia, including: single anode chips for use as fundamentally pumped mixers, dual anode antiparallel configurations for subharmonically pumped mixers, and separately biasable dual anode chips for balanced mixers [12]. A technology has also been developed to replace the GaAs substrate with quartz for lower pad-to-pad capacitance [13]. Chip dimensions range from approximately 10 x 10 mils to 3 x 8 mils with chip thickness as small as 0.5 mil. All of the devices are intended to be inverted and soldered to the circuit (flip chip mounting).

These devices have been RF tested in both waveguide and quasi-optical mixers by several research groups. A summary of these results are given in Tables I and II.

Table I. Room Temperature Waveguide Mixer Results Using UVa Planar Diodes

Diode Type	Mixer Type	Signal Frequency (GHz)	Mixer Noise Temperature (K SSB)	Conversion Loss (dB SSB)	LO Pwr (mW)	Research Group
SC2R2 Single Anode 5x15x5 mil	Fundamental	94	520	5.3	2.6	Garfield UVa/NRAO [14]
SC1T4 Antiparallel 3x8x2 mil	Subharmonic	205	1590	8.7	5.7	Siegel JPL [15]
SC2T1 Single Anode 5x15x0.5 mil	Fundamental	345	2740	9.5	1.4	Newman UVa/NRAO [16]
2 x SC2R4 Single Anode 5x15x4 mil	Fundamental (Balanced)	74-114 (16 GHz Inst. BW)	5.2 dB Noise Figure (DSB Receiver)		10-20	Haas Aerojet [17]

Table II. Room Temperature Quasi-Optical Mixer Results Using UVa Planar Diodes

Diode Type	Mixer Type	Signal Frequency (GHz)	Mixer Noise Temperature (K DSB)	Conversion Loss (dB DSB)	LO Pwr (mW)	Research Group
SC2T3 Single Anode 5 x 15 x 2 mil	Fundamental Dipole on Membrane Integrated Horn	86 92 106	870 725 830	6.2 5.5 6.2	2.0 to 2.5	Ali-Ahmad U. Mich [18]
SC1T4-S20 Single Anode 3 x 8 x 1.5 mil	Fundamental Dipole on Membrane Integrated Horn	243 249 258 264	1850 1420 1310 1500	8.4 7.3 7.2 7.5	1.0 to 1.5	Ali-Ahmad U. Mich [19]
SR2T1 Antiparallel 5 x 10 x 2 mil (Quartz Substrate)	Subharmonic Log-Periodic Silicon Lens	90 182	1080 1820	6.7 8.5	9	Kormanyos U. Mich [20]

III. Recent Planar Diode Fabrication Progress

State-of-the-art receivers in the terahertz frequency range are currently constructed with a whisker-contacted diode. The RF signal and local oscillator energy are coupled to a long wire antenna in a corner cube assembly. This quasi-optical technique has a coupling efficiency of only about 50% [21].

The surface channel diode has recently been integrated with a monolithic antenna structure to improve energy coupling to the diode and to eliminate the fabrication and reliability problems associated with the corner-cube system. The SA1T2 antenna-diode chip, designed in collaboration with the University of Michigan, is shown in Fig. 3. This chip consists of a log-periodic antenna structure with a single 0.8 micron diameter Schottky diode located near the center. The antenna consists of ohmic contact metallization and 5 microns of highly doped n^+ GaAs. The surface channel follows this antenna pattern and is etched approximately 5 microns into the semi-insulating GaAs substrate. The anode contact finger is approximately 7 microns long and 2.5 microns wide.

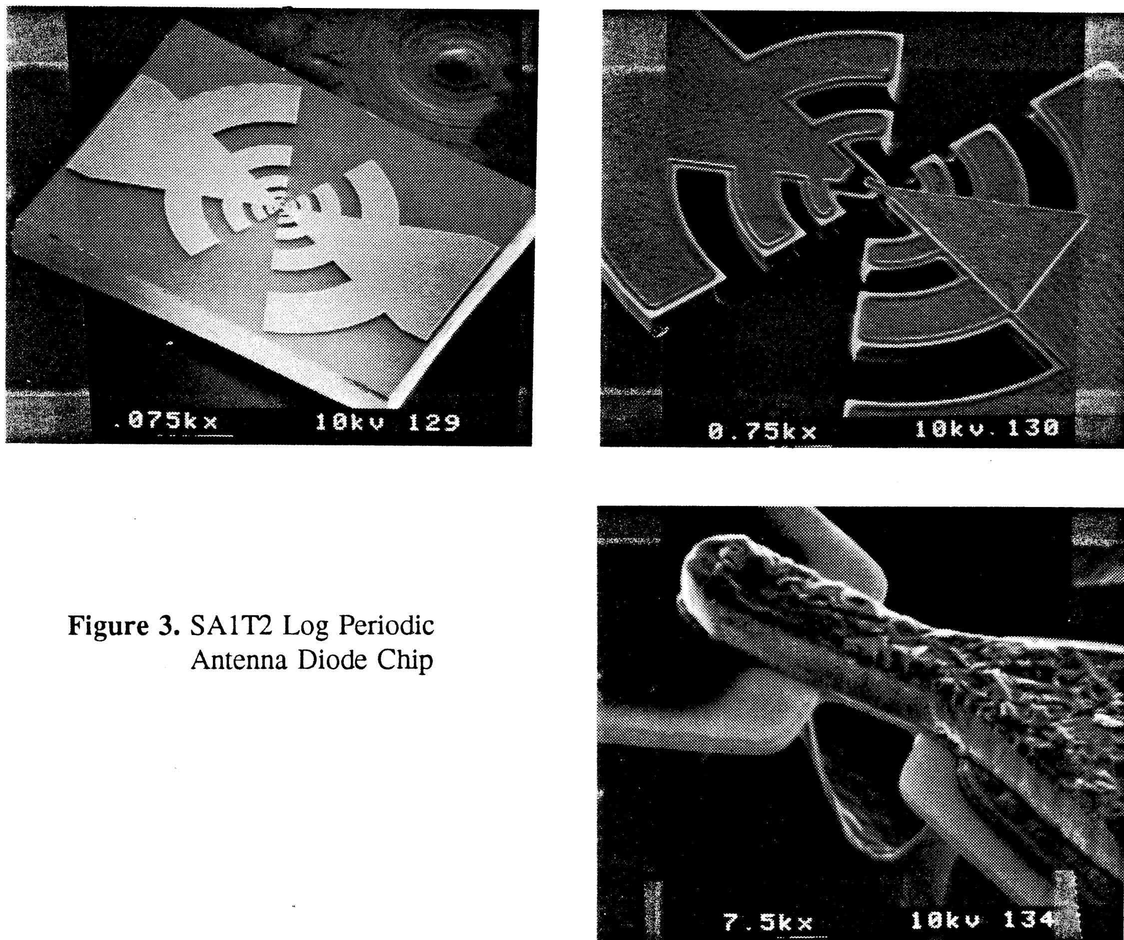

Figure 3. SA1T2 Log Periodic Antenna Diode Chip

Wet chemical etching of the surface channel was not attempted in fabricating the log-periodic antenna diode because of the short contact finger. Instead, a combination of chlorine-based reactive ion etching (RIE) and wet chemical etching was utilized. RIE was first used to vertically etch approximately 8 microns into the GaAs. This left a 2 micron thick wall of GaAs directly beneath the finger. This conductive material was removed by wet chemical etching which also moved the wall of the channel approximately 2 microns towards the anode. Because of some local variations in the wet etch rate, this remaining GaAs was not completely removed on all devices and some were short circuited. This experience illustrates the limitations of the current surface channel formation technology.

A quasi-optical mixer was constructed by placing the SA1T2 log periodic antenna-diode on a hyperhemispherical lens made of high resistivity silicon. The system exhibited excellent antenna patterns and good mixer noise temperature and loss performance at 762 GHz. The details of this RF testing are presented by Gearhardt in the Conference Proceedings [22]. This is the first planar Schottky diode to achieve reasonable mixer noise temperature at such a high frequency.

IV. Planar Diode Fabrication Challenges

Although surface channel planar diodes have done well at millimeter wavelengths, the greatest interest and challenge lies in pushing the diode performance to the terahertz frequency range. Fabrication technology will play a major role in achieving the goal of improved high frequency performance. Following is a discussion of the most important fabrication issues:

Reduce R_s x C_{j0}

Theoretical studies and practical results with whisker-contacted diode mixers show improved high frequency performance as the R_sC_{j0} product is reduced [8]. This is achieved by reducing anode diameter and choosing optimum active layer doping and thickness. For terahertz frequencies this requires anode diameters in the 0.5 micron range. While circular anodes with diameters of one micron and above are relatively easy to fabricate, submicron devices are difficult to uniformly and repeatably produce. Few, if any, commercial mask makers will guarantee submicron circular features due to a lack of measurement methods (lines are much easier). Uniform submicron masks, deep UV lithography and reactive ion etching (RIE) may facilitate the fabrication of high frequency planar diodes. Direct wafer patterning with electron beam lithography (direct write) is also a proven method [23]. Alternative anode etch mask formation in which a relatively large mask feature is reduced (electroplating, oxygen plasma etching), or where some layer thickness (photoresist, oxide, etc) is transformed into a mask opening, may be effective [24,25,26].

The problem of planar diode anode formation extends beyond that of a uniform submicron mask. The technology requires that circular wells be RIE etched into the silicon dioxide leaving a thin layer ($\cong$300 Å) to protect the underlying GaAs from damage. This thin oxide in the bottom of the anode wells is removed with buffered hydroflouric acid (BHF) just prior to electroplating the platinum anode metallization. If this final wet chemical etch is insufficient, the resulting device may be an open circuit or may exhibit high resistance. If the etch is overdone, the resulting diode may be too large. Uniformity is important for discrete devices but even more so for multiple anode chips and arrays. The uniformity and repeatability of the process depends on accurate

determination of the thickness of the remaining silicon dioxide and its wet etch rate.

In the case of whisker-contacted diodes, the removal of this thin oxide and anode plating are performed on a chip-by-chip basis, thus providing chips for experimentation to determine the etch time for a given batch. Planar diodes, by contrast, are etched and plated on a wafer basis, with no opportunity for fine tuning. For better process control and ultimately more uniform anode diameters, a bilayer or trilayer insulation layer could be used [12]. For example, a thin (300 Å) layer of silicon dioxide could be deposited on the active GaAs and its thickness could be measured. A relatively thick layer of polyimide or other suitable polymer could next be deposited on this thin oxide. This polymer layer could be patterned with an oxygen RIE etch step which would stop at the thin SiO_2 layer. The known thickness of SiO_2 could then be wet etched prior to anode plating. This process would relax the etch rate accuracy requirement and would leave a known amount of oxide to be removed. A process of this type would probably require a substantial research effort to test polymers for chemical and thermal process compatability and reliability but would yield great potential benefits.

Optimized Chip Geometry

The geometry of the planar diode chip has a major effect on the capacitance and inductance presented to the mixer circuit. Fabrication technology limits the geometry which can be produced. Even though the surface channel diode structure is referred to as a "planar" device, we are actually concerned with all three dimensions.

Capacitance between the contact pads is normally the largest shunt conductance [10]. This capacitance can be minimized by: reducing contact pad area, separating the pads as much as possible, providing the deepest possible channel, making the channel sidewalls vertical or retrograde, or removing non-essential GaAs substrate. Technology for most of these requirements has already been developed at UVa. For example, our smallest chips have contact pads which are only 30 x 60 microns with overall chip dimensions of 75 x 200 x 25 microns. A chip with smaller pads would be very difficult to handle and bond to the circuit. A technique has been developed to completely remove the GaAs substrate and replace it with quartz. The quartz can even be removed once the chip is soldered in place [13]. As discussed previously in connection with the log-periodic antenna diode, vertical channel sidewalls are most important for short finger designs but are difficult to achieve with wet etching or a combination of RIE and wet chemical etch. A planarization method which will allow the channel to be formed before the finger could solve this problem.

Shunt capacitance from the finger must also be minimized. This can be done by reducing the width of the finger, etching the surface channel as close as possible to the anode, increasing the dielectric thickness between the n-type GaAs and the finger, or producing an upward arch in the finger. Present UVa planar mixer diodes have a 2 micron finger width. A new mask set reduces this to 1 micron for the final 5 microns of the finger length. A lower limit for width is set by considerations of alignment and mechanical strength as well as concerns about the finger resistance and inductance. A thicker dielectric would reduce the finger overlay capacitance and could be facilitated by the multilayer scheme described above. The upper limit for dielectric thickness is determined by film stress and cracking in the case of oxides. Polymers could be very

thick but may be limited by an inability to electroplate into very deep, small diameter wells. Finally, an upwardly arched finger could be a beneficial byproduct of a polymer planarization.

The optimum length and geometry of the anode contact finger in a planar diode is a topic of great interest. Some modeling has been done by Siegel to determine the effect of length on mixer noise and loss [27]. Erikson has found that finger inductance can be useful in tuning out capacitance for planar varactors [28]. Additional modeling is needed but researchers must be careful not to blindly accept model predictions. A new mask set is now available for antiparallel mixer diodes with fingers from 10 to 50 microns in length on the same wafer. RF testing of these devices will provide greater understanding of this question.

Minimize Ohmic Contact Resistance

Series resistance added by the ohmic contact is small for many planar diodè chips, especially those designed to operate at millimeter wavengths. For example, a 10^{-5} Ω-cm^2 ohmic will add approximately one ohm if the contact is 30 x 30 microns. Since ohmic contacts of this quality are easily achieved and since this pad size is at the lower limit for flip-chip bonding, simple planar diode chips are probably not seriously affected by the ohmic contact. However, devices which require ohmic contacts which are very small (< 100 μm^2) will be seriously affected unless they can be made with correspondingly lower specific contact resistance.

For example, it is desirable to reduce the ohmic contact size to minimize pad-to-pad capacitance. In these cases, a small ohmic contact could be connected to a larger bonding pad on a quartz substrate or to a beam lead pad. Also, some pads in multiple diode configurations are not needed for bonding. Smaller ohmics could thus be made to reduce shunt capacitance. Via holes may reduce the area available for the ohmic contact.

An important example of the need for the lowest possible ohmic contact resistance are integrated antenna-diodes. These devices will perform best when current flows in the metallization rather than in the buffer layer. For the log-periodic structure shown above, the contact area available adjacent to the anode and ahead of the 1 THz active antenna region (the first tooth) is only about 40 um^2. Thus, a one ohm contact resistance will require a specific contact resistance of about $4x10^{-7}$ Ω-cm^2.

Present UVa planar diodes utilize an electroplated Sn/Ni-Ni-Au alloyed ohmic contact. This contact has been measured with TLM techniques by Slade at 10^{-5} to 10^{-6} Ω-cm^2 [29]. However, measurements on device pads indicate that the specific contact resistance must be in the low 10^{-6} range. Gold germanium contact systems are reported to have specific contact resistance in the 10^{-6} to 10^{-7} Ω-cm^2 range and this contact has recently been applied to planar diodes in our laboratory. Ohmic contacts on highly doped InGaAs are reported to be as low as 5 x 10^{-9} Ω-cm^2 [30].

Improve Energy Coupling

Energy coupling to the planar diode can be improved with an integrated or hybrid planar antenna. However, antenna structures must be optimized to prevent energy loss. In the log-periodic antenna diode, for example, radiation is coupled through the semi-insulating GaAs substrate and

may be partially dissipated in the buffer layer below the antenna metallization. This loss can be reduced by using a thinner buffer layer or by limiting the buffer layer to a small region near the anode with proton isolation or selective epitaxy. Coupling may also be improved by integrating tuning structures with the antenna-diode.

V. A New Planarization Process

As previously mentioned, the present surface channel diode fabrication sequence (i.e., finger formed before channel) is not without disadvantages: (1) The isolation trench is difficult to properly form if the finger is very short or wide and devices can be shorted by conductive material which is left between the pads; (2) The geometry of the contact finger is limited to relatively simple, narrow shapes while RF performance may benefit from some other finger geometry; (3) The distance from the sidewall of the trench to the anode, which determines the finger overlay capacitance, is difficult to minimize since the anode is hidden by the finger (the finger cannot be used as a reference for the anode due to alignment errors). A conservative etch time may yield higher capacitance while overetch may produce open circuits or high resistance if the anodes are undercut. Surface channel diode fabrication would benefit from a temporary planarization process which would allow the formation of the surface channel isolation prior to formation of the contact finger. The anode contact finger could then be formed on top of this planarization layer and afterwards the material could be removed to form the air-bridge.

A planarization material for surface channel diode fabrication must meet numerous criteria: (1) easy to remove, (2) unaffected by process chemicals (including resist solvents), (3) easy to pattern, (4) low skrinkage, (5) good adhesion to GaAs, SiO_2, and gold, (6) sufficient elongation to prevent the formation of voids, (7) low viscosity, (8) and low cure temperature. The material and its method of application must produce a high level of planarization for deep trenches. Available planarization materials include Novolac-based photoresist, polyimides and other polymers [31-36]. Excellent planarization has been achieved with multiple spun-on coatings and/or thermal reflow before final curing. However, photoresist is not compatible with all of our process chemistry and cure temperatures for polyimides generally exceed 160 °C, with much higher temperatures for thermal reflow.

Workers in the multichip module (MCM) fabrication area have been planarizing metal interconnect lines for several years [37]. One of the most effective planarizing systems for this application is benzocylobutene (BCB). BCB's are low molecular weight, thermoset polymers which have demonstrated greater than 90% planarization of metal lines with a single spin application and excellent chemical resistance [38]. They are being actively developed as permanent planarizing dielectrics for GaAs IC fabrication [39]. However, BCB's require 200 to 250 °C for full cure and may be difficult to completely remove from beneath the contact finger. BCB which has been partially cured at reduced temperature may be easier to remove.

Dill of IBM proposed a simple planarization technique in 1984 which he referred to as the "top cap" method [40]. This technique consists essentially of applying a droplet of thermosetting polymer or liquid thermplastic polymer to a wafer and then covering this with a flat superstrate. Once the polymer hardened, the superstrate is removed. Dill suggested that capillary action would spread the liquid polymer to form a thin, uniform film. This technology was never demonstrated by IBM and to our knowledge it has not been demonstrated or developed by any other research

group. The method is related to a very old technique used to "polish" the surface of polymer-embedded specimens. Instead of laborious lapping and mechanical polishing of a block of cured thermoset ploymer, a rough lapped surface can be "glued" to a glass plate (treated with a release compound) with the same polymer. Once the resin has set, the block is separated from the glass. The lapped surface is filled in with the polymer and the exposed surface replicates the polished glass surface.

We have developed this technique, illustrated in Fig. 4, for device applications. A wafer with trenches is first patterned with photoresist shims near the corners. The shims are used to control the thickness of the planarizing layer and must be formed in areas on a plane which is parallel to the original GaAs epitaxy (i.e., not on metallized or etched regions with different heights). Photoresist must be completely removed from all other regions. This can be assured during development of the shims by providing a high exposure level or even a second long exposure to areas where resist may be hidden from direct exposure, such as under overhanging structures. The shims are baked at relatively high temperature (120 °C) and exposed to short wavelength UV (deep UV cure) to prevent chemical attack by the liquid polymer. Next, a low viscosity thermoset polymer is applied to the wafer. A flat, smooth superstrate is then placed atop the wafer. The weight of this superstrate (plus any added force) pushes it to the level of the shims and expels excess polymer. The polymer is cured in this position and finally the superstrate is removed.

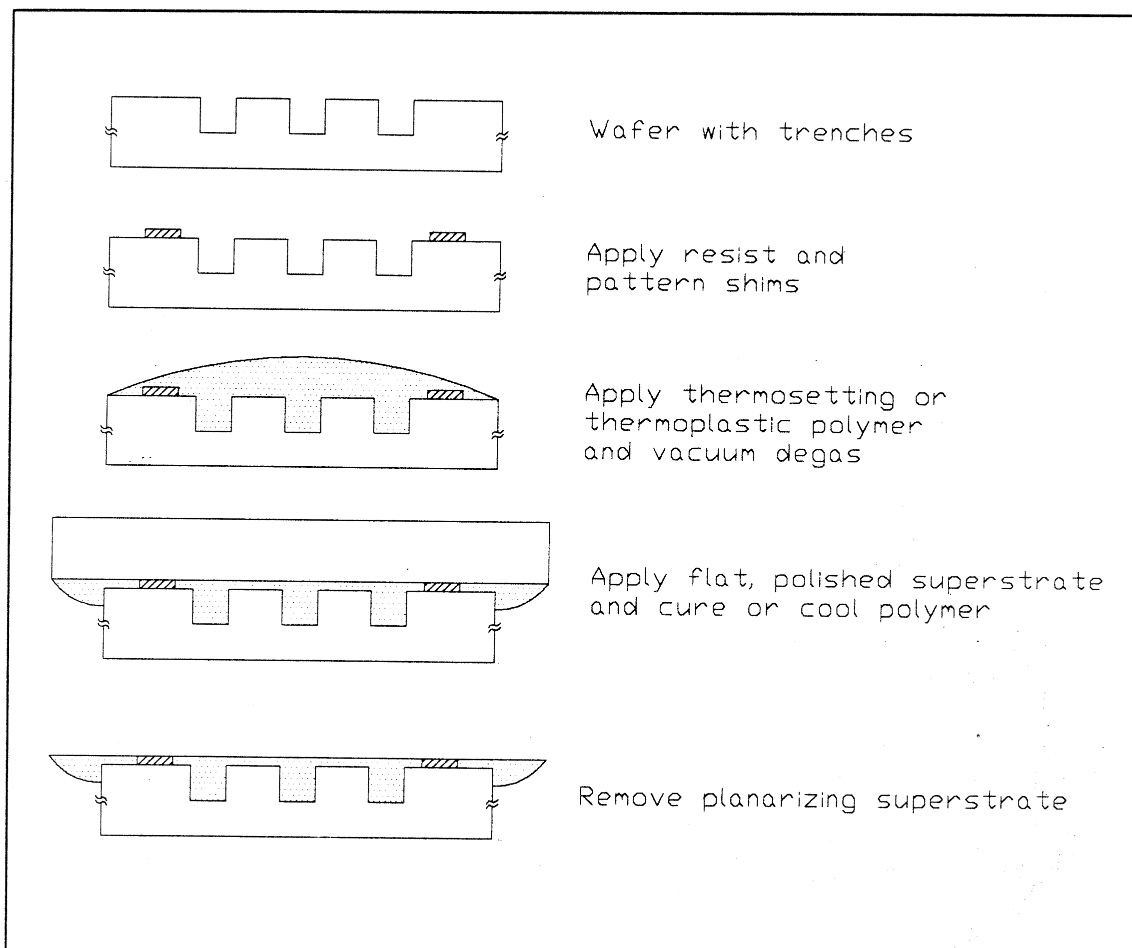

Figure 4. Superstrate Replica Planarization

In practice the wafer is inverted and placed onto the superstrate. A "curing stack" consisting of glass plates and thin Mylar sheets has been developed to align and hold the wafer and superstrate and to apply a controlled pressure to the sandwich. In addition to this fixturing, the choice of polymer and superstrate are most critical. Epoxy resins were considered to be promising candidates. Many epoxy formulations are available with generally excellent adhesion, low shrinkage, good adhesion, high elongation, and good chemical resistance. A number of epoxy resins were tested and our current material of choice is Epotek 377. It can be cured at temperatures as low as 120 °C and has excellent resistance to chemicals used in our process. It can be repeatedly patterened with photoresist and the resist can be stripped with acetone. The cured polymer can be readily etched in oxygen RIE or oxygen plasma with no apparent residue. As with most other polymer etching with oxygen, a polymer platter must be used at low pressure to avoid residue from backsputtered material.

The superstrate must be flat and smooth and must be removable. A suitable release layer may eventually be found so that a high quality optical flat or silicon wafer could function as a reusable superstrate. For this preliminary work a simpler approach was taken. A polished optical window made of sodium chloride was used. Inexpensive NaCl windows are available for infrared spectroscopy [41]. High quality, optically flat NaCl windows designed for infrared laser work are available at higher cost. These windows are rapidly removed with water which has no effect on the epoxy. The adhesion of the epoxy to the NaCl is excellent.

This procedure has been tested by planarizing GaAs wafers which have a series of deep trenches etched into the surface. The SEM photographs in Fig. 5 show a cross section which has been diced through one of the planarized wafers. The trench is approximately 14 microns deep and 80 microns wide. The wet etch used to form the trench produced a retrograde sidewall. The dark layer is cured epoxy which is approximately 2 microns thick over the unetched region. The trenches are almost perfectly planarized. Profilometer measurements indicate a 0.5 micron drop over the trench which represents a 95% planarization level.

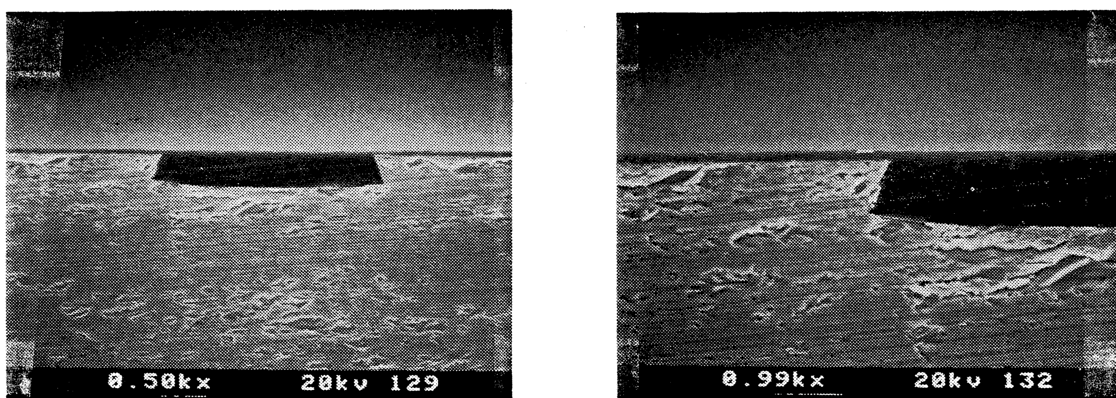

Figure 5. Trench Planarized By SRP Method

Figure 6 shows plan and cross sectional views of proposed SRP planarization and contact finger formation for the log-periodic antenna diode. After the anodes and ohmic contacts are produced, the surface channel trench is formed. The initial etching will be done with RIE to establish a vertical-walled, flat-bottomed trench. Slow wet etching of the gallium arsenide can then be used to "trim" away excess GaAs and move the channel wall as close as possible (0.5 micron) to the anode. Visual inspection and re-etch can be used to control this step.

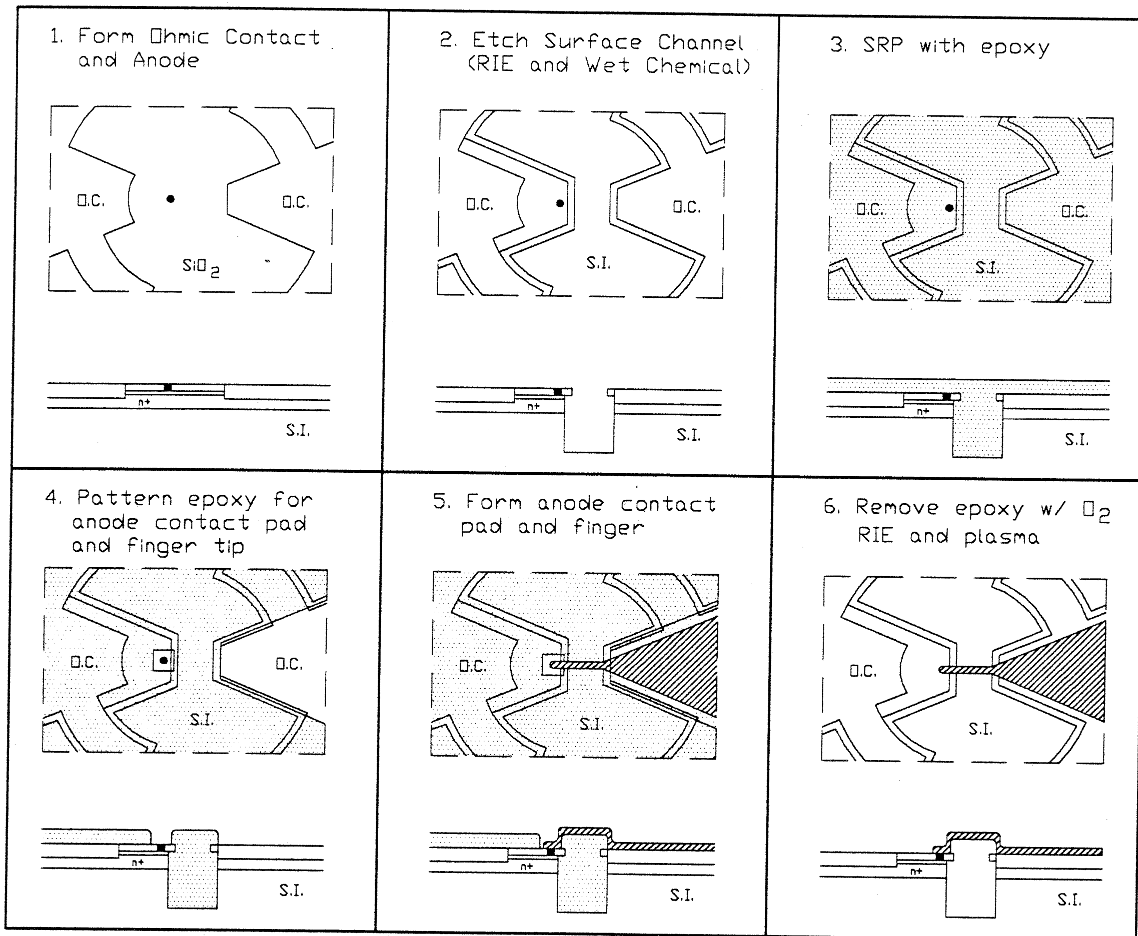

Figure 6. Surface Channel Fabrication With Planarization

Summary

Planar technology is now replacing whisker-contacted diodes at millimeter wavelengths. This technology shows great promise for submillimeter wavelengths, both as heterodyne receiver elements and as a frequency multipliers. Integration of multiple diodes and antennas will improve performance, expand the range of receiver designs and simplify their construction. The integrated log-periodic antenna diode has demonstrated great promise for rugged, broad band terahertz receivers.

The greatest challenges in fabricating planar diodes for submillimeter wavelengths are uniform, repeatable submicron anode formation and improved surface channel formation. The submicron anode problem will be solved with better mask formation techniques, possibly aided by multilayer dielectrics. Planarization technology, especially with polymers, is expected to improve the surface channel isolation process which will reduce the shunt capacitance of the diodes, improve uniformity and yield, and remove some design constraints which presently limit the geometry of the diodes.

Innovation and refinement of fabrication techniques will play a major role in the effort to improve Schottky diode performance, along with device theory, epitaxial layer engineering and RF design. New fabrication technology can drive the design of planar diode circuitry much in the same way that manufacturing technology influences mechanical design and production. These new fabrication techniques will require a significant research effort to bring them to maturity.

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