FIXED-TUNED SUBMILLIMETER WAVEGUIDE MULTIPLIERS USING MMIC TECHNOLOGY

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ABSTRACT

We have developed tools and fabrication processes which led to the design and fabrication of a MMIC waveguide doubler to 320 GHz and a MMIC waveguide quadrupler to 640 GHz. This includes extensive diode modeling and analysis and optimization [1], design and fabrication of input and output ridge-waveguide-to-microstrip transitions, to provide the fixed tuned input and output ports, and the design and fabrication of the MMIC multiplier chips containing the active devices and all matching elements and bias circuitry [2].

To date, measurements have yielded 10 μW at 640 GHz and 420 μW (2.7% efficiency) at 320 GHz, with 15 mW of pump power at 160 GHz. We believe these are the first working waveguide MMIC multipliers above 200 GHz. The waveguide block concept used for these multipliers is very efficient for mounting/dismounting devices, allowing rapid and repeatable measurements of different chips.

However, these measurement results are much poorer than expected from our original analysis, and we have taken a more detailed look to explain the discrepancy. After including the diode physical structure and radiation loss in the circuit models, we have been able to obtain excellent agreement between our measured performance and that predicted from our finite element analysis. With this improved circuit model in hand we have designed a new MMIC doubler which is expected to perform significantly better than the original chip. Due to the limitations of microstrip (substrate thickness) above 300 GHz, we have begun a CPW design with the more accurate device model as well.

INTRODUCTION

There are now a significant number of space applications in the Earth remote sensing, planetary and astrophysics areas which require solid state local oscillator sources in the 300 to 1000 GHz range. Although some new approaches look very promising in the long term (photomixers, fundamental or harmonic oscillators...), solid state harmonic multipliers based on varactor diodes still offer the best performance in the near term. For many years, the most common implementation has been the discrete Schottky barrier honeycomb diode mounted in a waveguide block and contacted via a fine whisker wire [3]. More recently, the whisker contacted

diode has been replaced by the planar discrete diode, used in a similar mount configuration [4]. Both of these approaches have led to very good results, and whisker contacted diodes are still the only way to reach the higher submillimeter wave frequencies. A recent planar diode result (an array of six varactor diodes on a single planar chip) has yielded amazing output power in the 100 to 300 GHz frequency range (76 mW at 160 GHz, and 8 mW at 320 GHz [5]). However, all of these discrete diode approaches have limited circuit flexibility, are complicated to analyze and difficult to assemble. Also, the output power available above 400 GHz is low in the case of the whisker diode, and non existent in the case of the discrete planar device.

Because we need high efficiency, high output power, reliable wide-band multipliers up to 1 THz, we have proposed a new approach, which pushes further the integration of the multiplier device and surrounding circuitry, moving toward a true GaAs MMIC implementation. The MMIC's we are now fabricating at 300 and 600 GHz are composed of GaAs chips containing the active device(s), all matching and bias circuitry and transitions to a new waveguide block configuration, in which the chip is coupled to inline input and output waveguides by means of micromachined E-plane ridges [6,2].

We believe that a benefit of this approach is that it provides a very flexible, potentially wide band structure, in which one can easily accommodate many different chip designs and devices. Like MMIC's at lower frequencies, we have found that a very thorough analysis of the entire structure is required to accurately predict the performance.

DESIGN AND FABRICATION

The basic concept used for all the multiplier designs presented here is shown in Figure 1. Thin metallic ridge transitions, similar to those employed by [6], are used to convert the input and output signals from fundamental waveguide to a microstrip mode. All other RF functions - frequency multiplication, matching and filtering - are then performed on chip. No tuning capability, other than adjustment of the bias voltage, is present. The chip is held in place under the ridge transitions with a spring loaded mechanical micrometer drive assembly and no soldering is required. Wire bonds are used to couple bias into the chip through channels perpendicular to the input and output waveguide (not shown in the Figure).

Because of their proven performance in this frequency range, we have implemented the multiplier circuits with planar Schottky barrier diodes. Our designs are based on the derived equivalent circuit of the strip or T-gate rectangular diode [1]. The rectangular anode devices have lower than average series resistance compared to traditional planar varactors, making them ideal candidates for higher frequency circuits. We implemented a Schottky barrier diode model, including saturation effect [7], appropriate for the rectangular anode geometry, in an harmonic balance program. The electrical parameters of the diode are described as a function of the epilayer doping, Nd and the anode length and width, L and W. Using the diode model, we optimized the physical parameters of the diode, i.e. doping profile and anode geometry, for specific input power and frequency, and determined the optimum embedding impedances for each harmonic [1].

The diodes are matched to the waveguide input/output ports at the fundamental and harmonic frequencies through traditional microstrip elements - stubs and high/low impedance filters. Bias is coupled in through bypass capacitors formed on-chip. The matching circuit must provide both filtering and impedance matching from the real impedance of the ridge transitions to the complex impedance of the diode, at the input, output, idler and higher harmonic frequencies. Figure 2 shows a picture of the 320 GHz doubler chip. Since the diode is in series in the circuit, it must be shorted at the input frequency on the output side (right of the diode). A quarter wavelength open radial stub provides this short. Similarly, another stub shorts the diode at the output frequency on the input side (left of the diode). A high-low impedance matching circuit converts the 30 Ohm real impedance of the ridge to the optimized complex diode impedances at 160 GHz. Similarly on the output side, another high-low impedance circuit matches the diode impedance at 320 GHz to the final 50 Ohm microstrip line which couples to the output waveguide ridge. As we are working at high frequencies (320 and 640 GHz), the substrate must be mechanically as thin as possible. The circuits have been designed for a 50 μm thick GaAs substrate, the thinnest substrate we felt could be reasonably handled. The nominal diode size for which we designed our circuit is 10x1.3 μm^2. Variations of 1.2x7 and 1.3x12were also included on the mask set.

Details of the MMIC fabrication process can be found in [5]. The recessed and alloyed ohmic contacts were formed (bottom to top) of Ni/Ge/Au/Ni/Ag/Au. Mesas were reactive-ion etched using chlorine and boron trichloride. The air-bridge Schottky contacts were made of evaporated Ti/Pt/Au. 1500 angstroms of silicon nitride passivation/dielectric was deposited over the top in a plasma-enhanced chemical vapor deposition system. A subsequent nitride etch and air-bridge metal step formed the necessary isolation for bias, input, and output connections. Before scribing, the wafer was mechanically lapped to 50 μm. DC characterization of the chips shows very good yield. The I(V) and C(V) characteristics are as expected, and Rs is as good if not better than that predicted with our device model.

The ridge transition works like a Chebychev step transformer that matches the impedance difference between the waveguide mode (~500 Ohm) and the microstrip mode (50 Ohm). The ridges are fabricated from BeCu using a double sided photoetch technique. The 160 GHz ridge is formed from .003" BeCu and the 320 and 640 GHz ridges from .0015" sheet. The sheets, containing many ridges, are etched in ferric chloride and then gold plated. We obtained an overall accuracy of 2-7 μm for the final dimensions. After separation from the "spider mount" (Figure 3) the individual ridges can be readily handled and are soldered permanently into position in the split-block waveguide mount.

The multiplier mount which contains the ridge transitions and multiplier chip is formed in three parts, two of which are used to permanently fix the ridges in place at the center of the waveguide. A separate top piece protects the chip and, when removed, allows access for positioning and wire bonding the bias line during assembly. The waveguides and transitions are formed in the split block (Figure 4), but once the ridges have been positioned and soldered in place the two halves are permanently mated. Insertion of the GaAs chip is made possible by a spring loaded moving post controlled by a micrometer with a simple cam mechanism. During contacting, the chip is placed in position in a recess under the two ridges and moved upwards

into final position where it is pressed lightly against the ridges on both sides (Figure 5). Once contact is made, the micrometer is locked and no further adjustments are required.

Measurements of the transmission properties of the ridge and the block were performed in a test mount at 180 GHz. A block similar to that described above has been fabricated, with identical input and output waveguides to allow a back to back ridge measurement with a straight 50 Ohm transmission line in-between. The measured transmission through the two transitions and the wafer with the 50 ohm line are shown in Figure 6. When the measured waveguide loss of 0.5 dB and calculated substrate loss of 1 dB are subtracted, the ridge transitions show an insertion loss of better than 0.75 dB each over 40% bandwidth.

MEASUREMENTS

Assembly of the block starts with permanent fixing of the two ridges. The ridges are first positioned and then epoxied in cavities provided on one half of the split waveguide block, such that they fall in the center of the E-field plane of the waveguide (Figure 4). They are then soldered to the block to provide a DC path to the chip. As will be seen later, positioning the ridges is critical. Several contacts and actual RF measurements are necessary to verify that the ridges are in their optimum position. Rotation and height are easily controlled by positioning the ridges against a chip placed in the waveguide. The longitudinal position of the ridge along the waveguide axis is more difficult to set, and requires precise measurement of the dimensions. Once the ridges have been fixed in place, the two block halves can be permanently mated, and no further adjustments are needed. For making measurements on actual MMIC chips, the chip is placed on top of the moving post, which is then driven up until the ridges come in contact with the microstrip lines (Figure 5). Mounting and dismounting a chip takes only a few minutes.

Since there is no tuning besides DC bias, RF measurements are very simple to perform. A BWO tube providing around 15 mW output power in the 145 to 175 GHz band is used as a source. This is followed by a variable attenuator and then the multiplier block. At 320 GHz, a 140-220 GHz Anritsu power meter (used out of band) is used to detect the signal. At 640 GHz, the output is radiated through a feed horn machined into the split block, and a planar diode Schottky detector [8] is used to initially detect the signal and determine optimum bias and frequency response. In both cases, a Thomas Keating acousto-optic bolometer was used to calibrate the detected power. For return loss measurements, a directional coupler can be inserted between the attenuator and the input waveguide of the multiplier block.

Using the set up described, we measured a maximum output power of 420 μW at 320 GHz, corresponding to an efficiency of 2.7%. At 640 GHz, we are near the sensitivity limit of the Keating power meter and measure approximately 10 μW.

Measurements over a range of chips with the same anode area gave similar output power (300-420 mW) at 320 GHz. We also observed that the DC current detected in the diode conforms to what is expected from analysis with a reverse bias of 2 V, the detected current was 100 μA, showing that there is good input power coupling. The effect of diode biasing follows

the expected trend for high quality varactors, with optimum power conversion at a reverse bias which is about half the breakdown voltage.

When the ridge transitions are not optimally aligned, we still measure repeatable performance among chips of a particular diode size, but output power and input coupling efficiency are both degraded (maximum output power around 100 μW, very low detected current), and the frequency for maximum output power is shifted.

The best performance was obtained with the smallest diode size (1.2x7 μm^2). The nominal anode gave poorer input coupling, and almost no output power (maximum around 100 μW).

The strong effect of the ridge position on the chip performance is consistent with the behavior of the Chebyschev transformer when the last section is varied in electrical length. If the ridges are mounted slightly off in longitudinal position, the transformation provided by the last ridge step and microstrip line is directly affected. Future ridges will mitigate this effect by using tapered transitions.

PERFORMANCE ANALYSIS

Since the diodes appeared to be behaving properly, we suspected that the poor multiplier performance was due to neglected properties of the circuit itself. For expediency during the initial design of the MMIC, some effects were knowingly neglected, such as the diode mesa and air bridge geometry, microstrip radiation effects, and tolerances of the ridge transitions. In order to check the accuracy of our measurements and to understand the reason for our poorer than expected performance, we conducted a more careful analysis of the complete 320 GHz doubler using a combination of finite element and harmonic balance analysis, in which we included the diode mesa/air bridge and radiation effects. The approach consisted in describing each individual circuit element in Ansoft's Maxwell Eminence, deriving the S parameters, integrating together all the pieces, and finally applying harmonic balance techniques to derive the full circuit performance (including ridges).

An example of the individual structure analysis is shown Figure 7, where the air bridge and mesa's have been accurately modeled (a photo is shown as Figure 8). In our original design the effect of the diode mesas and air bridge were modeled as simple transmission lines. The finite element structure includes two microstrip ports and a diode port defined using a "coaxial probe", where the Schottky contact lies. The S parameters of that structure are then imported to a circuit simulator, and the diode embedding impedances are compared with those of the diode only, and those of the diode with the transmission line equivalent circuit. It can be seen in Figure 9, that the effect of the mesa/air bridge combination is quite large, especially at 320 GHz, where the embedding impedance becomes inductive when in fact it was designed to be capacitive. Although the effect is due to the overall structure, and therefore difficult to describe by means of a simple equivalent circuit, it is understandable that its effect is significant, considering that the

overall structure length is of the same order as the quarter wavelength radial stub shown in Figure 8.

Similarly, we have computed the S parameters of the output microstrip circuit associated with the output ridge (Figure 10). In our original analysis, only conductive and dielectric losses were taken into account. The finite element analysis adds radiative loss. Figure 11 shows the comparison of the two cases and the significance of the radiative loss. A closer examination shows that most of the radiation occurs at 320 GHz in the two radial stubs.

Finally, we have integrated all these elements together with our diode model in an harmonic balance circuit simulator (MDS), and compared the computed performance of the MMIC with measurements at 320 GHz. Figure 12 shows the result, a pretty good match. The same analysis also shows good agreement between measurements and computed performance for the other diode sizes we have fabricated. A separate analysis in which we have shifted the ridges longitudinally also confirms the trends observed during measurements, i.e. shifted maximum output power frequency and a degraded power level. These results make us confident that our multiplier is in fact working as designed - although not up to expectations! However, with the more accurate analytic description in hand, we can now redesign the circuit to realize its full performance potential.

CONCLUSION

We have demonstrated full MMIC multipliers with output power at frequencies as high as 640 GHz. The first iteration of our 320 GHz doubler design has demonstrated that this approach has the potential to realize reasonable performance, and an efficiency of 2.7% has already been obtained. The current performance, especially at 640 GHz, is much poorer than what we were expecting, but a more accurate analysis of the physical structure gives good agreement with measurements and has allowed us to understand where the deficiencies of our design lie. Analysis indicates that these problems can be easily fixed, and a second iteration is already in progress and should provide greatly improved performance at 320 GHz (Figures 13 and 14).

The design, measurements and analysis described in this paper also helped us to identify some inherent problems with the present circuit realization, especially above 320 GHz. We have found that the microstrip ridge and its step transformer design introduce too tight a tolerance for simple mounting in the block. Also, at higher frequencies, the problem of radiation in the thick GaAs substrate is disastrous. A solution to both of these problems consists in the use of coplanar transmission line (CPW), and tapered ridges for the transitions. Such a design is now under way.

ACKNOWLEDGMENTS

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FIGURES

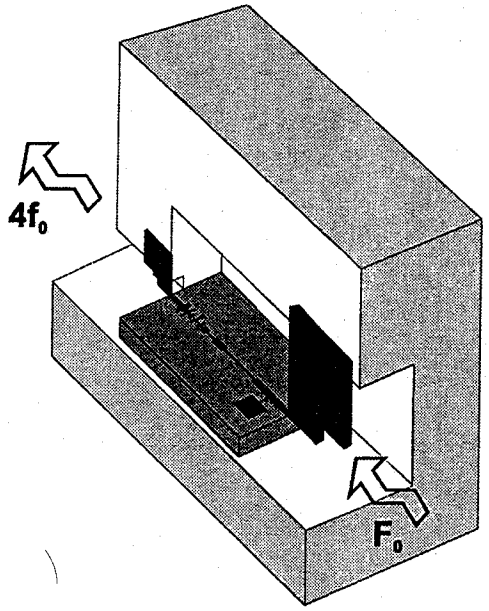

Figure 1 - Conceptual drawing of a MMIC multiplier in its ridge/waveguide block.

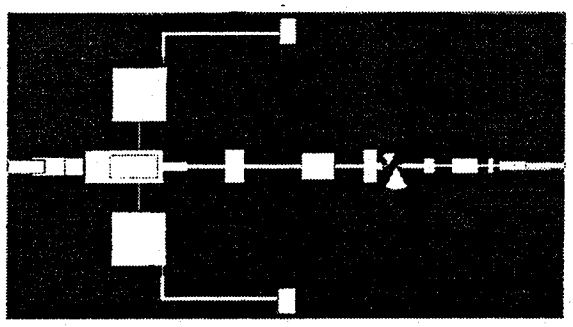

Figure 2 - Picture of the 320 GHz MMIC doubler chip.

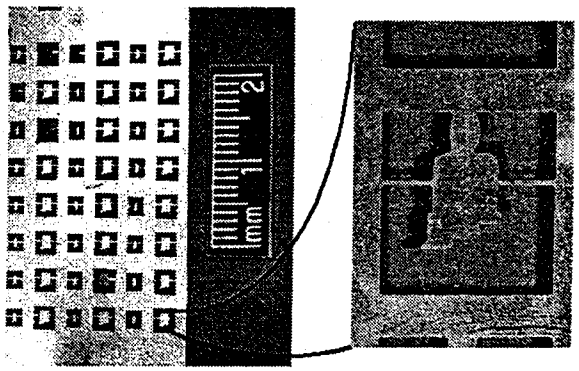

Figure 3 - Picture of the photoetched BeCu ridge sheet and close up of one ridge.

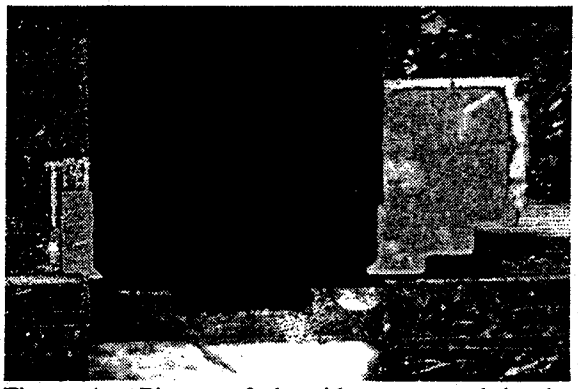

Figure 4 - Picture of the ridges mounted in the waveguide block (here a 160 GHz ridge and a 640 GHz ridge in the quadrupler block).

Figure 6 - A MMIC multiplier chip mounted in its ridge waveguide block. One can barely distinguish the ridge tips on the left and right of the chip, contacting the microstrip lines.

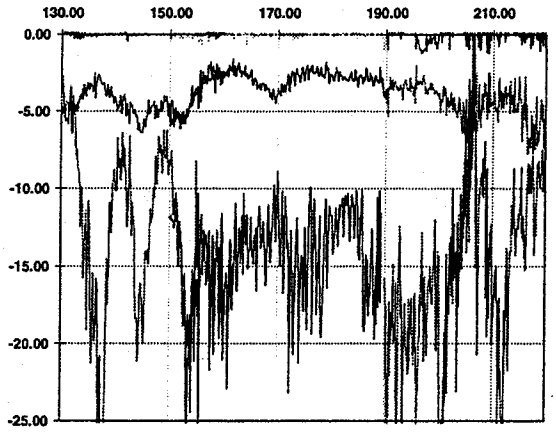

Figure 5 - S21 and S11 of a back-to-back ridge transition (two ridges and a 50 Ohm through line), ridge designed for 180 GHz.

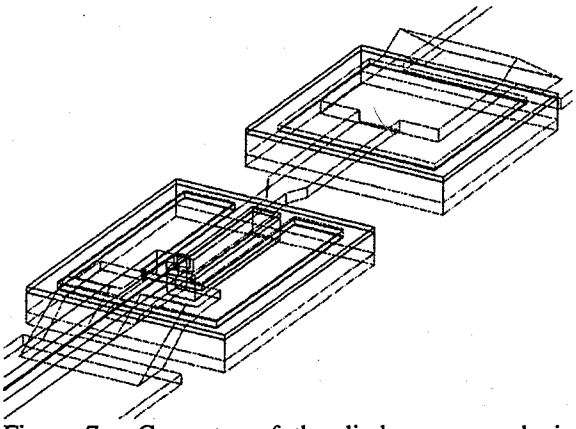

Figure 7 - Geometry of the diode mesas and air bridge as described in the finite element analysis.

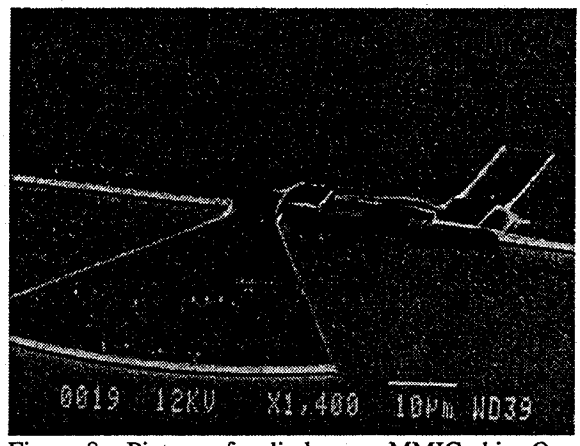

Figure 8 - Picture of a diode on a MMIC chip. One can see the mesas, air bridges, a 320 GHz quarter wavelength radial stub, and a 640 GHz quarter wavelength stub.

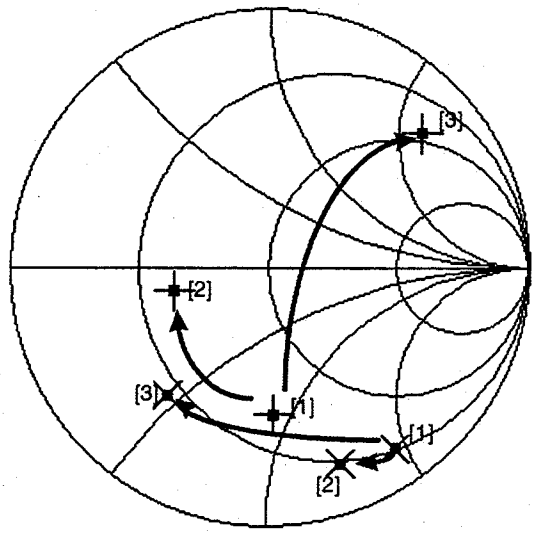

Figure 9 - Embedding impedances at 160 GHz (X) and 320 GHz (+), for the diode alone [1], for the diode with transmission line equivalent circuit of the mesas/air bridge [2], and with the finite element analysis of the mesas/air bridges [3].

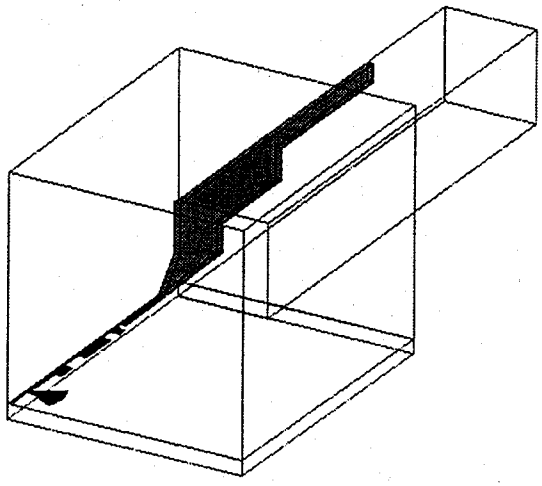

Figure 10 - Geometry of the output microstrip circuit and output ridge of the 320 GHz MMIC doubler, as described in the finite element analysis.

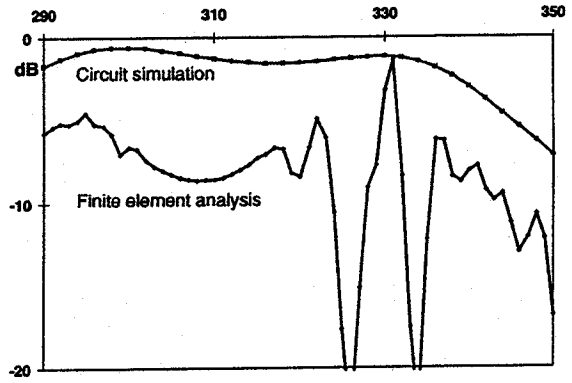

Figure 11 - Comparison of the performance of the output circuit of the 320 GHz MMIC doubler, analysed with a circuit simulator and with finite element.

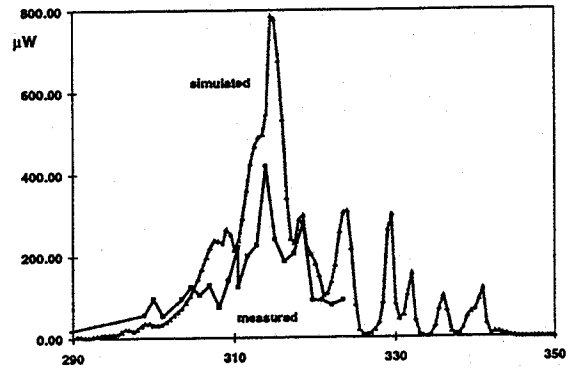

Figure 12 - Comparison of the measured and computed performance of the 320 GHz MMIC doubler using finite element analysis for each component.

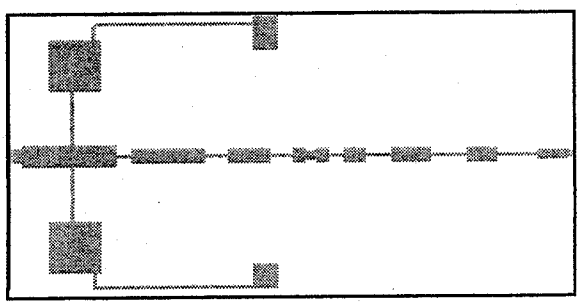

Figure 13 - Second iteration design of a 320 GHz MMIC doubler using full finite element analysis.

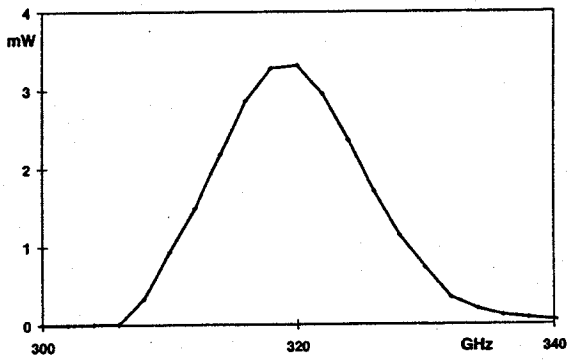

Figure 14 - Performance computed with finite element analysis and harmonic balance of the second iteration design of the 320 GHz MMIC doubler. Input power is 15 mW at 160 GHz.