A BACK-TO-BACK BARRIER-N-N+ (bbBNN) DIODE TRIPLER AT 200 GHz

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ABSTRACT

This paper describes the performance of planar back-to-back Barrier-N-N+ (bbBNN) devices for mm- and submm wave multiplier applications. A technique has been developed for characterizing planar bbBNN devices with Vector Network Analyzer, which gives both the series resistance and voltage dependent capacitance of the device. Results show that bbBNN devices do not have a high series resistance like Barrier-Intrinsic-N+ (BIN) devices. Multiplication efficiency of bbBNN devices has been calculated using large signal analysis approach. A high C_{max}/C_{min} ratio is essential for high efficiency. The embedding impedance requirement has also been analyzed. So far, flange-to-flage tripling efficiency of 2.9% has been achieved using these planar devices in a 200 GHz crossed waveguide mount. The efficiency at the device is estimated to be about 6%. This is the first reported experimental result with a bbBNN waveguide frequency multiplier.

INTRODUCTION

To achieve the high sensitivity and spectrai resolution requirements of the submillimeter wave space missions, the baseline focal plane instrument consists of

heterodyne radiometers. In a heterodyne radiometer, a remote signal is downconverted to a much lower frequency by mixing with a local oscillator (LO) signal in a nonlinear device. Emphasis is placed on using technologies which are space qualifiable. The current approach is to use a solid state mm-wave Gunn oscillator driving a chain of multipliers to generate the desired frequency. One of the primary causes of failure in mm- and submm-wave mixers and multipliers is the whisker contact. Planar varactor devices are being developed to replace whisker contacted devices in order to improve the performance and ruggedness of spaceborne submillimeter wave heterodyne receivers [1]. One candidate is the planar back-to-back Barrier-N-N^+ (bbBNN) varactor device. It exhibits a very sharp change in its capacitance versus voltage resulting in very efficient harmonic generation with small input power levels. The bbBNN device has a symmetric C-V and an anti-symmetric I-V characteristics, thus generating only odd harmonics. Therefore, there is no need for an idler termination in the case of a frequency tripler. It is expected that bbBNN devices can be made to operate efficiently at frequencies over one terahertz [2-6]. Lower leakage current in these bbBNN devices provides an advantage over the conventional Schottky devices.

DEVICE DESCRIPTION

A conceptual diagram of the device is shown in Fig.1. It consists of several layers: the barrier, a sheet doping layer, a moderately doped layer and a highly doped region [6]. The layer thicknesses and compositions can be adjusted for optimum performance. When forward bias is applied, charge supplied by the sheet doping layer accumulates at the barrier, resulting in the maximum capacitance of the device, determined by the barrier thickness. When reverse bias is applied, the charge is depleted to the heavily doped n^+ region and the capacitance is minimum, determined by the barrier and the moderately doped region thickness. The architecture of the GaAs based BNN device presented in this paper is illustrated in Fig.2. The structure from the top surface down, is (i) a thin GaAs cap layer (optional), (ii) an AlGaAs layer that is sufficiently thick to preclude tunneling but sufficiently thin to allow a large capacitance per unit area (15 to 20 nm of $Al_{0.45}Ga_{0.55}As$ is typical), (iii) a highly doped (delta doped) region which introduce a built-in potential to ensure that the high capacitance mentioned above is achieved at zero voltage, (iv) a moderately doped GaAs drift/varactor region in which all of the doping can be depleted with little parasitic conduction to the metal contact

pads, and (v) a highly doped region that provides a low resistance path between the two metal contact pads. The fabrication process is described in details in [5].

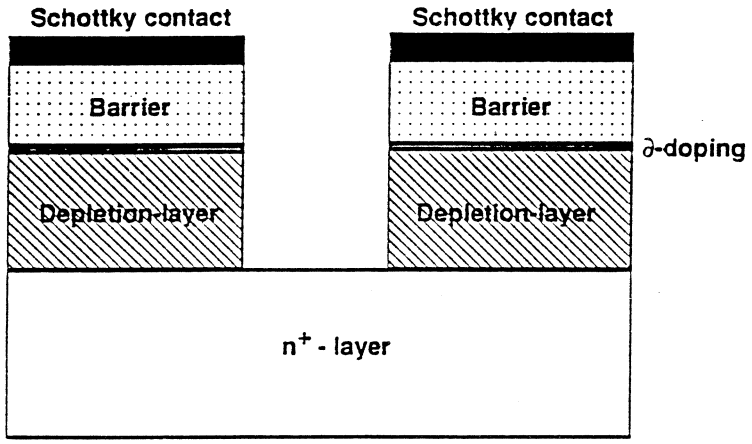


Fig.1 Back-to-back BNN varactor

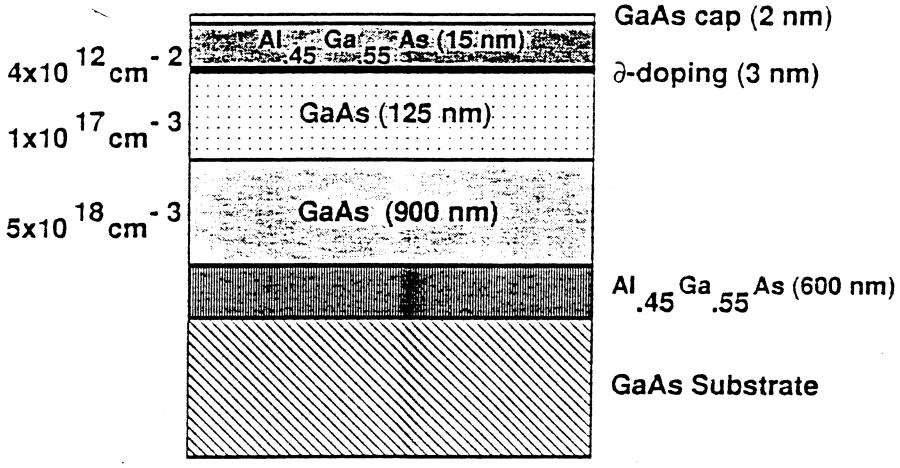
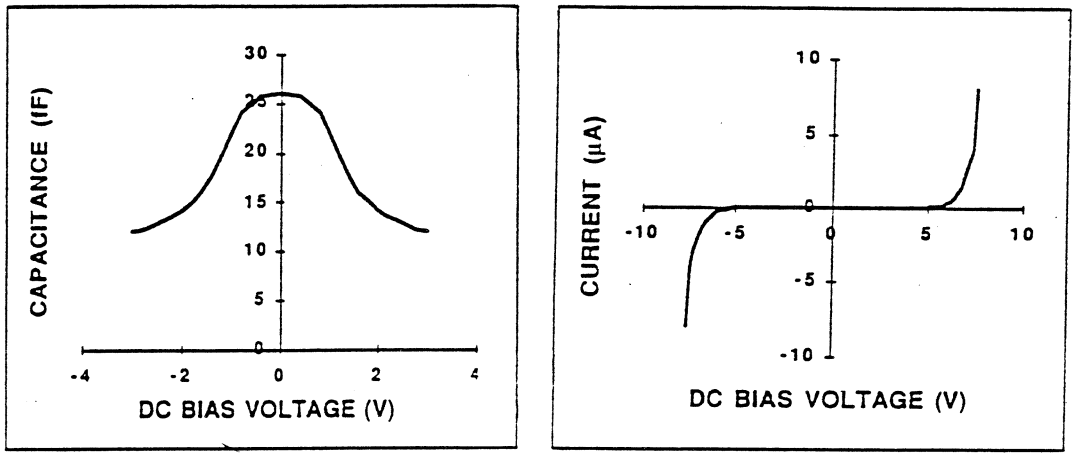


Fig.2 A typical MBE grown GaAs/AlGaAs layer structure for BNN diodes used in this study.

bbBNN VARACTOR CHARACTERIZATION

Devices were first characterized by measuring the current/voltage (I-V) and capacitance/voltage (C-V) characteristic at 1 MHz. Fig.3(a) shows the capacitance of a 2 μm X 4 μm device. Fig. 3(b) shows the DC leakage current, which is many orders of

magnitude lower than that for the conventional Schottky diodes. The series resistance of the device cannot be determined in the conventional way from the DC I-V curve. However, the remaining series resistance of some of these bbBNN devices were measured by shorting the device with an electric shock. With this technique, a DC resistance for several bbBNN devices was found to be between 7-14 Ω. This technique damages the device permanently and does not necessarily give the correct series resistance of an operating diode.



(a) (b)

Fig.3 Measured (a) C-V and (b) I-V characteristics of a 8 μm^2 bbBNN varactor diode.

In order to more accurately determine the series resistance, a special mount was designed for mounting the planar bbBNN devices to perform S-parameter measurements with a HP 8510C vector network analyzer. Measurements were done at 1-20 GHz with 10 dBm source level and 20 dB port attenuation. The bias voltage was varied from -3.0 V to +3.0 V. S11 of the device at different bias voltages was measured. The results were fitted with a linear equivalent circuit model using HP's Microwave Design System (MDS). This technique gives both the series resistance and the voltage dependent capacitance of the device. Fig. 4 shows a schematic diagram of the device mounted in a test mount (see also [7]). Fig.5 shows measured S11-response at two different bias voltages. Fig.6 illustrates the equivalent circuit of the test mount and the varactor device. Series resistance values of about 11-14 Ohm were measured using this technique for various devices having maximum capacitances of 25-60 fF.

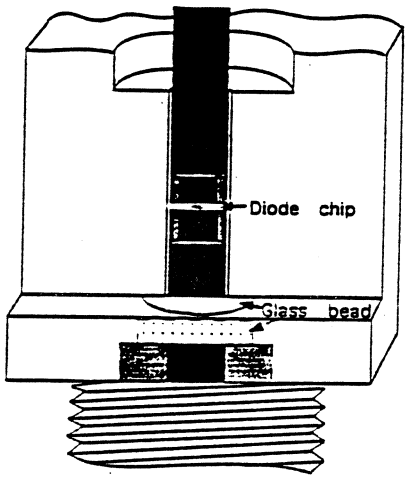
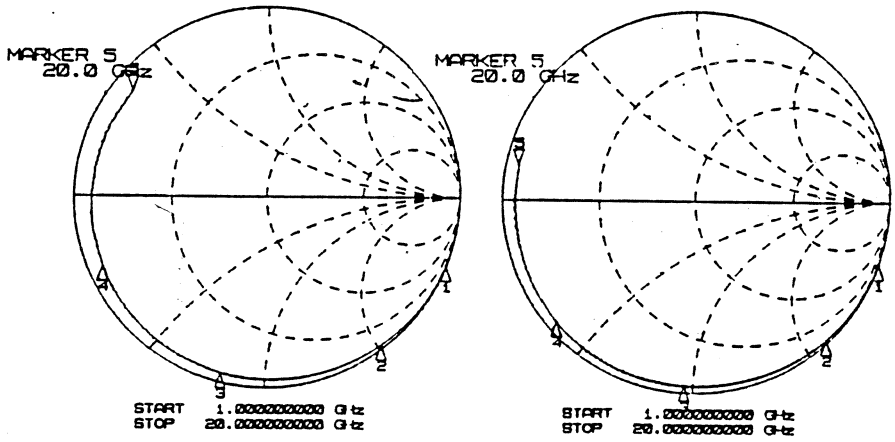


Fig.4 Schematic diagram of the planar bbBNN device in a test mount without the cover.



(a) (b)

Fig.5 Measured S11 - response at 1-20 GHz of the bbBNN device at (a) zero bias voltage and at (b) 2.0 volt (input reference plane inside the K-connector).

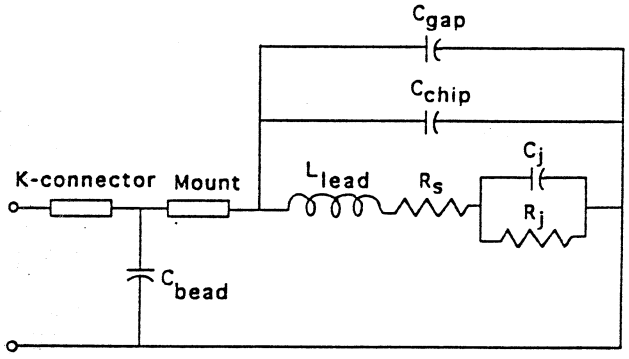


Fig.6 Equivalent circuit of the device in the test mount.

LARGE SIGNAL ANALYSIS

To achieve optimum performance of the device, it must be provided with the appropriate circuit embedding impedances. The impedances at the input and output frequencies must be set to maximize power coupling into and out of the device. The general circuit requirements are matched terminations at input and output frequencies, open circuited terminations at the higher harmonics and optimum reactive terminations at the idler frequencies.

A modified version of the nonlinear program by Siegel et. al [8], was used to calculate the tripling efficiency of the bbBNN devices. This analysis also optimized embedding impedance values. Measured C-V and I-V characteristics of a device with anode area of 8 μm^2 (as shown in Fig.3) were used to carry out large signal analysis of bbBNN devices. Since the series resistance is important in evaluating the device performance, calculations were carried out for a range of resistances. Fig.7 presents efficiency versus input power for a bbBNN tripler to 192 GHz with the series resistance of the device as a parameter. Theoretical efficiency is found to be high at low input power levels. Due to a very low leakage current, efficiency of the device does not degrade significantly when the measured I-V characteristic is included.

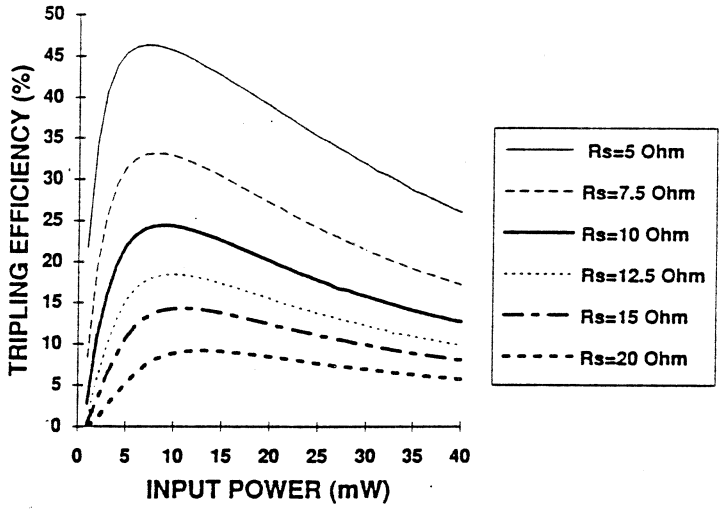


Fig.7 Calculated tripling efficiency at 200 GHz for bbBNN varactor with series resistance of the device as a parameter.

The effect of C_{max}/C_{min} ratio on the device tripling efficiency was also analysed using the large signal analysis approach. Fig.8 shows the tripling efficiency versus input power plot parameterized by the C_{max}/C_{min} ratio. Here, C_{max} is assumed to be 30 fF while C_{min} is changed. In practice this can be achieved by changing the epilayer thickness while the barrier thickness remains constant. The minimum capacitance is reached when the epilayer (in one of the back-to-back diodes) is completely depleted. The voltage required to fully deplete the epilayer depends on both the epilayer thickness and the epilayer doping. The width (FWHM) of the C-V curve was fixed by decreasing the epilayer doping to offset the effect of increasing the epilayer thickness. This has a minor effect ($\leq$ 1 Ω) on the series resistance. In these calculations, the series resistance was assumed to be constant.

Calculated results (Fig.8) show that, the highest possible C_{max}/C_{min} value is desirable independent of the input power available.

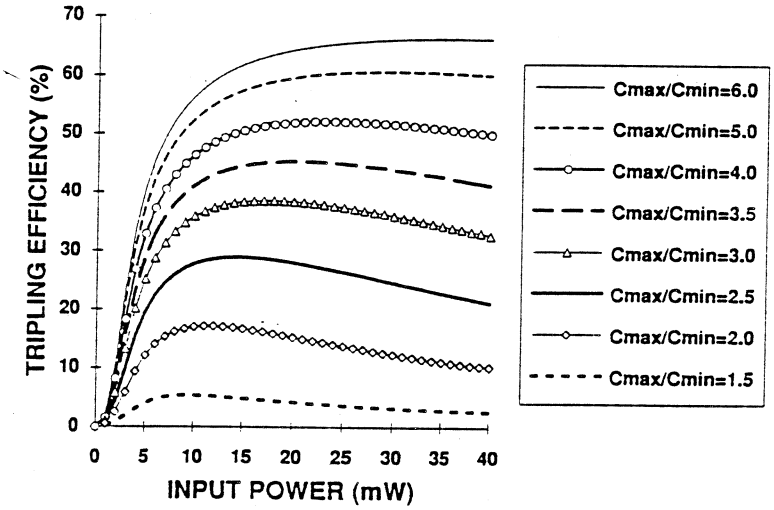


Fig.8. Tripling efficiency versus input power plot at 200 GHz parameterised by C_{max}/C_{min} (Rs=12.5 Ohm).

EXPERIMENTAL TRIPLER PERFORMANCE

The embedding impedances are provided to the planar bbBNN device by a crossed waveguide mount. A schematic of the crossed waveguide block of the 200 GHz mount is shown in Fig.9. The output waveguide in the mount is actually oriented

perpendicular to the plane of the paper.The planar bbBNN device is mounted spanning the output waveguide as shown in the diagram. The input waveguide is 0.148" x 0.074" and output waveguide is 0.039" x 0.010". The input power is coupled to the varactor in the output waveguide through a suspended substrate low-pass filter on a 76 μm thick quartz substrate. The filter prevents the second and third harmonic power from propagating back to the input waveguide and is a critical element in providing the proper embedding impedances to the varactor at the various harmonics. The output waveguide is cutoff at the fundamental and the second harmonic frequencies. Sliding backshorts in the input waveguide, in its E-plane arm and in the output waveguide as well as the proper design of the low-pass filter provide the possibility of partial optimization of the embedding impedances at the fundamental and third harmonic frequencies.

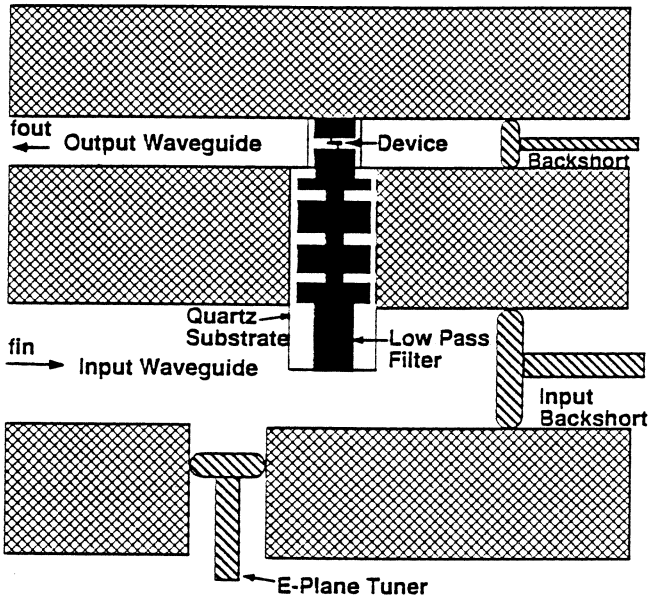


Fig.9 Schematic diagram of the 200 GHz tripler mount

The performance of the assembled tripler was measured using the set-up described in reference [9]. Backshorts and E-plane tuners were adjusted for best performance at each measurement frequency and each pump level. Fig.10 shows the measured flange-to-flange efficiency versus input power for the tripler at 188 GHz. The flange-to-flange efficiency of the tripler reaches its maximum value of 2.9% at 6 mW input power and then begins to decrease as the pump power level is increased.

In order to find out the embedding impedances available at the varactor terminals, a 20 times scaled model of the crossed waveguide mount was constructed.

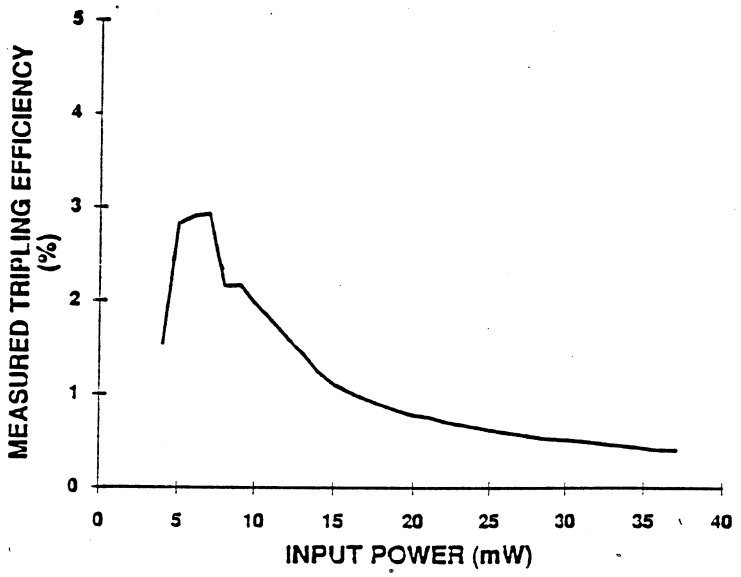


Fig.10 Measured tripling efficiency versus input power plot at 188 GHz.

The embedding impedances at the fundamental and its two higher harmonics were measured for variable mount parameters with HP 8510C vector network analyzer at 3-12 GHz. The end of a miniature coaxial cable (UT 34) was used as a probe to measure the impedances seen by the gap for the varactor diode. This technique is described in reference [10]. According to the measurements, this multiplier mount can provide a perfect impedance match at the fundamental frequency band of 60-70 GHz to any of our bbBNN devices. But, the behaviour of the third harmonic impedance at 180-210 GHz is less optimum. The output embedding impedance as a function of the output backshort position circles around the desired impedance region as shown in Fig.11. At frequencies above 200 GHz, there is a small leakage of the third harmonic signal back to the input waveguide. This is due to the suspended stripline quartz substrate of width of 635 μm which can support a parasitic waveguide mode in the filter channel.

Large signal analysis of the bbBNN device was also carried out with the available embedding impedances of the mount from the scale modeling. The effect of the third harmonic embedding impedances on the tripler efficiency was studied for five different available embedding impedance values obtained from scale model measurements (compare Fig.11). Fig.12 shows efficiency versus input power plots for the bbBNN tripler with the third harmonic embedding impedance of the mount as parameter. The embedding impedance at the fifth harmonic was found to have insignificant effect on the tripler efficiency.

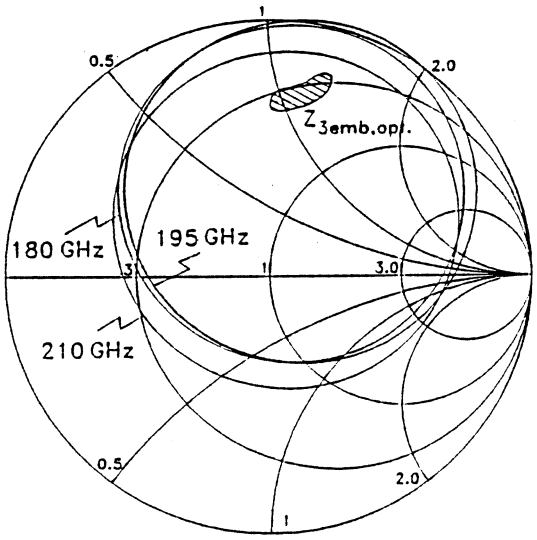


Fig.11 Smith chart showing third harmonic embedding impedances versus backshort positions obtained from the scaled model measurement of the multiplier.

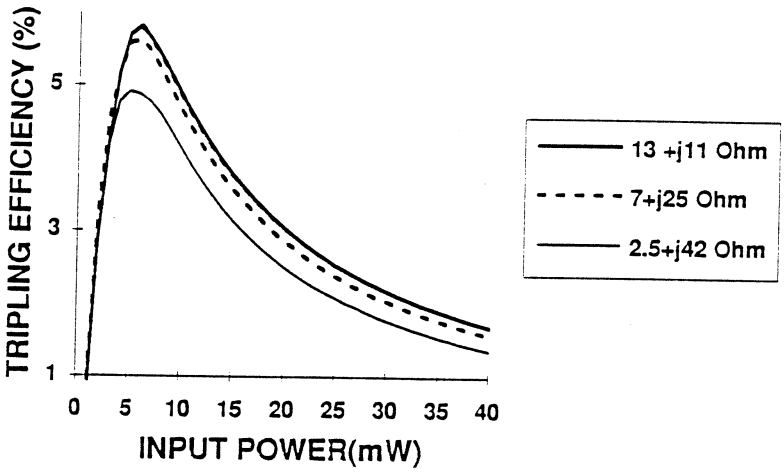


Fig.12 Calculated tripling efficiency to 188 GHz for bbBNN varactor with third harmonic embedding impedance of the crossed waveguide mount as a parameter.

Based on previous measurements of the mount (see ref. [9]), losses in the input and output waveguides and the filter are about 45%. Hence, the measured efficiency at the diode is estimated to be near 6%. This is in excellent agreement with the calculations taking into account the mismatch loss shown in Fig.12.

CONCLUSIONS

At 200 GHz, a flange-to-flange tripling efficiency of 2.9% has been obtained using planar bbBNN devices, with efficiency at the diode of about 6%. This is the first reported experimental result with a bbBNN waveguide frequency multiplier. A new technique has been developed to characterize the C-V curve and series resistance of these devices using automatic network analyzers. Measured device characteristics compare very well with those using other techniques. bbBNN varactor devices are found to have low series resistance compared to BIN devices [11]. Highest possible C_{max}/C_{min} value is also desirable for these devices. High efficiency at low input power levels makes these devices very attractive for submillimeter wave frequency multiplier applications.

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