Heterostructure Barrier Varactors on Copper Substrate for Generation of Millimeter- and Submillimeter-Waves

[1]Lars Dillner, [1]Jan Stake, [1]Stein Hollung [2]Chris Mann and [1]Erik Kollberg

[1]*Microwave Electronics Laboratory, Chalmers University of Technology, SE-412 96 Göteborg, Sweden.*
[2]*Rutherford Appleton Laboratory, Chilton, Oxon, UK.*
Email: dillner@ep.chalmers.se

Abstract:: We demonstrate a fabrication process where heterostructure barrier varactors are fabricated on a copper substrate which offers reduced parasitic losses and improved thermal conductivity. This have been done without degrading the electrical characteristics.

I. INTRODUCTION

The heterostructure barrier varactor (HBV) has received considerable attention as a promising symmetric varactor element for frequency multiplier applications at millimeter and submillimeter wave frequencies [1]. Compared with a Schottky barrier varactor, an HBV simplifies frequency tripler and frequency quintupler circuits and has the ability of epitaxial stacking, which increases its power handling capacity considerably [2]. However, parasitic resistance and limited thermal conductivity decrease the efficiency and the power handling capability of an HBV multiplier [3]. This paper describes a fabrication process which reduces the spreading resistance (part of the series resistance, R_s) and improves the heat sink by replacing the InP substrate with a copper substrate. The benefits of a copper substrate are excellent thermal and electrical conductivities.

II. DEVICE FABRICATION

The structure shown in Table 1 was grown by MBE. A Ti/Pt/Au ohmic contact is e-beam evaporated on the InAs top layer. The chip is then annealed at 200°C to improve the adhesion of the contact. Copper is then plated from a solution based on $CuSO_4$ and H_2SO_4 for 1 hour to a thickness of about 50 μm. For chemical protection, a gold layer is plated on the copper. The InP substrate is etched away in a $HCl:H_3PO_4$ 3:1 solution for about 2 hours (the epitaxial lift-off process (ELO) [4, 5]). The InGaAs buffer layer serves as etch stop layer. The buffer layer is reduced to about 0.5 μm using a wet etch ($H_3PO_4:H_2O_2:H_2O$). Notice that the epitaxial layers now are stacked on copper in reversed order compared with the growth order on the original InP substrate.

Table 1: The material structure. (The structure was originally designed for planar diodes.)

	Material	Doping (cm^{-2})	Thickness (Å)
Contact	InAs	$>10^{19}$	100
Contact	$In_{.53-1}Ga_{.47-0}As$	$>10^{19}$	300
Contact	$In_{.53}Ga_{.47}As$	$>10^{19}$	3000
Modulation layer	$In_{.53}Ga_{.47}As$	10^{17}	2500
Spacer layer	$In_{.53}Ga_{.47}As$	Undoped	50
Barrier layer	$In_{.52}Al_{.48}As$	Undoped	90
Barrier layer	AlAs	Undoped	20
Barrier layer	$In_{.52}Al_{.48}As$	Undoped	90
Spacer layer	$In_{.53}Ga_{.47}As$	Undoped	50
Modulation layer	$In_{.53}Ga_{.47}As$	10^{17}	2500
Spacer layer	$In_{.53}Ga_{.47}As$	Undoped	50
Barrier layer	$In_{.52}Al_{.48}As$	Undoped	90
Barrier layer	AlAs	Undoped	20
Barrier layer	$In_{.52}Al_{.48}As$	Undoped	90
Spacer layer	$In_{.53}Ga_{.47}As$	Undoped	50
Modulation layer	$In_{.53}Ga_{.47}As$	10^{17}	2500
Spacer layer	$In_{.53}Ga_{.47}As$	Undoped	50
Barrier layer	$In_{.52}Al_{.48}As$	Undoped	90
Barrier layer	AlAs	Undoped	20
Barrier layer	$In_{.52}Al_{.48}As$	Undoped	90
Spacer layer	$In_{.53}Ga_{.47}As$	Undoped	50
Modulation layer	$In_{.53}Ga_{.47}As$	10^{17}	2500
Buffer layer	$In_{.53}Ga_{.47}As$	$>10^{19}$	30000
Substrate	InP	S.I.	

After the ELO process, diode mesas of 3, 4.5, 7, 10, 15 and 30 μm diameter are fabricated using standard photo lithographic methods and e-beam evaporation of Au/Ge/Au/Ni/Au/Ti. The titanium serves as etch mask. After anealing at 370°C, diode mesas are etched using a chlorine based Reactive Ion Beam Etching (RIBE) and a wet etch.

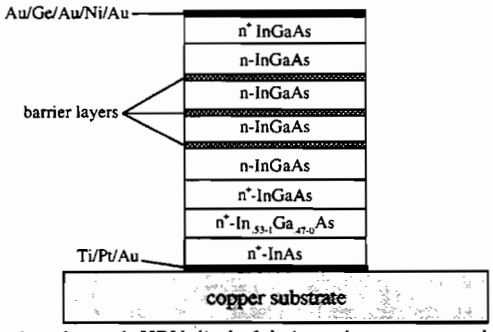

Figure 1: Schematic cross-section through HBV diode fabricated on copper substrate.

To prevent the whisker wire from sliding off the mesa, gold cups were fabricated on top of the mesas using photo lithography, sputtering of titanium and gold, and lift-off. Figure 1 shows the schematic cross-section of an HBV diode fabricated on copper, and figure 2 shows a SEM picture of HBV diodes fabricated on a copper substrate. For comparison, diodes have also been fabricated on the original InP substrate.

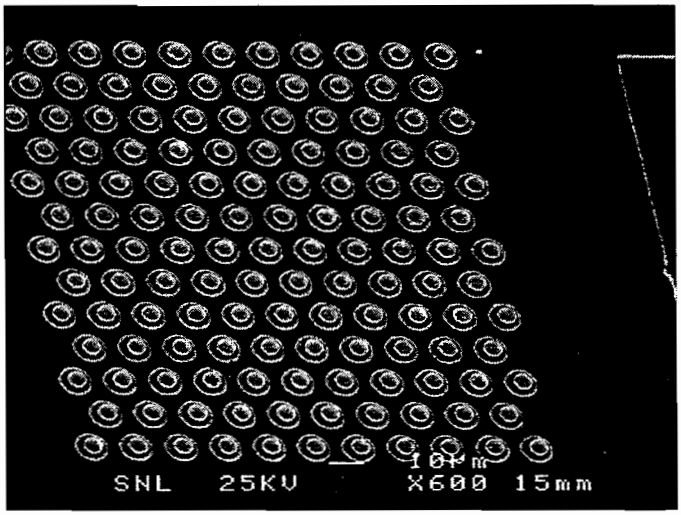

Figure 2: An array of 10 μm HBV diodes fabricated on a copper substrate

I-V and C-V characterization

The conduction current and the capacitance-voltage characteristics of HBVs on copper and InP are shown in figures 3-4. A very small difference in the electrical characteristics of the HBVs on copper and InP can be seen from the figures. This verifies that the

fabrication process does not degrade the epitaxial layers. The measured C-V characteristics are displayed with a C(V) generated by the quasi-static HBV model

$$V(Q) = N\left(\frac{bQ}{\varepsilon_b A} + 2\frac{sQ}{\varepsilon_d A} + Sign(Q)\left(\frac{Q^2}{2qN_d\varepsilon_d A^2} + \frac{4kT}{q}\left(1 - e^{-\frac{|Q|}{2L_D AqN_d}}\right)\right)\right) \quad (1a)$$

$$L_D = \sqrt{\frac{kT\varepsilon_d}{q^2 N_d}} \quad (1b)$$

where N is the number of barriers, b is the barrier thickness, s is the undoped spacer layer thickness, A is the device area, N_d is the doping concentration in the modulation layer, ε_b and ε_d are the dielectric constant in the barrier material and modulation layer respectively, T is the device temperature, q is the elementary charge, and Q is the charge stored in the HBV[3, 6]. With b=200, s=50 Å, N_d=1.15 10^{17} cm^{-3} and N=3, the model agrees excellent with the measured C-V. The measured conduction current density was fitted to the simple empirical expression

$$J_{cond.} = a * \sinh(b * V) \quad (2)$$

with the constants a= 50.3 and b=1.13.

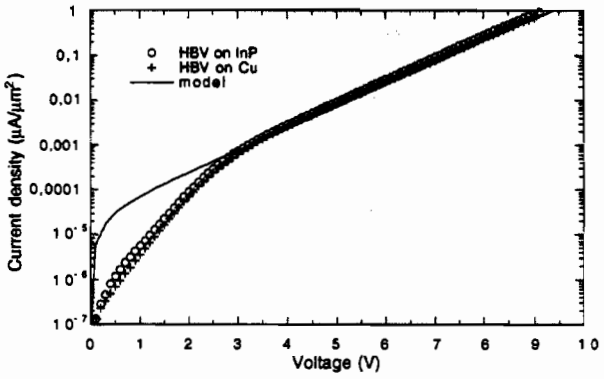

Figure 3: Measured and modeled conduction current density through an HBV fabricated on InP and copper respectively.

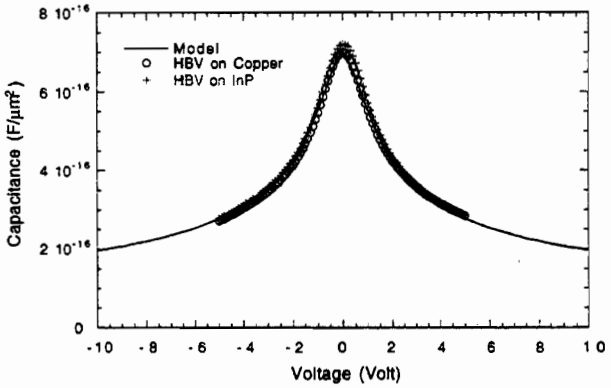

Figure 4: Measured and modeled capacitance-voltage characteristics for HBVs on InP and copper respectively. The C-V characteristic was measured with a LCR-meter (HP4285) at 1 MHz.

Thermal resistance of the heat sink

For heat flow from the diode into a semi infinite heat sink, the thermal resistance can be estimated by

$$R_{T,heat\ sink} = \frac{1}{2d\kappa} \tag{3}$$

where d is the diode diameter and κ is the thermal conductivity of the heat sink material. The thermal conductivity of copper is $\kappa \approx 400\ Wm^{-1}K^{-1}$, to be compared with $\kappa \approx 70\ Wm^{-1}K^{-1}$ for InP and $\kappa \approx 45\ Wm^{-1}K^{-1}$ for GaAs.

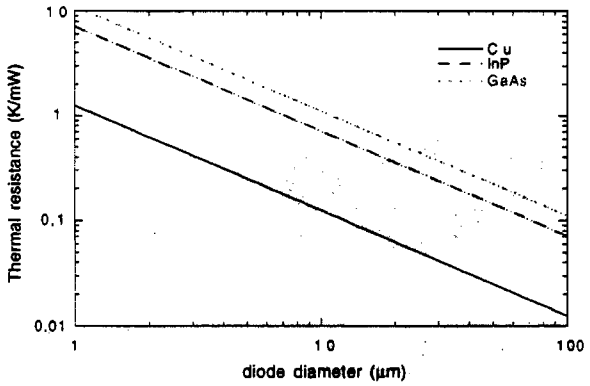

Figure 5: The thermal resistance of copper, InP and GaAs heat sinks as a funktion of diode diameter.

For a complete thermal analysis, the diode mesa and the whisker wire must be included in the calculations [7].

The series resistance

The series resistance is the sum of the resistance of the diode mesa, the spreading resistance, and the ohmic contact resistance. The resistance of the modulation layers, which dominates the mesa resistance, can be estimated by

$$R_{smesa} = \frac{(N+1)t}{\mu N_d q A} \tag{4}$$

were N is the number of barriers, t is the thickness of the modulation layers, μ is the electron mobility, N_d is the doping concentration in the modulation layers, q is the elementary charge, and A is the area of the diode. We have assumed the electron mobility to be 6500 $cm^2/(Vs)$. The specific contact resistance have been measured using TLM patterns to 40 $\Omega\mu m^2$ for the Ti/Pt/Au on InAs contact and 60 $\Omega\mu m^2$ for the Au/Ge/Au/Ni/Au on InGaAs contact. Figure 6 shows the specific contact resistance of the latter contact as a function of temperature. Notice that copper can be anealed at temperatures above 400°C were InP is unstable.

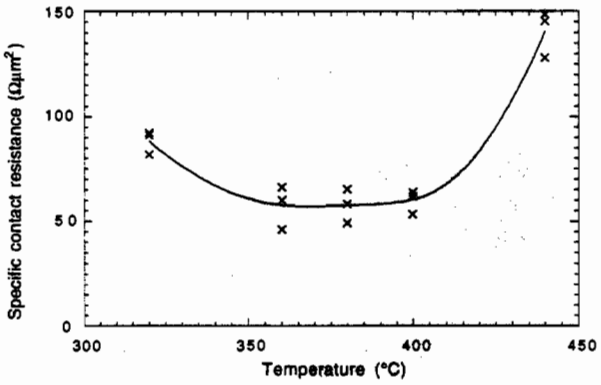

Figure 6 The specific contact resistance of the Au/Ge/Au/Ni/Au on $In_{0.53}Ga_{0.47}As$ contact as a function of temperature.

The spreading resistance at high frequencies can be estimated by:

$$R_{sp} = \frac{\ln(\frac{D}{d})}{2\pi\sigma\delta} \tag{5}$$

were D is the diode chip diameter, σ is the conductivity at the surface of the substrate, and δ is the skin depth. In our case, the substrate surface is covered by gold, platinum and titanium which makes the calculations more complicated. However, for frequencies below 1 THz the skin depth of platinum and titanium is larger then the film thickness (500 Å of titanium and 500 Å of platinum was evaporated). Therefore, the losses in the gold layer and the copper substrate dominates. We have used the conductivity of gold, $4.3\ 10^7$ S/m, in our calculations. The chip diameter, D, have been assumed to be 200 μm. To include effects of surface roughness etc, we have multiplied the resistance from (5) by a factor 2. Table II shows estimated series resistances at DC and 1 THz. If the capacitance is extrapolated to the break down voltage, 9 Volt, and the DC series resistance is assumed, the dynamic cut-off frequency

$$f_c = \frac{1}{2\pi Rs}\left(\frac{1}{C_{\min}} - \frac{1}{C_{\max}}\right) \tag{6}$$

can be estimated to be 2.7 THz.

Table II: Estimated series resistances.

diode diameter (μm)	R_s at DC (Ω)	R_s at 1 THz (Ω)
3	28	29
4.5	13	13
7	5.2	5.5
10	2.5	2.8
15	1.1	1.4
30	0.28	0.46

IV. SIMULATIONS

We have made harmonic balance calculations for frequency multipliers with the described HBV diodes. In the simulations the series resistance, conduction current and capacitance voltage models described above were used. Circuit losses are not included in the simulation and optimum embedding impedances are assumed.

For our harmonic balance simulations to be valid, the velocity for the electrons in the modulation layers may not exceed the saturation velocity, $\approx 2.5\ 10^5$ m/s for $In_{0.53}Ga_{0.47}As$. If an abrupt depletion region is assumed, the current density is given by:

$$J = N_d q v \tag{7}$$

where v is the velocity of the electrons in the modulation layers. Consequently, it is possible to estimate the maximum electron velocity from the current waveform. Table III shows results from simulations of a 250 GHz tripler and a 750 GHz quintupler. The simulations predict 44 % efficiency for the 250 GHz tripler and 10 % efficiency for the 750 GHz quintupler.

Table III: Multiplier simulations of a 250 GHz tripler and a 750 GHz quintupler for HBVs on copper substrate.

Output frequency	250 GHz	750 GHz
Input frequency	83.3 GHz	150 GHz
Diode diameter	10 μm	4.5 μm
Estimated series resistance	2.7 Ω	12.8 Ω
Input power	40 mW	18 mW
Output power	17.5 mW	1.9 mW
Efficiency	44 %	10.4 %
Input impedance	6.0-62j Ω	26-165j Ω
Optimum load impedance	10.5+26j Ω	20+40j Ω
Optimum idler impedance	--	73j Ω
Maximum voltage	8.9 V	9.0 V
Maximum electron velocity	$1.1 \cdot 10^5$ m/s	$2.5 \cdot 10^5$ m/s

V. CONCLUSION

We have demonstrated that HBV diodes can be fabricated on copper substrate without degrading the electrical characteristics. This fabrication process should decrease the spreading resistance and improve the heat sink significantly. Simulations predict very competitive efficiencies for HBV diodes on copper. Another advantage with this fabrication process is that HBV material grown on semi-insulating substrate can be used for whisker diodes, enabling the same material to be used for whisker contacted diodes and planar diodes.

VI. ACKNOWELEDGEMENT

This work was supported by SSF High Speed Electronics program. The authors would like to thank Emmanuil Choumas and Byron Alderman for fruitful discussions.

VII. REFERENCES

[1] A. Rydberg, H. Grönqvist, and E. L. Kollberg, "Millimeter- and Submillimeter-Wave Multipliers Using Quantum-Barrier-Varactor (QBV) Diodes," *Transactions on Electron Devices*, vol. 11, pp. 373-375, 1990.

[2] K. Krishnamurthi, R. G. Harrison, C. Rogers, J. Ovey, S. M. Nilsen, and M. Missous, "Stacked Heterostructure Barrier Varactors on InP for Millimeter Wave Triplers," presented at Fifth International Symposium on Space Terahertz Technology, 1994.

[3] J. Stake, L. Dillner, S. H. Jones, C. Mann, J. Thornton, J. R. Jones, W. L. Bishop, and E. Kollberg, "Effects of Self-Heating on Planar Heterostructure Barrier Varactor Diodes," *Transactions on Electron Devices*, vol. 45, pp. 2298-2303, 1998.

[4] W. K. Chan, A. Yi-Yan, and T. Gmitter, "Grafted Semiconductor Optoelectronics," *IEEE Journal of quantum electronics*, vol. 27, pp. 717-725, 1991.

[5] G. Augustine, N. M. Jokerst, and A. Rohatgi, "Single-crystal thin film InP: Fabrication and absorption measurements," *Appl. Phys. Lett.*, vol. 61, pp. 1429-1431, 1992.

[6] L. Dillner, J. Stake, and E. Kollberg, "Modeling of the Heterostructure Barrier Varactor Diode," presented at International Semiconductor Device Research Symposium, Charlottesville, 1997.

[7] J. R. Jones, "CAD of Millimeter Wave Frequency Multipliers: An Experimental and Theoretical Investigation of the Heterostructure Barrier Varactor," in *School of Engineering and Applied Science*: University of Virginia, 1997.