High Frequency Limitations of Diode Frequency Multipliers[1]

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ABSTRACT

A computer program has been written to investigate the design tradeoffs of high frequency diode frequency multipliers. Velocity saturation and breakdown have been included in a device model that is part of a nonlinear multiple reflection simulation. The device doping, epitaxial layer length and velocity vs. electric field curve are input parameters. The program has a search routine to match the diode input impedance and to optimize the load impedance to maximize the efficiency. The DC bias point choice varies the operation from a resistive to a reactive mode. A useful measure of the operating point is the input Q. Lower Q's correspond to more resistive operation and higher Q's correspond to varactor operation. The input Q also determines the ease of matching and the resulting sensitivity of the circuit design to small changes. This computer program has been used to investigate diode multiplier operation over an input frequency range from 100 to 300 GHz. The results give useful insight into diode multipliers. The optimum multiplier design for power is shown to be different than the optimum efficiency design. The best results at lower frequencies are varactor designs. The designs become more resistive with increasing frequency. The paper will give design details and a physical description of the tradeoffs.

Introduction

Diode based frequency multipliers are critical components in millimeter and submillimeter wave systems. These multipliers are the only convenient source of local oscillator power for frequencies above 200 GHz. The design of multipliers at lower frequencies is well established. A variety of useful design tools have been developed based on harmonic balance or multiple reflection techniques[1, 2]. Commercial software packages are also available[3, 4]. These programs depend on a voltage dependent equivalent circuit to describe the nonlinear device. However, as the operating frequency and RF level increases, these simple equivalent circuit descriptions of the device do not correctly describe the device behavior and a more detailed description of the device is needed. Recently velocity saturation effects have been shown to be important in multiplier operation[5, 6, 7]. Additional effects including the choice of doping level and the resulting breakdown voltage also need to be considered. There are also tradeoffs in choosing a resistive vs. reactive mode of operation. Many frequency multiplier designs use a Schottky diode as a varactor, or nonlinear capacitor, since, at least in the limit of low series resistance, a varactor multiplier can have a high conversion efficiency. A nonlinear resistance multiplier is limited to an efficiency of $1/n^2$, where n is the harmonic number. However, the conditions required for the reactive multiplier can lead to a high Q circuit at the input side of the multiplier. High Q circuits can be difficult to fabricate at high frequencies, are sensitive to small changes to the structure, and can have high loss.

The goal of this paper is to examine the design tradeoffs of high frequency diode multipliers when the effects of velocity saturation, doping, breakdown voltage and the mode of operation are included. A nonlinear multiple reflection code based on a computer simulation discussed by East et. al. [8] that includes velocity saturation effects and diode breakdown has been used. The solution is embedded in an optimization loop that matches the input port and searches the output impedance plane to maximize multiplier efficiency. The semiconductor diode area, epitaxial layer doping and length, carrier velocity vs. electric field and dc bias point are input variables. Since different frequencies and dopings will be compared, the device areas are chosen so that the zero bias reactance at the frequency under consideration

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is 50 ohms. Breakdown effects can also be important under large signal operation. An approximation for the breakdown voltage vs. doping level given by Sze [9] was used. It was also useful to operate the multiplier under constant input Q conditions. The program has an additional loop to modify the bias point in order to keep the device input Q constant. This program was used to investigate diode multiplier operation.

Device Input Q Effects

The input impedance of a multiplier depends on the voltage and current waveforms across the device, which in turn depend on the device structure, the available pumping power and the tuning conditions at the local oscillator frequency and it's harmonics. The input capacitance is approximately the device capacitance averaged over the RF cycle. There are several sources of resistance. In an ideal varactor with a small series resistance, the input resistance would account for power being adsorbed at the pump frequency and "generated" at the output frequency. If the diode is being pump hard enough, there will be saturation effects in the undepleted epitaxial layer that will produce an operating condition dependent series resistance. If the diode is forward biased during a portion of the RF cycle, the thermionic current flow will introduce a shunt conductance across the diode depletion layer. If the diode is being reverse biased enough to breakdown the junction, there will also be a shunt junction conductance. In the multiple reflection code, the nonlinear current and voltage time waveforms across the semiconductor diode are Fourier analyzed to obtain an input impedance that takes all these effects into account.

The relationship between the RF voltage across a diode multiplier and it's input Q can be illustrated with the help of the simple circuit in Fig. 1. The input impedance of the diode multiplier is represented by $R_d - jX_d$. The circuit impedance $R_{in} + jX_{in}$ can be chosen to match the diode in order to maximize the power transfer into the multiplier. The diode Q at the input frequency is

$$Q_d = \frac{X_d}{R_d}. \tag{1}$$

The input match condition gives

$$R_s = R_d \tag{2}$$

and

$$X_c = -X_d. \tag{3}$$

The resulting current flowing in the loop is

$$I_{rf} = \frac{V_{rf}}{2R_d}, \tag{4}$$

and the voltage across the diode is

$$V_d = I_{rf} * Z_{diode} = \frac{V_{rf}}{2}(1 - jQ_d). \tag{5}$$

The RF voltage across the multiplier diode for a given available local oscillator power increases as the input Q increases. This large voltage swing combined with the nonlinear capacitance is the source of the harmonic power. However, the large voltage swing will also increase the saturation effects in the device.

The effect of the input Q on diode conditions is shown in Fig. 2. This figure gives results for a diode with a doping of $5 \times 10^{16} cm^{-3}$ being pumped with an available power of 50 mW. The dashed data is at 75 GHz and the solid data is at 150 GHz. The input Q is varied between 1.5 and 6 by adjusting the bias voltage. Fig. 2(a) shows the DC current vs. Q and Fig. 2(b) shows the bias voltage. Low Q input impedances correspond to low reverse bias voltages and relatively large conduction currents. This is approaching a "resistive" multiplier condition, although the current associated with the forward biased junction capacitance is larger than the conduction current. Since the device Q is $\propto \frac{1}{R_d C_d}$, increasing the Q requires a smaller $R_d C_d$ product. R_d has a modest variation with bias voltage and C_d has a much stronger variation. A six volt bias is needed to raise the Q to 6. The peak voltage of the 75 GHz example varies between 6 and 18 volts, due both to an increasing bias voltage and the Q effect shown in equation 5. The resulting output power in Fig. 2(d) shows the expection variation with Q, increasing from 10 to 25 milliwatts. The 150 GHz example shows strong saturation effects. The series resistance at 150 GHz is higher at 75 GHz. The higher resistance implies a lower capacitance for a given Q value, and thus a larger bias voltage. This is shown in Fig. 2(b). The lower values of dc current in Fig. 2(a) are a result of the larger bias. The peak voltage swing in Fig. 2(c) is 24 volts, near the breakdown voltage of this device. Saturation effect produce a flat power vs. Q curve for 150 GHz operation. This figure shows that saturation effects alter the operation of multipliers, the large tuning dependent voltages are possible across multiplier diodes and that these effects can alter the design tradeoffs in diodes with different matching conditions. These tradeoffs will be discussed in more detail next.

Saturation Effects in Diodes

The results of the nonlinear simulation are discussed in this section. The results are for a doubler with a conjugate match on the input. The second harmonic impedance is adjusted for maximum output power and the remaining harmonics are shorted. The frequency dependent doping and bias effects on multiplier performance are shown in Fig. 3. This figure shows the maximum breakdown voltage limited input power for a diode multiplier for epitaxial doping levels between $5 \times 10^{16} cm^{-3}$ and $2 \times 10^{17} cm^{-3}$ for diode bias points adjusted so that the input Q varies between 2 to 5. The results in Fig. 3a show the effects of velocity saturation and increasing resistance on a low doped structure. The input Q, $\frac{1}{\omega C_d R_d}$ is constant on each line of this figure. The current through the undepleted portion of the epitaxial layer is increasing with frequency. The velocity is saturated so increasing the current increases the resistance. Since the R_d in the Q expression is increasing, the C_d must be reduced to keep to Q constant. This occurs with an increasing bias voltage. This increasing bias voltage reduces the allowed RF voltage swing and thus limits the input pump power with increasing frequency.

Fig. 3a also shows the effect of the input Q or tuning on diode performance. Increasing the input Q reduces the maximum input power. The input Q is increases by increasing the bias voltage. Higher Q bias points will have larger RF voltages across the diode for a given available RF power. Both these effects will increase the peak voltage across the diode and the limit the maximum input power. The peak input power at 100 GHz is reduced from 200 to 75 mW as the Q increases from 2 to 5. The $5 \times 10^{16} cm-3$ multiplier is showing saturation effects over the entire operating range of the figure.

Fig. 3b shows the effect of doubling the doping. Increasing the doping reduces the breakdown voltage and thus the maximum voltage swing, but increases the allowed current density in the epitaxial layer. This combination of effects reduces the maximum power at low frequencies and increases it at higher frequencies. The cross over point depends on the device Q , varying between 230 GHz for the low Q case to 175 GHz for Q=5. Additional increases in the doping shown in Fig. 3 (c) and (d) further reduce the maximum power. These curves are more constant with frequency than the lower doped structures. The epitaxial regions in these higher doped structures can carry the required current without saturation. The resistance remains approximately constant with frequency.

The information in Fig. 3 is only part of the story. The performance of a diode multiplier depends on the output power and efficiency. Low Q input impedances correspond to resistive multiplier operation. Since ideal resistive multipliers are limited to an efficiency of $1/n^2$ and ideal reactive multipliers can have 100% efficiency, we need to investigate the doping and tuning effects on the power output and conversion efficiency.

The performance of a diode multiplier is usually defined in terms of the output power or the conversion efficiency. In cases where there is a large amount of available local oscillator power, the requirement is for the output power to be as large as possible. In other cases, usually at higher frequencies, the available pump power is small, and the multiplier efficiency is more important. These two extremes have been investigated to point out the design tradeoffs for multipliers.

Figure 4 shows the peak output power vs. frequency for diodes doped between $5 \times 10^{16}/cm^3$ and $2 \times 10^{17}/cm^3$ with the input Q as a parameter. These multipliers all show a reduction of peak output power with increasing frequency. The $5 \times 10^{16}/cm3$ structure is strongly saturated for all frequencies and input Q's. Doubling the doping to $10^{17}/cm3$ greatly increases the peak output power at 100 GHz. An additional increase in the doping does not increase the output power. These devices are limited by the reduction in peak input power caused by the reduction in the breakdown voltage with doping. Finally, there is a drop in the peak power as the doping is increased to $2 \times 10^{17}/cm3$ caused by a reduction in the maximum input power. The data in the figure shows a reduction in the peak power with increasing Q. This is related to the limitation of the voltage swing with increasing Q shown in figure 3. These results show that low Q modest doping level devices produce the higher powers.

Figure 5 shows the same structures optimized for peak efficiency. In all cases the pump power required for peak output efficiency is less than the pump power required for peak output power. Here there is a monotonic increase in the efficiency with increasing doping level. Increasing the Q also increases the efficiency. The advantages of a higher Q are greatest at lower frequencies. The Q results converge at frequencies around 200 GHz for the two lower doped examples and around 300 GHz for the two higher doped structures. The information in figures 4 and 5 points out the need for an optimization of the device structure with the end application in mind.

Summary

This paper has given a brief description of design tradeoffs of diode multipliers when the choice of the bias point, and the effects of breakdown and current saturation are included in a nonlinear device circuit simulation. The results show Q and doping dependent effects. High input Q's result in high RF voltages that limit the peak input power of the devices. High output powers are available from lower doped, lower Q conditions. Higher efficiencies with lower output powers are available from higher doping higher Q conditions. The improvements from high Q varactor operation are highest at lower frequencies and are reduced with increasing frequency.

References

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[8] J. East, E. Kollberg and M. Frerking,"Performance Limitations of Varactor Multipliers," presented at the Fourth International Conference on Space Terahertz Technology, Los Angles, California, March, 1993.

[9] Equation 79a on page 104 of S. M. Sze, "Physics of Semiconductor Devices," 2nd edition Wiley, 1981.

List of Figures

Series Resonant Circuit

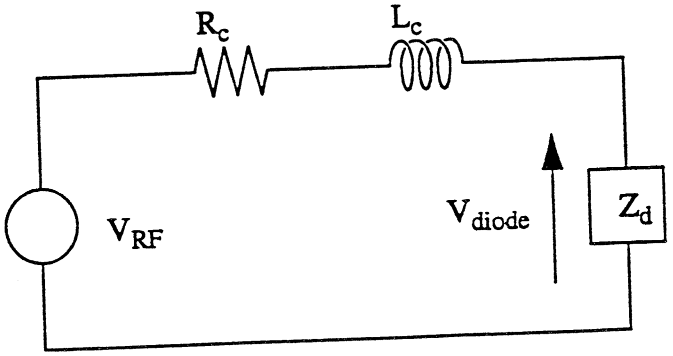
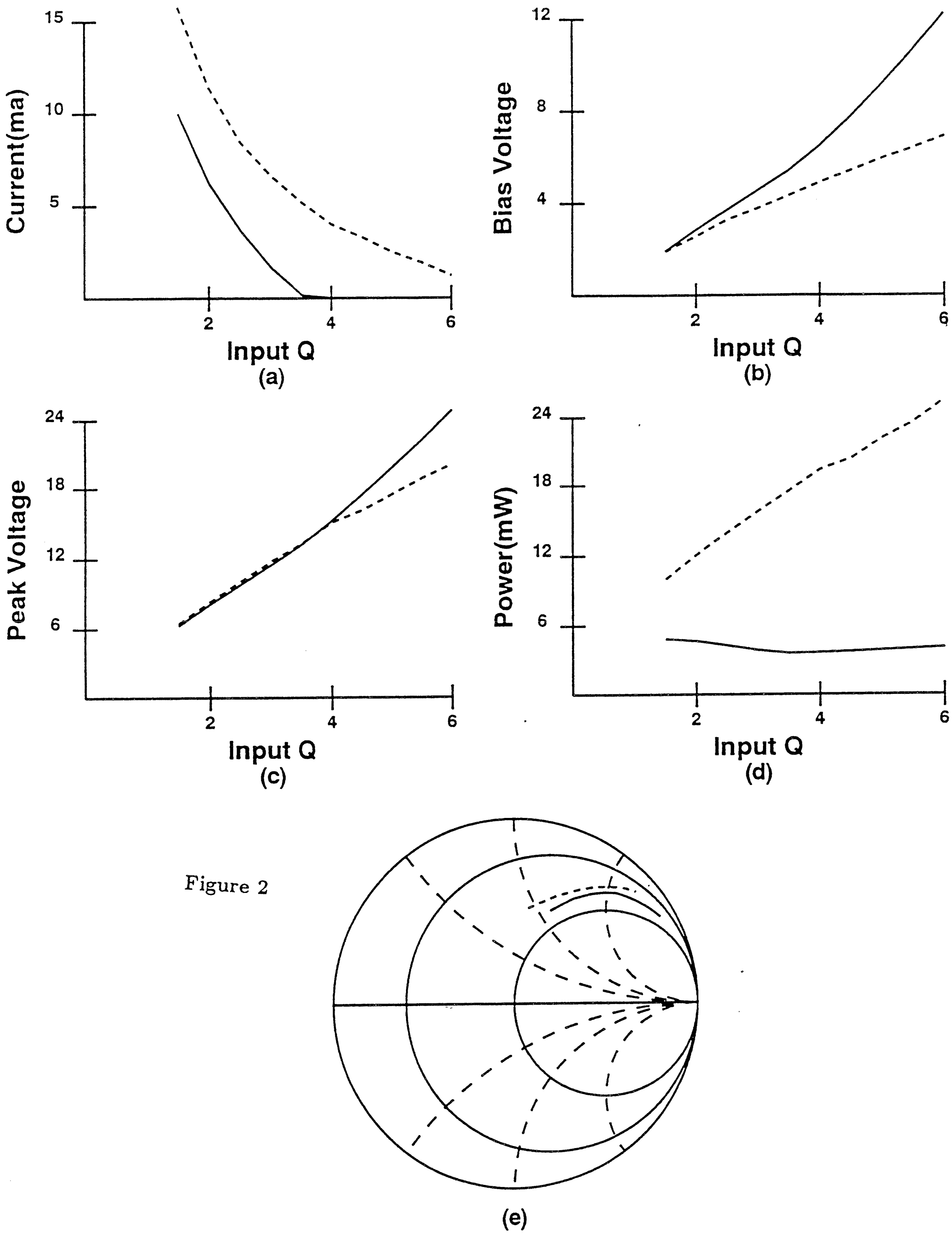


Figure 1



(a)

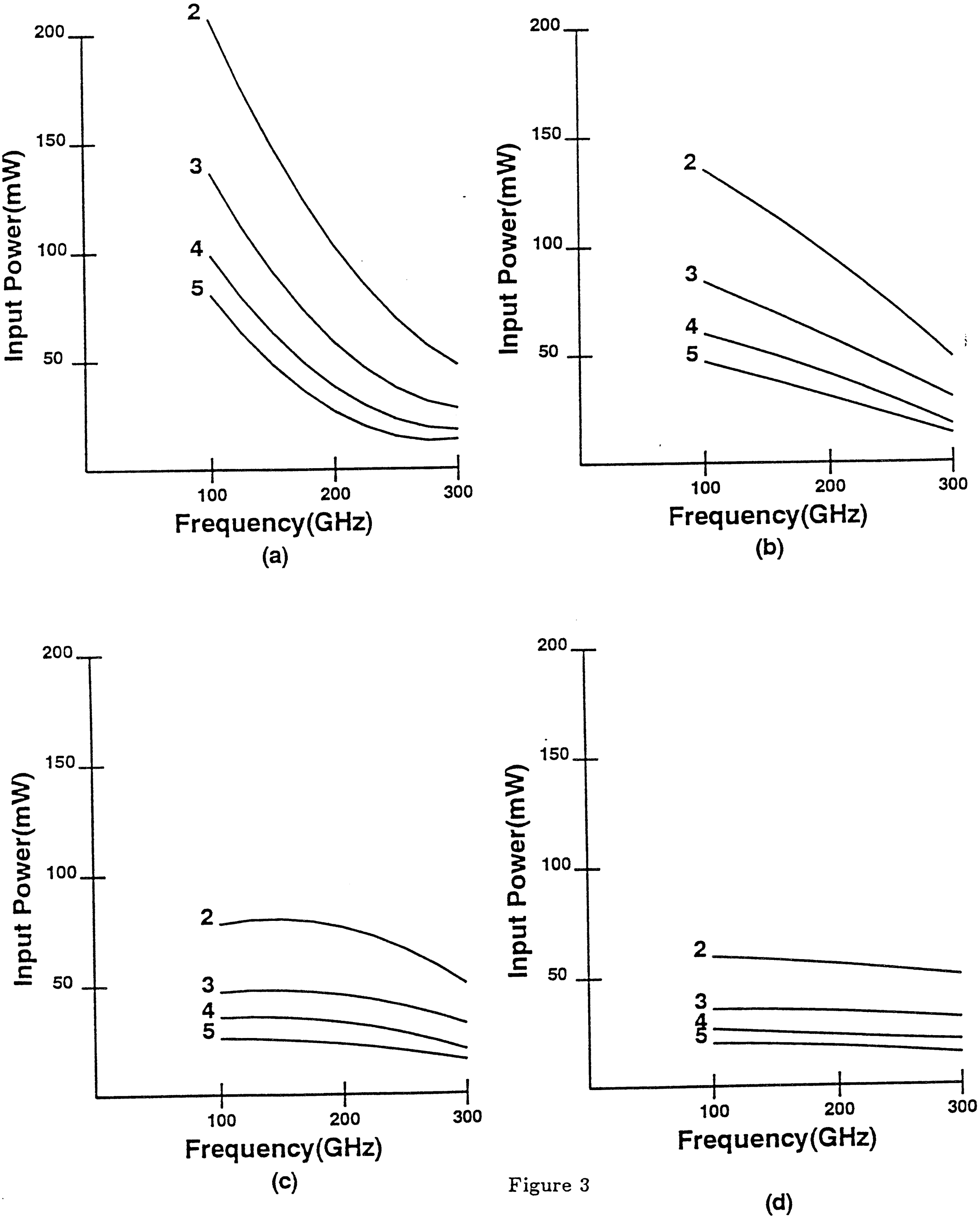
(b)

(c)

(d)

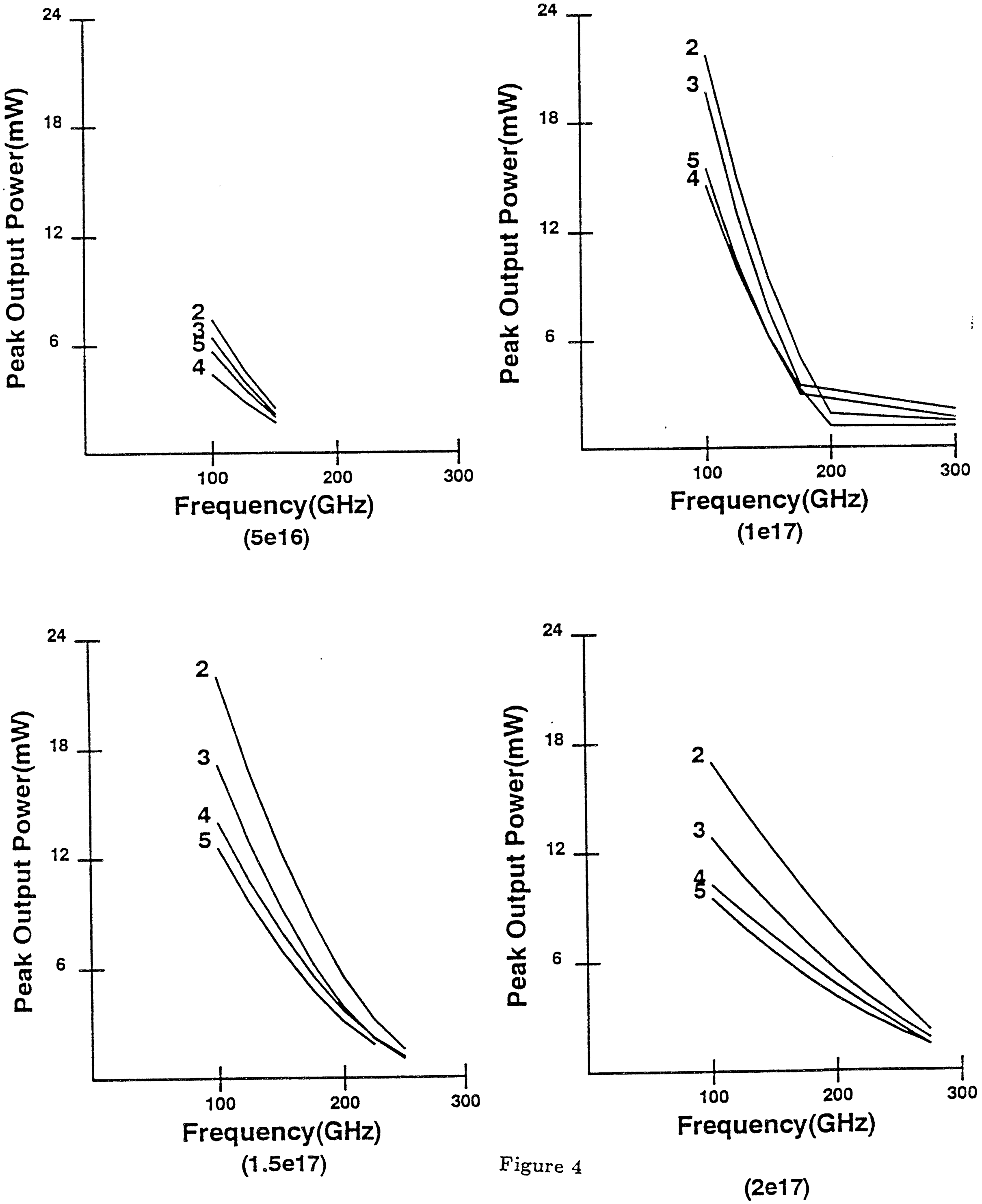
(e)

Figure 2



(a) (b) (c) (d)

Figure 3



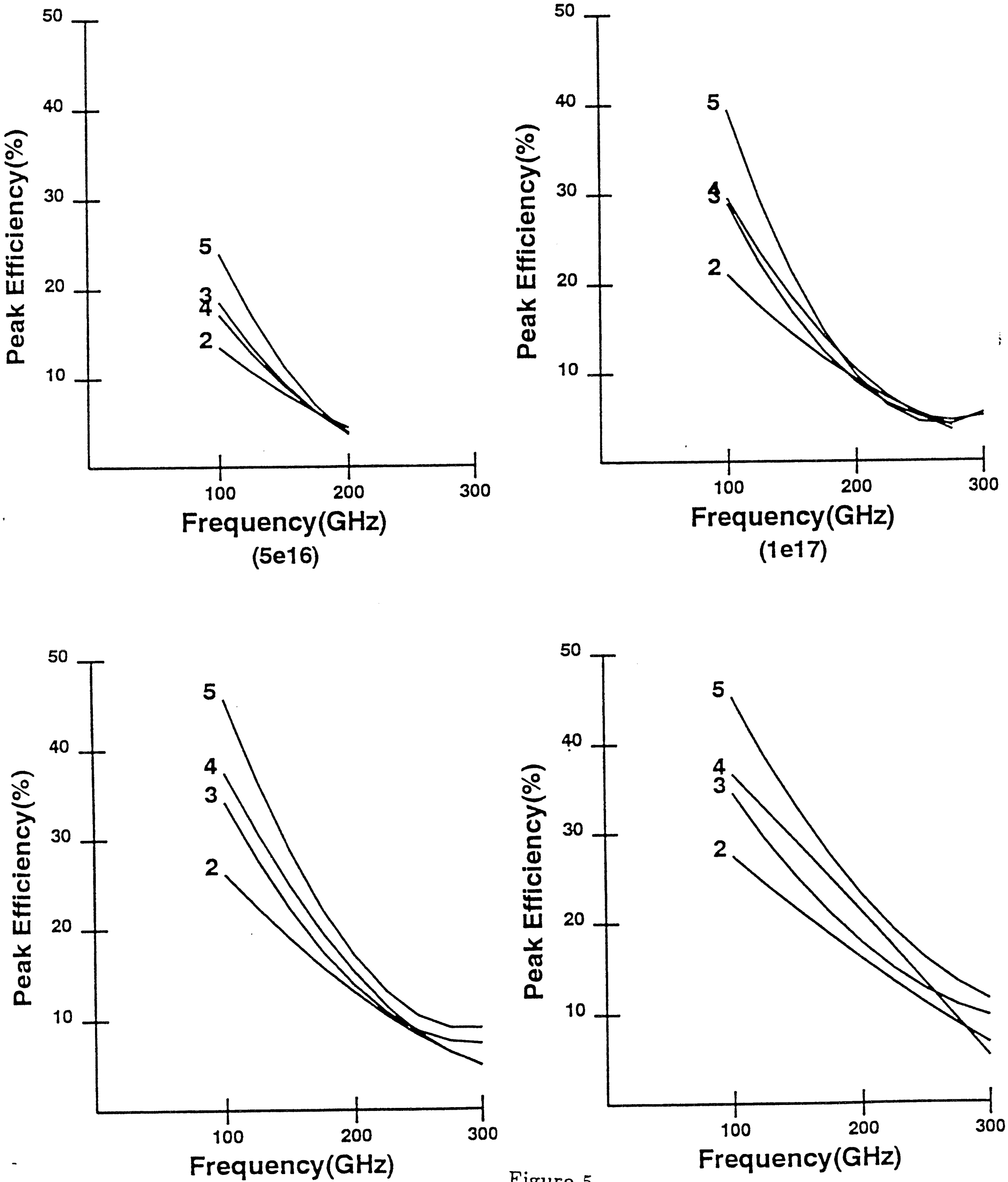
(5e16)

(1e17)

(1.5e17)

(2e17)

Figure 4



(5e16)

(1e17)

(1.5e17)

(2e17)

Figure 5