A High Power Doubler for 174 GHz Using a Planar Diode Array

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ABSTRACT

A balanced doubler for 174 GHz has been built using a planar array of four varactor diodes. The maximum output power is 55 mW, and this power is limited only by the available pump source. The peak efficiency is 25% at 150 mW input, with little saturation at higher power levels. Circuit parasitics due to the chip are not serious, and device heating is not predicted to be large at the present power levels. Higher efficiencies should be possible with minor improvements in the diode parameters.

INTRODUCTION

In the frequency range above 100 GHz, frequency multipliers can achieve high conversion efficiency at low input power, but tend to saturate in output at a rather low output power. The saturation mechanism is believed to be due to the limited carrier velocity in the GaAs epitaxial layer [1], which leads to a maximum displacement current in the varactor. This causes the efficiency to decrease rapidly above a critical power (when the peak displacement current reaches the saturated value), despite the classical prediction of increasing efficiency up to the reverse breakdown limit. Since the current increases with frequency for a given voltage swing, this becomes a major limitation for submillimeter applications. Because the saturated carrier velocity is not easily increased, except in some applications by operating at reduced temperature [2], the only alternative is to decrease the current density, through the use of several diodes or diodes with a larger area. One partial solution has been to build balanced doublers using a pair of whiskered diodes [3], but this is not extendible to larger numbers of diodes.

One of the most attractive approaches is to use series arrays of diodes, because they allow one to increase both the area and the number of diodes, while they may be treated as a single diode so far as circuit design is concerned. In an array having the same impedance level and total power handling as a single diode, the current density varies inversely with the number of diodes. Alternatively, for the same breakdown voltage per junction, the power handling increases as the number of diodes squared. While series arrays are quite impractical using whiskered diodes, they are readily fabricated using planar technology. The doubler described in this work, operating with an output frequency near 170 GHz, uses four planar diodes fabricated on a single chip. It produces two times the output power of a two diode whisker–contacted doubler at a similar frequency, clearly demonstrating the potential for such arrays.

DIODE DESIGN AND CHARACTERIZATION

The doubler circuit used is based on the balanced doubler of Erickson [3]. This circuit was chosen because it operates with very high efficiency, and is also quite simple to fabricate. Thus an initial design constraint was that the chip must fit into this multiplier mount. Diodes for this work were fabricated using the surface channel process [4], with the four diodes laid out as a linear array of discrete devices. The diode is shown in Fig. 1, with

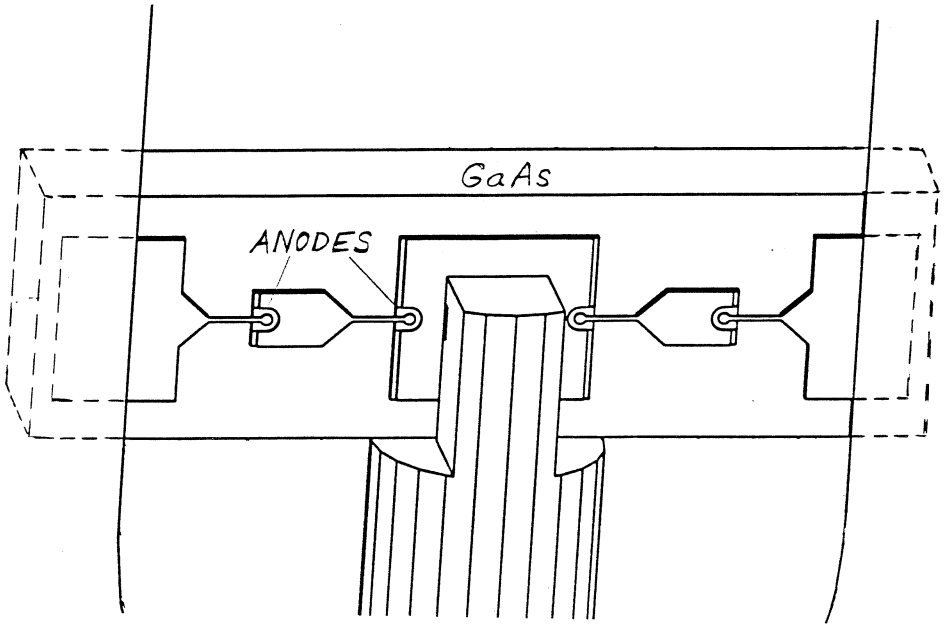

Fig. 1. Planar diode array, showing the method of installation into the circuit. The dashed ends are soldered to the input waveguide walls, while the center pad solders to a pin connecting to the output waveguide. Chip is 800x225x25μm, waveguide is 635μm high.

the connections to the doubler mount at three points. The large central pad serves as the ohmic contact for the two central diodes, as well as the output terminal. The ohmic contacts for the end diodes are the two small inner pads. The end pads are sized to permit the chip to be soldered to the top and bottom walls of the waveguide. In the absence of any detailed knowledge of the device parasitics, an effort was made to maximize the circuit inductance within the chip, since the whiskered doubler worked well with rather long whiskers (0.25 mm of 12 μm wire). After the restrictions of overall waveguide height, ohmic pad size, and central bond pad size were satisfied, the inductive "finger" length ended up being rather short. However, this geometry is easily fabricated and was adopted for initial tests of the concept. The necessity to include inductance within the chip makes planar varactors somewhat tuned to a specific frequency, while the fixed length makes them well suited only for a particular waveguide mount. Thus their advantages over whiskered diodes are partially offset by a reduced flexibility in their application.

The junction capacitance of each anode was chosen to be twice the junction capacitance of a single whiskered diode (U.Va. type 6P2) as used in the earlier balanced doubler [3]. This produces the same total capacitance as that of a single whiskered diode, about 20 fF. Breakdown voltage is less important because it is not the only limitation on useful power input in the presence of current saturation, and in this case, the available pump power required a breakdown voltage of only ~15 V. To optimize the diode parameters, the epitaxial layer doping was increased and the layer thickness decreased to achieve a lower series resistance, with a resulting reduction in V_b per junction, relative to the whiskered diodes.

Diode parameters were measured carefully to compare results with theory. DC measurements of the series resistance of diodes tend to be affected by heating of the junction, which depresses the voltage at the highest current. This lowers the measured resistance, relative to the true value. One way to avoid this difficulty is to measure the voltage immediately following the application of a fast rising pulse, but this requires special equipment. An alternative method is to make small signal resistance measurements at frequencies well above the thermal time constant of the diode using an error corrected vector network analyzer. The resistance of the diode is measured over a range of bias currents and is then fit to a behavior law:

$$R = 1/\alpha I + R_s, \text{ where } I/I_o = e^{\alpha V} - 1,$$

and $1/\alpha I$ is the small signal resistance of the ideal diode junction. The exponential slope, α, is determined from the low current portion of the IV curve measured at dc, leaving only the one free parameter R_s to be determined. In this work, the series resistance of the parallel combination of the two pairs of diodes (equivalent to a single diode) was measured in the doubler mount using an HP 8720 network analyzer at 130 MHz. Small signal (–25 dBm) impedance data were taken over a range of dc bias currents up to 50 mA. The accuracy in these measurements is ~0.1Ω for the lower impedances. The data is shown in Fig. 2, which also shows a line at the best fit value of 6.4 Ω. This contrasts to a dc value of 5.2 Ω. There is evidence for an increase in R_s by about 0.5 Ω at 50 mA (~25 mW per diode), due to heating of the junction, but this should not lead to serious problems at the highest dissipated power levels of 50 mW/jct. The resistance at the lower current values shows an increase due to the amplitude of the test port signal, which is no longer a "small signal" at the lower bias currents. Applying this signal raises the diode impedance below 5 mA, but this bias region is not essential to determine R_s.

The capacitance of each junction was measured over the range 4–10 GHz using a transmission measurement between two Cascade wafer probes, with the transmission amplitude measured with an HP 8510B network analyzer. These probes had two conductors

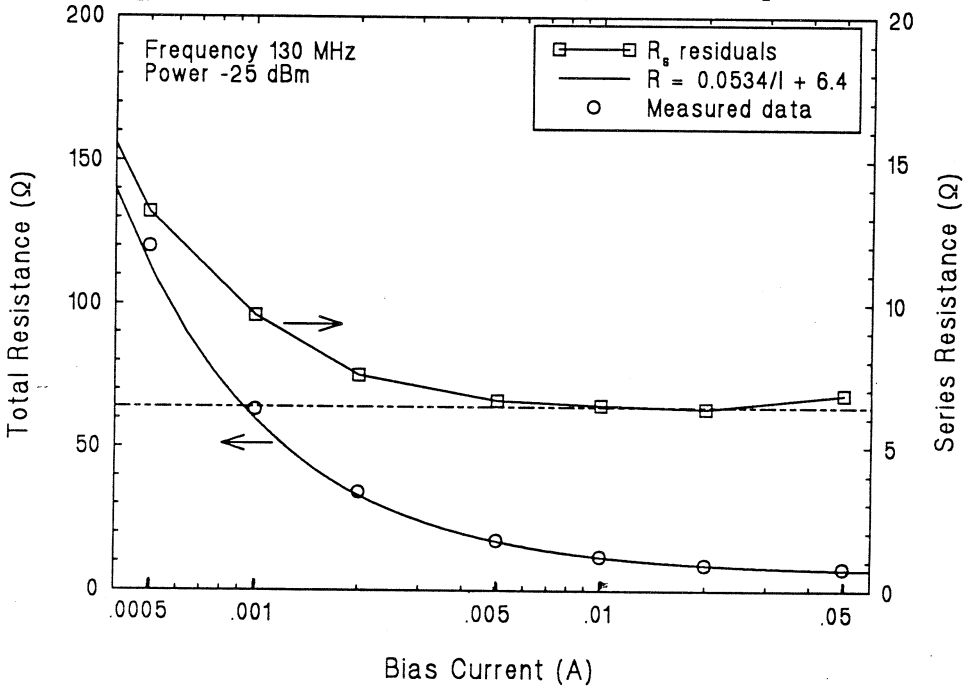

Fig. 2. Microwave resistance vs. bias current for the planar diode array. The lower curve is a fit to the data, while the upper curve shows the residuals after subtraction of the ideal diode resistance. Resistance data below 5 mA is affected by the test signal level. The dashed line is at the best fit value of 6.4 Ω.

(ground and signal) separated by 150 μm. The signal pad of each probe contacted either end of the diode under test while the grounds were connected by a parallel metal strip 30 μm from the diode chip. This transmission mode was used to enhance the accuracy of the pad–to–pad capacitance measurement, which is much less affected by probe self coupling than a single probe shunt determination. The accuracy in this measurement is ±0.2fF. Measurements of a diode with broken air bridges showed the pad to pad contribution to be 9.7 and 11 fF between the pads of the outer and inner diodes respectively. An additional capacitance of 2 fF is found between the inner and outer pads of the series pair. The remaining capacitance, assumed to be due the junction, is 38 fF, varying by ±1 fF for a range of diodes probed. The C/V characteristic of this diode is shown in Fig. 3. This data was then fit to a power law dependence of the form:

$$C(V) = C(0)/(1+V/\varphi)^{\gamma} + C_p.$$

where φ is the built in potential and C_p is a parasitic capacitance adjacent to the anode. The data can be fit by a $\gamma = 0.4$ law assuming $C_p = 0$. As an alternative, the data can also be fit by a $\gamma = 0.5$ law if one assumes that $C_p = 4$ fF. The $\gamma = 0.5$ fit is mathematically better, but there is no way to measure the parasitics very close to the anodes to verify this, and the value seems much higher than the 1–1.5 fF that is estimated from the structure.

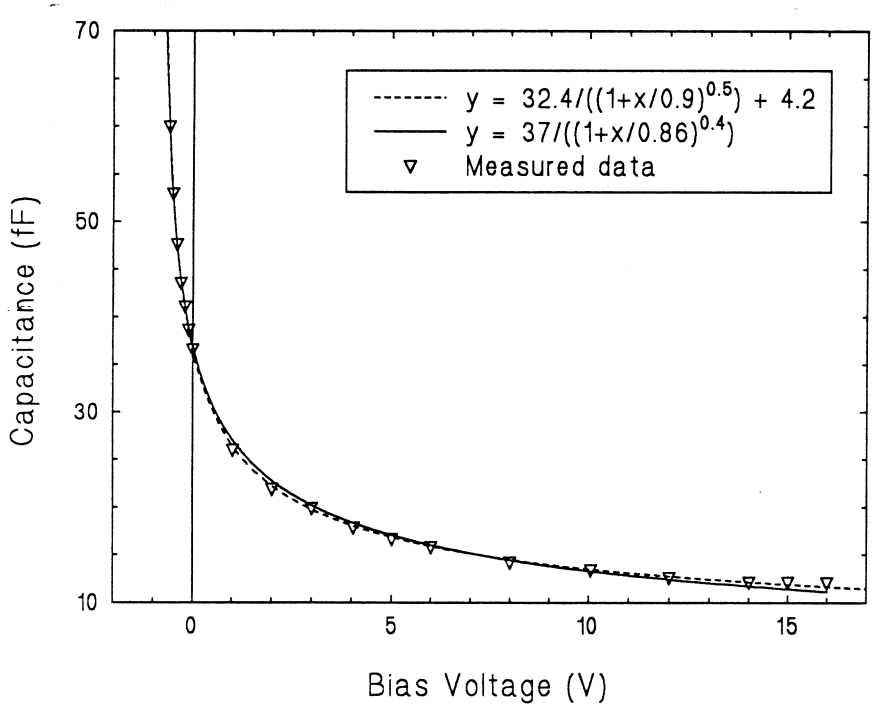

Fig. 3. Capacitance vs. voltage for one anode in the planar array.

The parasitics of the diode in an actual circuit are caused by both the pad to pad capacitance and the circuit loading by the GaAs substrate. In neither case do these cause a loss of efficiency, but they do affect the impedance matching, and the maximum useful bandwidth of a circuit. Pad–to–pad capacitance can be minimized by reducing the ohmic pad area between each series pair. The other three pads become part of the actual circuit and their areas are not critical. It is important to equalize the parasitics for each diode to achieve an equal power balance, and the present chip needs some small refinement in this respect. Circuit loading can be reduced by thinning the substrate, or by substituting a lower dielectric constant substrate such as quartz. This latter substitution would also reduce the pad–to–pad capacitance. However, the high dissipated power in varactors requires a careful study of the thermal resistance of the substrate before this can be done.

DOUBLER MOUNT AND TESTS

The doubler design is electrically equivalent to that in [3], but was redesigned for use with planar diodes. A cross section is shown in Fig. 4. All the waveguides were milled symmetrically about the center line with the coaxial sections milled with a square outer section. The pin connecting to the diode center pad is supported in one half of the block by Macor [5]. The diode is soldered to the waveguide top and bottom walls as well as to the center pin in one operation, in which the entire block is heated to 120 C. The chip is

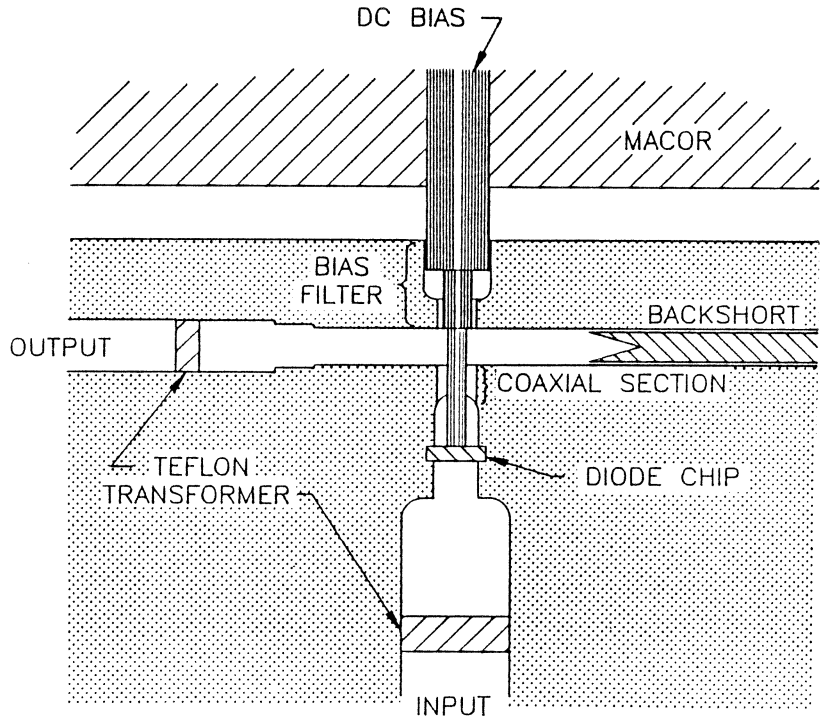

Fig. 4. Cross section through the balanced doubler mount.

unsupported except by the solder joints, but despite its apparent fragility, the structure is robust mechanically. Since the diode is face down in the soldering operation, centering of the contacts is difficult, but is aided by viewing the bottom surface in a mirror in the bottom of the waveguide.

Initial tests were made with an 80 mW Gunn oscillator source at 82 GHz, yielding an efficiency of 21% at 16.5 mW output, but these tests showed that the peak efficiency was at higher power. A klystron oscillator was then used to determine the high power behavior, but this tube produced its maximum power of 250 mW only at 87 GHz. For these tests, the input and output match were optimized using teflon quarter–wave transformers positioned in the waveguide so that the output power was maximized. These transformers can correct a maximum VSWR of:

$$\epsilon(\text{teflon})[\lambda_g/\lambda(\text{air}) \;/\; \lambda_g/\lambda(\text{teflon})]^2 \cong 2.9 \text{ (typically)}.$$

The improvement in power with the addition of the output transformer was only about 10%, meaning that the output match was very good. The input reflected power could be measured with a coupler and was 8% at 87 GHz. Bias voltage at ~250 mW input was 11–12 V, with 0.5 mA forward current. Data for the power output and efficiency vs input power, with the bias optimized at each point, are shown in Fig. 5. This shows that the

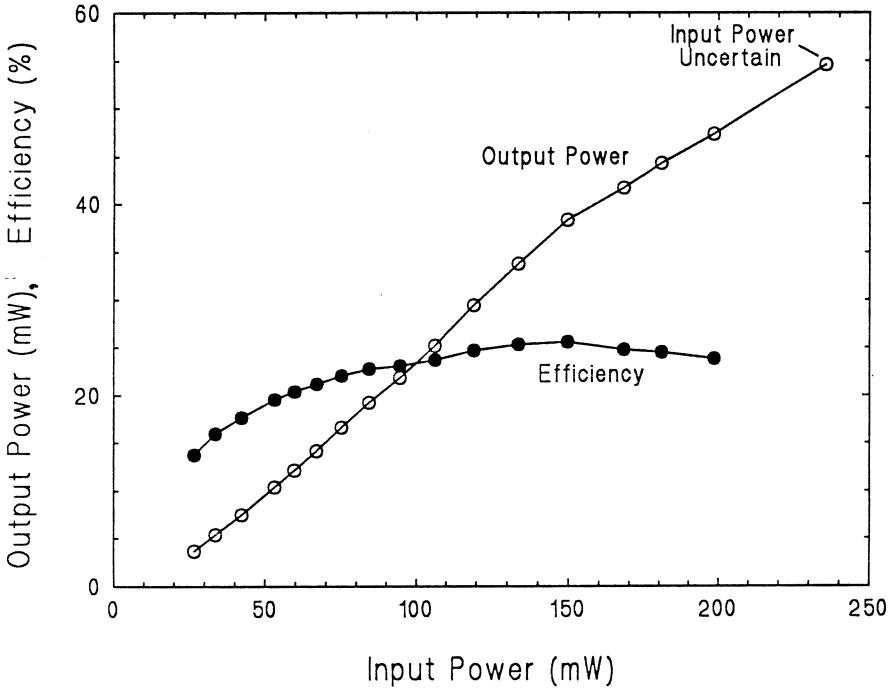

Fig. 5. Output power and efficiency for the planar array at 174 GHz output.

efficiency peaks at ~150 mW input, and has only fallen slightly by 180 mW, which is the theoretical reverse breakdown limit. Thus current saturation appears to have only a minor effect. The peak efficiency is 25% and probably would be 26–27% with a perfect input match.

The peak output power is 55 mW at an estimated input power of 240–250 mW (all other input powers were measured with a directional coupler which was removed for this final test). Input and output power calibrations were obtained with the same calorimeter built in WR–12 waveguide [6]. This maximum output power is over a factor of two higher than the previous best doubler result at a nearby frequency, and may be comparable to that available from any spectrally pure CW source. Fig. 6 shows the comparison of the array with the best previous result using a pair of whisker contacted diodes. The array shows very much less saturation, as well as operation at higher power, but its peak efficiency is lower.

The theoretical efficiency of the diode (assuming $\gamma = 0.4$, $R_s = 7\Omega$, $C_j(0) = 38$fF) is 33% at an input power of 160 mW, corresponding to the measured efficiency peak. This is somewhat less than the breakdown limit of 180 mW. The efficiency predicted for $\gamma = 0.5$ would be 40%, if the excess capacitance of 4 fF is entirely outside the series resistance.

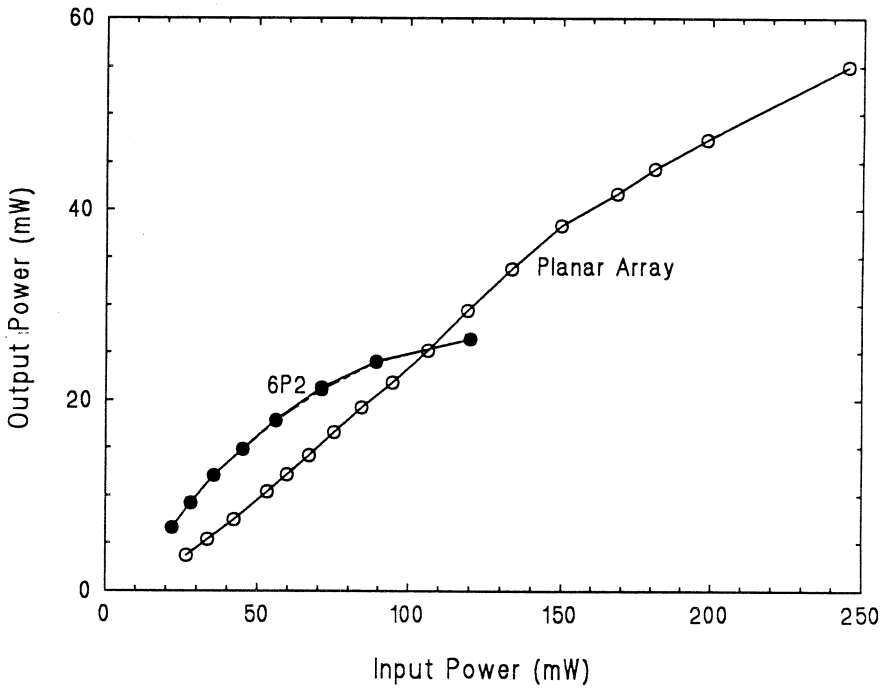

Fig. 6. Comparison of the planar doubler with a whisker contacted model. Planar array data is at 174 GHz, while the 6P2 data is at 158 GHz.

Assuming the former case, then the efficiency is consistent with 1 dB loss within the doubler block. This is consistent with the losses expected for the mount, but is rather uncertain, since there is no way to directly measure the mount losses. The data at the highest power levels is well above the classical reverse breakdown limit, but as is typical for varactors, the efficiency rolls off slowly in this region.

The quality of the impedance match that was achieved is comparable to that with whiskered diodes in the comparable mount, indicating that the parasitics of the planar diode with 25 μm substrate are small in the real circuit. Matching becomes much worse with diodes on 100 μm substrates, so thinning the GaAs appears to be important for wideband applications. This is discussed from a theoretical viewpoint in ref [7] in this same digest. In these high power applications, thermal considerations may prevent much further reduction of the substrate thickness. The thermal resistance of each junction is estimated to be 800 C/W, assuming most of the conduction is through the substrate rather than the metalization, leading to a peak temperature rise of 40 C for the junctions near the center of each span, and somewhat less for those next to the central pad.

CONCLUSIONS

We have demonstrated the first application of a planar array of diodes in the mm–wave range, and have achieved the highest output power from a frequency doubler in the 170 GHz range. The multiplier behavior is largely free of saturation effects, while the efficiency is only somewhat lower than that achieved with whiskered diodes. It appears that higher efficiency should be obtained with this type of diode if a better C/V modulation can be achieved. The series resistance is also higher than for the whiskered equivalent diode, so there is improvement possible there as well. This type of diode array seems well suited for use at even higher frequencies, where current saturation becomes a much more serious problem, and a new diode and doubler are being designed for use at ~300 GHz.

REFERENCES

[1] E.L. Kollberg, T.J. Tolmunen, M.A. Frerking and J.R. East, "Current Saturation in Submillimeter Wave Varactors," IEEE Trans. Microwave Theory Tech., Vol MTT–40, pp. 831–838, May 1992.

[2] J. Louhi, A. Raisanen, and N.R. Erickson, "Effect of Cooling on the Efficiency of Schottky Varactor Frequency Multipliers at Millimeter Waves," Proc. Third Int'l. Symp. Space THz Tech., Ann Arbor, MI., pp 134–145, Mar. 1992.

[3] N.R. Erickson, "High Efficiency Submillimeter Frequency Multipliers," 1990 IEEE MTT–S Int'l. Microwave Symp. Dig., Dallas, TX, pp. 1301–1304, May, 1992.

[4] W.L. Bishop, T.W. Crowe, R.J. Mattauch and P.H. Ostdiek, "Planar Schottky Barrier Mixer Diodes for Space Applications at Submillimeter Wavelengths," Microwave and Optical Technology Lett., Vol. 3, No. 1, pp. 44–49, Jan. 1991.

[5] Macor machinable ceramic, Corning Glass, Corning, N.Y.

[6] B. Vowinkel, "Broad–Band Calorimeter for Precision Measurement of Millimeter– and Submillimeter–Wave Power," IEEE Trans. Instrum. Meas., IM–29, pp. 183–189, 1980.

[7] J. Tuovinen and N.R. Erickson, "Finite Element Analysis of a Planar Doubler," this symposium proceedings.