

A Self-Biased Anti-parallel Planar Varactor Diode

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Abstract

A set of design criteria are presented which are required of varactor diodes for use in practical wideband circuits. These include: high power handling, low in-circuit Q , tolerance to input power variations and reasonably high real impedance. To better meet these criteria, a modified planar varactor diode is proposed, in which the varactor junction is dc isolated from the circuit so that it will self-bias to the correct operating point. The required structure may be made as a simple modification to a conventional planar varactor, by replacing the ohmic contact with a Schottky contact. This diode is ideally suited for anti-parallel operation in tripler circuits. The behavior of the diode in a wideband circuit is discussed, as well as various means to characterize devices which can not be measured at dc.

Varactor Design Criteria

A large number of novel varactor diodes have been proposed recently with antisymmetric CV curves intended for use in tripler circuits [1,2]. In most cases, the design has been based solely on the predicted efficiency in an optimized embedding circuit. Depending on the application there are many possible criteria that may be required for varactor diodes. Not all of these are relevant in every case, but the important point is that there is a lot more to consider than just a cutoff frequency. This list should make it clear that there needs to be a synthesis between the user, the circuit designer and the device fabricator. A particular point which must be made about evaluating the properties discussed below is that the in-circuit behavior of nonlinear devices can not be assessed without the use of a large signal circuit simulator. In the case of back to back devices, this simulation is particularly critical, because the rf pump produces a CV characteristic which may be very different from that measured at dc.

1. Efficiency at a useful power level. For nearly all devices it is easy to make a low power device by simply reducing the junction area. Since this has the effect of raising the effective impedance level, it presents no problem to the circuit designer. High power devices are much more difficult to make. Simply increasing the area will work, but large area diodes have

very low impedances and make matching difficult. Power handling may also be increased by raising the breakdown voltage of the diode, but this also raises the series resistance. Making devices in series tends to be the most effective way to handle high power. Most devices are also prone to carrier velocity saturation at some power level (or frequency) and this must also be considered.

2. Conservative design. Most devices work best near the upper end of their power range, but this should not be right on the edge of destruction. Heat sinking should be a part of the design. The desired input power should not drive the device into breakdown, although rf breakdown appears to be less of a problem than circuit simulators would predict.

3. Wideband impedance matching. The device should have a low Q (ratio of reactance to resistance) at both the input and output frequency for best bandwidth. The in-circuit impedance values must be derived from a nonlinear circuit simulator, and have little relation to R_s and $C_j(0)$. A Q of 3 at the input and 1.5 at the output is typical for a tripler under optimum load, although these Q values tend to increase significantly under nonoptimized conditions. Any higher optimum Q will seriously degrade the performance of full waveguide band multipliers.

4. Reasonably high real part to the optimum embedding impedance. Depending on frequency, this should be at least 25 ohms and even higher for submillimeter devices.

5. Efficiency and impedance level over a reasonable power range. In order to make real multipliers for system applications, there should be at least a factor of two power range for nearly optimum operation, and over this range the optimum circuit impedances should not change significantly.

6. For planar diodes the device package should include enough inductance for matching at the output. The package parasitic capacitance must be very small compared to the average junction capacitance for best bandwidth. While for general applications, a low level of integration on a chip is desirable, a highly integrated approach may be necessary for really wide band circuits.

7. A device with a voltage tunable junction capacitance is very helpful because it may be tuned to fit the mount. A nontunable device forces higher standards on the mount, and this may make fabrication very difficult. The absence of a bias port simplifies the mount and in some applications this may be very valuable.

8. The advantage of antisymmetric devices is primarily in the ease of fabricating triplers with wide bandwidth. In narrow band triplers it is fairly easy to provide the correct second harmonic terminations without much extra complexity. Antisymmetric devices also may permit the fabrication of quintuplers with only one idler. This would be a real advantage in the submillimeter even if the circuit has narrow bandwidth.

Schottky Varactor Advantages and Limitations

In reviewing this list, it appears that the conventional abrupt junction varactor still compares favorably to all other devices considered so far. It is a proven device; high power and efficiency have been achieved with practical planar devices, and moderate bandwidth ($\Delta f/f_c = 0.2$) circuits have been built successfully. Its limitations tend to be of the same sort as with other types of devices, and include the need to provide very different inductances

at the various circuit harmonics, and the need for idlers in higher order multipliers.

One of the primary drawbacks to conventional Schottky varactor diodes has been the need to provide bias to the diode. Under typical operating conditions this bias is $\sim .3 - .4$ times the breakdown voltage, applied in the reverse direction. Providing bias requires dc connections to the diode, with appropriate filtering, adding complexity as well as loss to the circuit. While bias is frequently applied by an external voltage source, under sufficient drive power a varactor will develop enough forward current flow to self-bias given the proper dc load, which is typically a high impedance.

In some cases such bias connections are only a minor problem, and may be incorporated somewhat naturally into the circuit. One such case is the balanced doubler [3], in which the pair of diodes have the same polarity with respect to the coupling line to the output circuit, and in which it is fairly easy to decouple the rf output from the bias. In other cases, the need for bias complicates the circuit sufficiently to make it quite difficult to implement.

The balanced tripler using an anti-parallel pair of diodes is a particularly good example of this problem. This circuit is quite desirable because it produces odd harmonics only, but the parallel connected diodes must be provided with equal and opposite bias. This means that while they are rf connected they must be dc isolated, and that two separate bias ports must be provided. While practical circuits may be built, they are complex and require split or overlaid rf lines to introduce bias, and such circuits become very difficult to build in the submillimeter range. Because this circuit is free of even order harmonics, and because the required second harmonic idler current circulates within the loop of the two diodes (independent of any external circuitry), it is particularly suitable for wide band triplers. It has little advantage in narrow band applications, in which a single diode can work very well, and bias circuitry is not very complex.

Planar Diode Modifications

This paper suggests a rather simple modification to the processing of planar varactors which can provide internal bias to the diode, so that the dc terminal voltage is zero yet the varactor operates at optimum bias. The basic concept is to add a second diode with the opposite polarity in series with the varactor, as shown in Fig. 1. This second diode has a very large area relative to that of the varactor, so that its effect on the rf circuit is negligible,

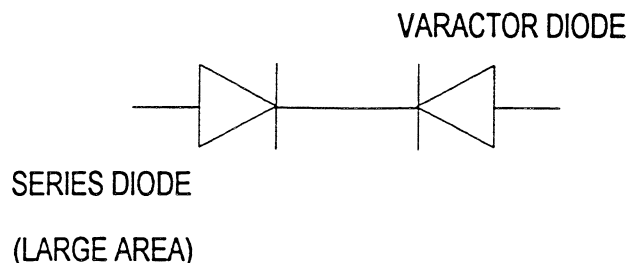


Fig.1. Varactor diode with large area diode in series to allow varactor to self-bias.

but it changes the dc behavior of the circuit. Assume that the dc voltage across the pair of diodes is constrained to be zero. With rf power applied, initially both diode junctions are at zero bias. The rf voltage across the varactor can cause forward current flow only, so the charge on the terminal between the diodes is depleted, and the varactor becomes reverse biased. Since this reverse biases the second junction, no charge can return via this route, either. This second junction has negligible rf voltage across it because of its high capacitance. Eventually, the reverse bias voltage reaches a steady state when nearly the entire rf voltage swing across the varactor is in the reverse direction. One extreme is at a small forward voltage to just balance the reverse leakage. The operating point which is achieved is almost optimal for varactor operation, because the bias seeks the point where no forward current flows. If the rf power continues to increase, the voltage swing will eventually reach reverse breakdown. At this point the bias will stabilize at the point where equal forward and reverse currents flow. This is not necessarily desirable, because typical varactors can not handle significant reverse current flow. It is also hard to predict the exact power level where this will occur, so there is no easy way to avoid over driving the diode.

It is preferable to operate the varactor with a fixed voltage bias, which is chosen for optimum performance at a given power level, and which keeps the circuit working in a similar fashion over a range of power. If this voltage is set to about $0.35 V_b$, then optimum pump will fully modulate the diode between forward conduction and reverse breakdown, while the reverse current will increase slowly for higher power levels, since the voltage swing instead is forced to go into forward conduction. It is easy to achieve this constant bias operation by causing the series diode to have a breakdown voltage of $\sim 0.35 V_{b(\text{varactor})}$. This diode will begin to conduct at this voltage and will let charge back into the isolated terminal, preventing it from going more negative. Except that this diode is internal to the circuit, the behavior is the same as that with an external bias zener diode.

It is remarkable that the structure required to achieve this behavior is very easily built. It can be made with only a small modification of the standard processing involved with a planar varactor. Consider the typical planar diode shown in Fig. 2. The junction itself is a small metallized pad on top of a thin moderately doped epi-layer, which is in turn on top of a heavily doped, highly conducting layer. This active junction is surrounded by a much larger metal pad which is connected to the highly doped layer through an ohmic contact. The ohmic contact is a graded junction which is made by thermally diffusing a high concentration of carriers into the semiconductor in such a way that no barrier is created, so that the metal

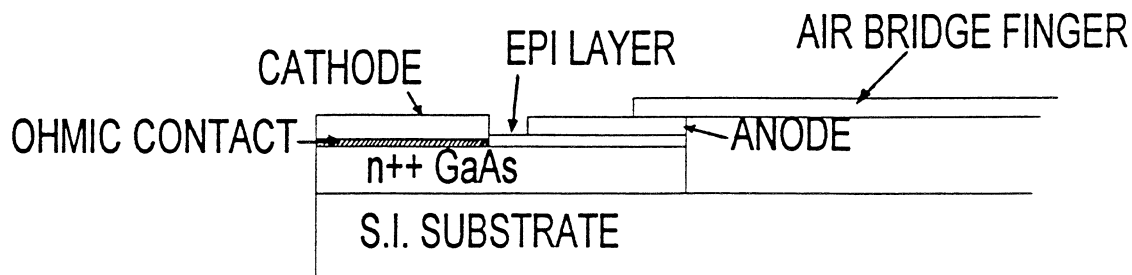


Fig. 2. Typical planar diode cross section.

pad is effectively connected to the highly doped layer. Ohmic contacts are a limitation to the fabrication of planar diodes because they require a minimum area to achieve a sufficiently small resistance, and creating them is a somewhat poorly understood process. Ohmic contacts have traditionally been required on all diodes, because the usual application has been in mixers, where substantial bias current must flow, and where intermediate frequencies may be very low compared to the signal and LO frequencies. This method of fabrication has been carried over into varactor diodes without much consideration as to whether it is still necessary.

If the ohmic alloying step were eliminated, the large area junction would become a second Schottky diode, creating the situation described above. If nothing else were done, this junction would have the same breakdown voltage as the varactor, and the questions about the operating bias would remain. However, the epitaxial material may be thinned so that this junction breaks down at a lower voltage, and this thinning is very easily controlled, since this type of processing is used in all diode fabrication. It appears that this new structure would be nearly ideal, except that the I/V curve of the varactor can no longer be measured at dc. This may not be entirely bad, since dc characterization frequently is misleading, although it does serve as a convenient means to screen out really bad diodes. There are a number of ways to measure R_s at microwave frequencies, and one possible probe configuration is described later.

This diode still requires a dc connection between the terminals to maintain them at the same voltage. This occurs naturally in some circuits, so it is not always a problem, and in the case of the antiparallel diode tripler, the diodes provide their own dc connection. This is because the internally developed bias currents have opposite polarities, and thus flow entirely within the loop formed by the two diodes. Assuming that the diodes are identical, they receive equal power from the pump, and so the bias currents will be the same. In this ideal case, the end terminals remain at the same voltage. The bias remains stable against reasonable variations in diode parameters. Even if one diode is larger and receives more of the input power, the voltage swing across it will be the same as that of its mate. Thus reverse breakdown through the bias diodes begins at the same power level, but the current through the larger varactor increases faster. This current imbalance forces the bias voltage on the larger diode to increase, and that on the smaller one to decrease until the currents are in balance. This situation is stable because with this distribution of voltages the larger diode is driven to lower capacitance, while the smaller diode is driven to higher capacitance, and the power coupled tends to become more equal. The final state will have some voltage across the terminals, which is not inherently bad if it is small relative to V_b .

Requirements for the Bias Junction

We now need to define the actual requirements for the bias junction. The most important is its capacitance relative to that of the active junction. From a circuit standpoint, the bias junction should have a reactance very small relative to that of the active junction so that it does not raise the Q of the varactor circuit. This is particularly important for wideband applications. This requires that the bias junction at reverse breakdown have a capacitance ~ 30 times that of the time averaged capacitance of the varactor. Typical varactors have a

time averaged capacitance 0.4 times $C_j(0)$, while the rather thin bias junction is biased to its minimum value. For such a thin junction this is not much less than that at zero bias (let us assume $\sim 0.7 C_j(0)$). Then to maintain a factor of 30 ratio, the area of the bias junction should be ~ 17 times the varactor area, which is a very modest constraint.

A second constraint is that the bias junction must be able to carry enough current in breakdown to stabilize the bias without being damaged in the process. While some multipliers operate with very low bias current, this is not the rule, and particularly in the case of very wideband devices, best operation tends to occur with ~ 1 mA of bias current. The reason for this is that operation slightly into the forward bias region lowers the time averaged reactance of the diode, lowering its Q , while the power lost in the bias circuit is not serious for a current of up to ~ 1 mA. This bias current is really only this large at relatively low frequencies (< 150 GHz input), and will become smaller as less input power is available. There is little data on the ability of Schottky diodes to carry continuous avalanche currents, and the damage usually occurs at areas of current concentration. It is routine to test the breakdown of $1\mu\text{m}$ diameter diodes at $1\mu\text{A}$ without apparent damage, so in principal, a $30\mu\text{m}$ diameter anode should be able to carry $\sim 1\text{mA}$. However, the fabrication of diodes to carry this current safely may require special care in processing.

These constraints appear to be less restrictive than the present requirement for the area of ohmic contacts, and have the advantage that the required area drops with increasing frequency. This is particularly important in the submillimeter, because ohmic contacts of the conventional size become inconveniently large even by 300 GHz.

Measurements of Diode Properties

It is essential to have some means of testing diodes outside of the complete circuit. Without independent tests, there is no way to determine how well the circuit is actually performing. Diode pairs present problems in isolating the quality of the individual elements, while the dc isolated diodes proposed here present additional problems. Let us first consider the problems in characterizing single diodes with dc isolation.

Measuring capacitance is little different than with conventional diodes. Since the bias junction is so large, it may be ignored in the capacitance measurement. Its only effect is to add its forward voltage to the total voltage across the device in the measurement of the C/V characteristic. The bias junction becomes reverse biased when the varactor is forward biased, but by using current bias, the forward region may be safely measured.

The series resistance is critical, and can not be measured at dc through the bias diode since its breakdown characteristic is not well known, and this junction may not be able to handle sufficient current in any case to permit accurate determination of R_s . This leaves rf measurements as the only practical means. This is a problem for on-wafer tests, so some diodes on a wafer could have ohmic contacts in order to check the process. In principal, the complete diode parameters can be determined through one port measurements using a vector network analyzer with conventional 50Ω wafer probes at some high microwave frequency, but in fact, the accuracy will be poor because the impedance is so highly reactive. It is essential to tune out the reactance of the diode in order to achieve reasonable accuracy. This could be done by adding an inductance at the end of the probe line, or by otherwise modifying the

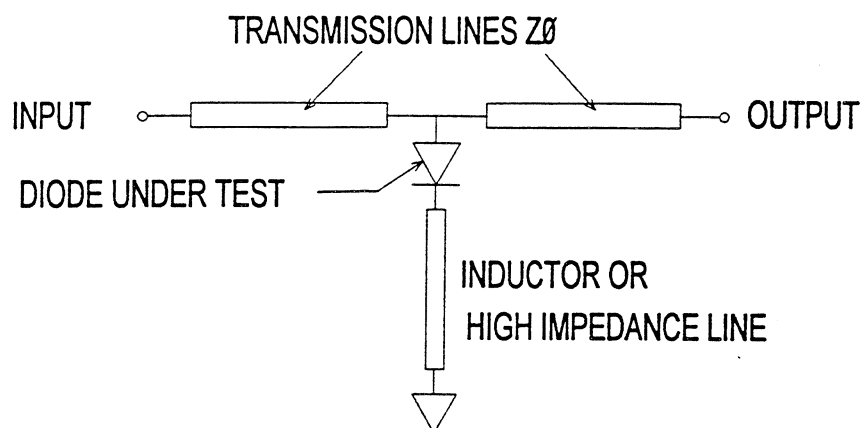


Fig.3. Schematic diagram of DeLoach fixture for testing varactor diodes.

probe to improve the match into a capacitive load.

One variation on this approach is the DeLoach fixture [4], in which a diode plus a suitable inductance are placed in shunt across a transmission line, as shown in Fig. 3. The frequency is swept over a wide band, and one measures the transmitted power on the resonance of the diode with the circuit, where it best shorts out the line. Any parasitic capacitance of the diode will somewhat alter the measured resistance, and require some interpretation of the data. While such measurements may require some special test fixtures, they have the advantage that R_s may be measured at a high enough frequency to be meaningful for predicting performance. In fact, a fixture in the 75-110 GHz band seems quite practical, and has the advantage that the diode is measured at a frequency near that of its actual use.

Evaluation of Anti-parallel Diodes

Anti-parallel diodes present special challenges in measurement, in order to determine the match between the properties of the diodes. The average resistance and capacitance at zero bias may be measured exactly in the way that they would be for a single diode. The match in properties may be determined if the measurement is made with bias applied with opposite polarities at a level sufficient to slightly forward bias each junction in turn. In measurements of R_s with a DeLoach fixture, this bias causes the capacitance of one junction to be much larger than that of the other, so that its resistance dominates the measurement. Some modeling is required to interpret the measurements, but the needed data is available.

The match in junction capacitance may also be derived from these measurements, using the change in resonant frequency with bias, but the same data may be as easily obtained with conventional capacitance bridge measurements. The total capacitance of the pair can be measured and a correction for fringing fields applied by measuring a sample with broken contact fingers. The interpretation of this measurement requires some modeling. There is no way to accurately measure the capacitance-voltage characteristic of the pair since the voltage distribution across the series diodes is not uniquely determined except for a bias voltage high

enough to breakdown one of the bias diodes, and in this case the capacitance is dominated by that of the forward biased diode. The interesting capacitance in the reverse direction is poorly measured, but can be measured at the batch level by breaking the contact finger on one diode of the pair.

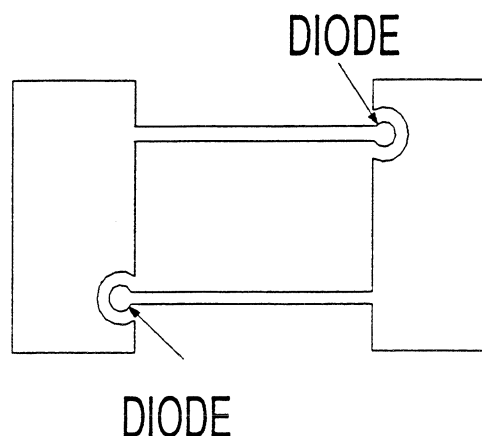


Fig. 4. Simplest circuit for a pair of varactors connected in anti-parallel.

Circuit Requirements for Tripler

All varactor circuits require inductive terminations at all harmonics, with the effective diode capacitance nearly the same at all harmonics. If the optimum inductances at the first three harmonics are defined as L_1, L_2 and L_3 : $L_1 = 4L_2$, and $L_3 = 0.44L_2$. The second harmonic currents are critical to operation of a tripler, so the idler inductance must be near optimum. Since the optimum real parts of the input and output impedances are less than their respective reactances, providing these correct inductances is also critical.

A major design challenge is to include enough inductance for the idler without increasing the circuit reactance at the output. Since the idler currents with anti-parallel diodes circulate in a loop, this loop must have the correct inductance. The simplest circuit shown in Fig.4 has problems in this respect. In this circuit, the mutual inductance of the parallel lines causes the inductance for odd harmonics to be greater than for even. To minimize this effect, the lines must be widely separated, and providing this separation in a microstrip or stripline environment is impossible. If the situation is accepted, then it is necessary to add capacitance in series with the output to tune out the excess capacitance, which decreases the circuit bandwidth. If we reverse the direction of the coupled lines, the situation changes. Now the inductance for odd harmonics is less than for even, and it becomes possible to provide optimized second and third harmonic reactance simultaneously. However, the circuit realization is not simple, as shown in Fig. 5. This layout requires a crossover, and extensive analysis in order to work out a feasible geometry. A preliminary study shows that such a layout is practical, but further work is required.

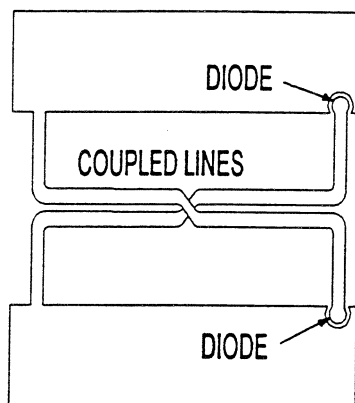


Fig. 5. Anti-parallel diode pair using mutual inductance of coupled lines to increase second harmonic inductance.

Conclusions

A modified construction of a planar diode is presented which eliminates the need for an external bias circuit for varactor applications. This diode must be tested at microwave frequencies, but various means are available to do this. The new diode is particularly well suited for anti-parallel operation in tripler circuits, but a suitable circuit still needs to be developed.

Acknowledgments

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