Planar Frequency Doublers and Triplers for FIRST

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Introduction

Local oscillator sources based on frequency multipliers appear to be the best developed of several types of sources needed for astronomical missions from airborne and space platforms. These applications extend well into the submillimeter range, potentially up to 2.7 THz for FIRST, and similar frequencies for SOFIA receiver systems. A new generation of frequency multipliers is needed for the FIRST mission, in which the old technology of whisker contacted varactor diodes is replaced with new planar devices. This use of planar devices should go well beyond replacement of the diode itself, and should replace much of the circuit used in the earlier devices. The goal is to make these sources far superior to present multipliers in cost, and performance. Desired properties include:

- High reproducibility
- Wide bandwidth with no mechanical tuning
- Easy machining and assembly
- High efficiency, better than the best whiskered designs.

Given that the frequency range for FIRST covers 480-2700 GHz, with nearly full coverage, and the required driver stages cover 140-225 and 280-450 GHz, this multiplier development will essentially fill in the submillimeter range with sources. For purposes of FIRST these sources must cover 10-15% width bands, although wider bandwidths should be possible using the same technology. Progress toward this goal to date is very encouraging although a lot remains to be done:

- Planar diode arrays have produced very large amounts of power, sufficient to strongly pump a following stage.
- A doubler for 185-203 GHz has been completed using a full planar style of construction suitable for fabrication as a MMIC.
- A tripler prototype for 220-275 GHz has been built of nearly full monolithic construction.
- Designs for many other frequencies in the required bands are complete (and some devices fabricated), although the actual complete multipliers have yet to be built.

Balanced Doublers for 140-210 GHz

The initial development in complex planar diodes was the balanced doubler using series diode arrays. These circuits began as an outgrowth of circuits based on whiskered diodes, and only recently have begun to look like truly planar circuits. So far the highest power and best bandwidth produced has been with a hybrid circuit using a 6 diode array in a circuit using gold ribbon and coaxial components [1]. This circuit was designed to tune 142-158 GHz, which is one of the

required FIRST driver bands. Planar arrays from both JPL and UVa have been used in this circuit with somewhat different results. These arrays are of nearly the same layout and are designed to produce an equal power split among the diodes. The JPL diodes (PBD150) use relatively low doping ($10^{17}/cm^3$) and have a breakdown voltage of 13V per diode. The UVa diodes (SB7T1) use higher doping ($2x10^{17}/cm^3$) and have V_b of 7 V per diode.

With the JPL diodes, the efficiency peaks at 200 mW input (140 GHz output), and is 26% at room temperature. The efficiency was tested at 80 K where it increases to ~39% (a 50% increase). This cold test was done with 280 mW input power producing a maximum output of 116 mW at the point of burnout. No test of safe operating power has been made but it should be ~80 mW output. With the UVa diodes, the room temperature efficiency is 34%, peaking at 150 mW input. The efficiency increases to 41% at 80 K (a 22% increase). While room temperature results differ a lot, the cold efficiencies are very similar because the mobility increase in the lower doped diodes is much larger than that for the higher doping. The frequency response of this doubler with the UVa diode is shown in Figure 1.

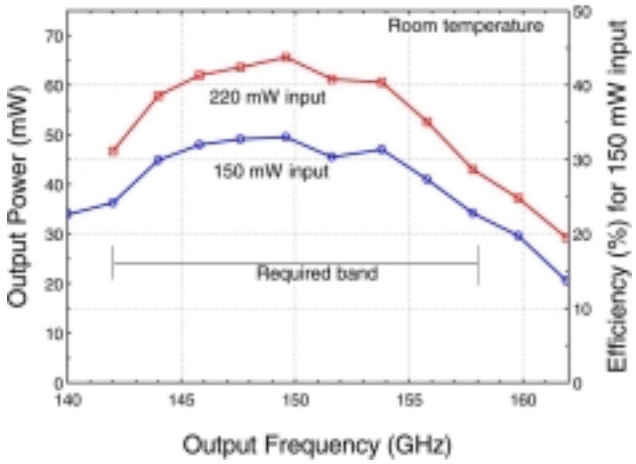

Figure 1. Frequency response of balanced doubler built to demonstrate one of the driver bands for FIRST. The efficiency corresponds to the lower curve.

In more recent work, a new doubler has been built for 200 GHz, which is suitable for MMIC fabrication using the "substrateless" fabrication technique [2]. This doubler uses the same 6 anode JPL diode array as the previously described doubler, but scaled down in size by a factor of 0.75. As before, the diode is soldered in place, but the remainder of the assembly is done by gluing and wire bonding. The bias circuit is decoupled with just a planar capacitor, eliminating the distributed filter previously used, and this capacitor is fabricated on GaAs with beam leads for grounding and bias connection. The doubler layout is shown in Figure 2.

The full circuit between the diode and the output waveguide is just a 12 μm diameter bond wire. It is found that more complex impedance matching is not needed in this region, and instead all of the wideband tuning of the circuit is done with waveguide elements. This makes the loss of these elements smaller, and reduces the complexity of assembly.

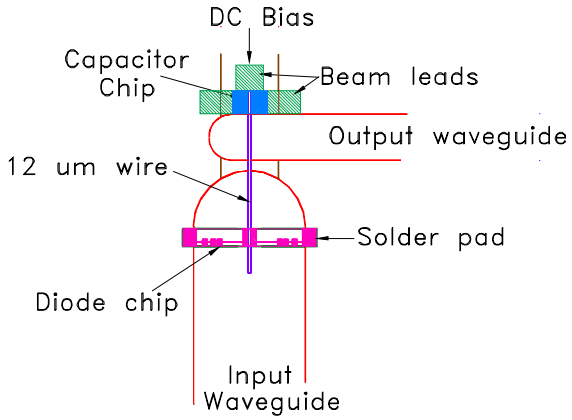

Figure 2. Drawing of the 200 GHz balanced doubler using a concept suitable for monolithic fabrication.

The design bandwidth is 188-212 GHz output with a very flat response, but a drafting error led to a loss of bandwidth in the prototype. However, the circuit operates close to the design frequency as shown in Fig 3, and the peak efficiency at room temp is 19% at 195 GHz, roughly consistent with 26% measured for the same diode batch at 140 GHz. The efficiency increases to 31% at 80K, a 60% increase, as shown in Figure 4. The peak efficiency occurs at the highest available input power, which is 220 mW, so it is not possible to be sure of the power handling capabilities.

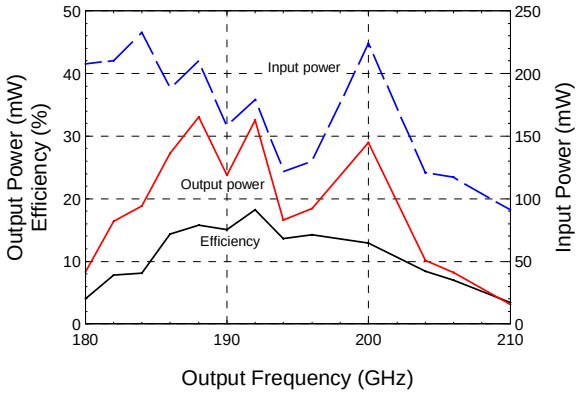

Figure 3. Frequency response of doubler with input power as noted.

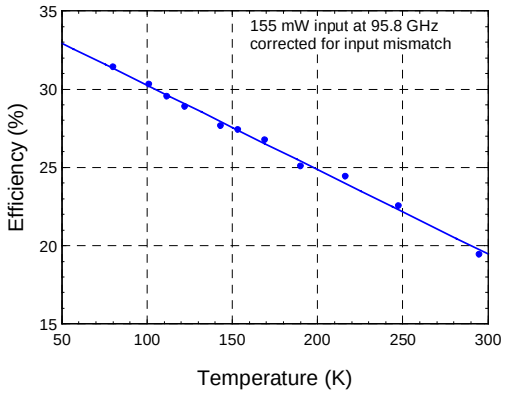

Figure 4. Efficiency of the doubler vs temperature measured at 95.8 GHz input.

MMIC Balanced Tripler

A nearly fully monolithic tripler has been designed which appears suitable for frequencies well into the submillimeter range. The circuit achieves nearly optimal terminations at the three frequencies of importance, in a very simple circuit. The circuit was designed with the aid of HFSS [3], and required many simulations to determine circuit parameters. Because simulations of such a complex structure were slow at the time of the design, the circuit is not well optimized over a wide bandwidth, and this version was viewed mostly as a proof of concept. The layout of the circuit is

shown in Figure 5.

The diodes are connected in antiparallel, with a DC break provided by an overlaid pair of lines with dielectric isolation on the output side of the circuit. Bias is applied to the diodes in series. The input is in a microstrip mode with an impedance near 50 Ω, and is fed by a waveguide to microstrip transition. At the input frequency the diode pair is in series with a short-circuited stub, which provides the correct input reactance. This stub is grounded using beam leads on the far side of the output waveguide. The output waveguide is cut-off at the input and so no additional filtering is needed at this frequency, but the line crossing the waveguide has very high impedance and so the waveguide must have quite reduced height in order to avoid adding excessive input inductance

At the output frequency, two radial stubs provide short circuits at either diode, and ensure that little power couples back to the input. At this frequency the input stub line becomes the coupling line to the output waveguide, as well as an impedance matching section. The narrow lines connecting to the diodes provide the required output inductance. Additional impedance matching is provided by a step transformer up to full height waveguide, and by a fixed backshort in the waveguide.

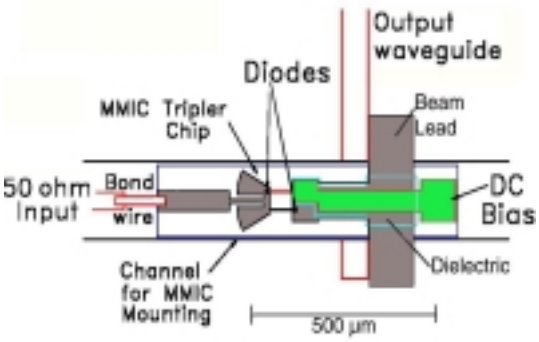

Figure 5. Drawing of the tripler chip, and its mounting relative to the output waveguide. The output step transformer is not shown.

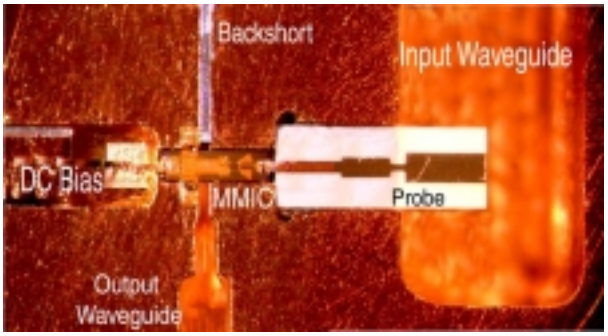

Figure 6. Photograph of the tripler for 280 GHz, showing the input and output waveguides, the alumina input transition and the bias connection.

At the second harmonic, the diode loop is tuned to provide nearly optimum inductance at midband without producing excess inductance at the output frequency. In part this is because the second harmonic currents flow in a different path, including transverse currents between the stubs, and across the wide output line. In addition, the radial stubs themselves act as quasi-lumped capacitances and load the loop in a way that increases its second harmonic reactance. The overall effect is an idler tuning which is optimized at midband and remains acceptable over quite a wide band, mainly at frequencies below the design band.

The circuit is in microstrip from the input to the radial stubs and switches to suspended stripline for the remainder of the circuit to avoid moding problems for the higher frequency part of the circuit. The channel housing the chip is significantly wider than the chip to further suppress

higher modes. This design is for a substrate thickness of 20 μm, chosen to minimize higher moding problems.

Triplers were designed for center frequencies of 280 and 320 GHz. These chips were fabricated on semi-insulating GaAs with epitaxial doping of 10^{17} cm^3. The anodes are made as rectangular strips of 1.5x9 μm with a breakdown voltage of 13 V, and a zero bias capacitance of 19 fF. The DC isolation dielectric is 0.1 μm thick SiN. The substrate has no backside metal, meaning that in the region where the mode is microstrip, the chip must be in good contact with the metal of the block. Chip separation was done by RIE (from the backside) which allows individual devices to be spaced very close to each other and also allows for the use of beam leads and arbitrarily shaped chips. The beam leads are essential to RF and DC ground the end of the chip where little area is available for wire bonding.

A photograph of the assembled tripler is shown in figure 6. Chips were glued down with a low viscosity epoxy, and then the beam leads were bonded to the block. An input transition to the WR10 waveguide was fabricated on 100 μm alumina [4]. Connections were made to the chip by ribbon bonding to the input and bias pads. Assembly was judged to be very easy compared to any other multipliers at a similar frequency.

Tests have been performed using a wide-band Gunn oscillator source, and some wideband power amplifiers. Bias was optimized at each frequency, and varied from 2 V at frequencies very low in the band, to 6-8 V at the higher (design) frequencies. While efficiency peaks at 20-30 mW input, as shown in Figure 7, the efficiency at 260 GHz remains high up to an output power of 7 mW. The input match varies from 6-10 dB return loss, and probably could be improved with some off-chip matching. The best efficiency of the 320 GHz device is 9%, increasing to 11% with the input mismatch corrected with a tuner. The output match has been measured with a sliding tuner only at 320 GHz, where it is very good. It is expected to be good only in the design band. Output power was measured with a wideband calorimeter sensor with an accuracy better than 5% [6]. The 320 GHz tripler survived cooling to 80 K, and its efficiency at 312 GHz increased to 14%, with 7 mW output. This corresponds to a 60% increase in efficiency.

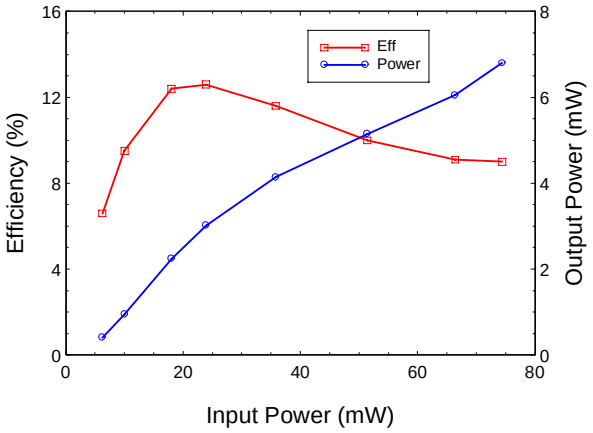

Figure 7. Efficiency vs input power level for the MMIC tripler at an output frequency of 260 GHz. Tripler is the nominal 280 GHz design on 38 μm substrate.

The best part of the operating band is very close to the design frequency, and is shifted low in both designs by only 2-5%. The peak efficiency measured at 320 GHz exceeds that obtained with the best whisker contacted triplers at a similar frequency [5], while the bandwidth, even in this non-optimized design, greatly exceeds that of whiskered devices. Fig 8 shows a comparison of a wideband fixed tuned whisker contacted tripler vs. this new design. The bandwidth was verified using a input source consisting of a WR10 tripler followed by a wideband medium power amplifier (25-40 mW output) [8]. The source was swept over an output band of 240-324 GHz with a minimum output of 0.3 mW at fixed bias.

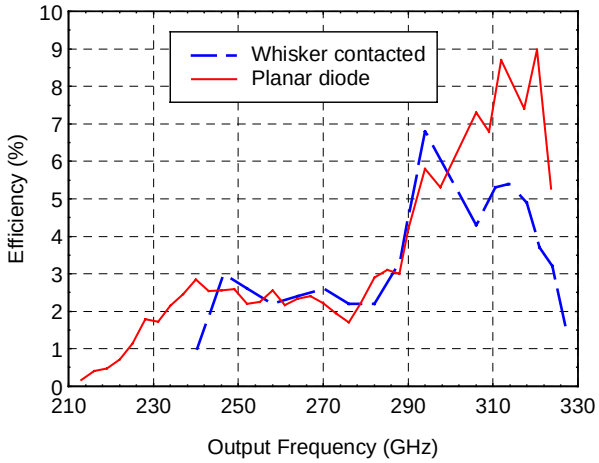

Figure 8. Efficiency of new MMIC tripler in the nominal 320 GHz design (solid), and older whisker contacted tripler (dashed) over a wide band.

Substrate thickness was initially thought to be important but later analysis showed that it could be much thicker without difficulties. Chips from the same wafer were also thinned to 38 μm and these devices were found to work as well as the design thickness, but with a frequency offset. Figure 9 shows the performance of chips of the 280 GHz design on the two thicknesses. While the thicker material appears to work better, this is probably due largely to better quality diodes in this chip, since simulations predict that there is no advantage to thicker material.

This design has been scaled to 1.0 and 1.2 THz using the JPL membrane and frame technology [7], and these wafers are in fabrication at this time. The membrane thickness of 3 μm makes the chips quite fragile, but there is no need to handle the thin part of the chip so assembly may prove relatively simple. The presence of the frame makes the block fabrication much more difficult, since waveguides can not cross the frame. However, the chip has been redesigned since this time, as noted below.

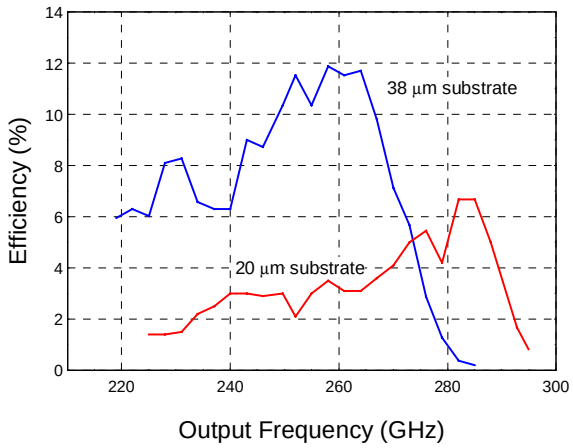

Figure 9. Triplers of nominal 280 GHz design fabricated on different thicknesses of GaAs. The difference in efficiency is probably due to the quality of the diodes, while the frequency shift is due to substrate thickness.

Improved MMIC Tripler

After discovering that the substrate thickness could be much larger, a 220-285 GHz circuit was redesigned for 38 μm GaAs. In this new design the radial stubs were rotated apart to allow the input line to have a lower impedance, which simulations showed was desirable. By increasing the diode capacitance, the idler loop was retuned to set the optimum idler match in midband for this wide bandwidth, rather than near the upper edge of the band. The input and output waveguide circuits were then optimized for flat response, resulting in a circuit that looks nearly the same yet achieves a very flat response at the peak efficiency of the previous design. In this design, the 1 dB bandwidth should be 13%, while the 3 dB bandwidth is 26%.

Thickening the substrate to 50 μm, and increasing the waveguide height by 60% still works with some loss of bandwidth, which makes higher frequency versions much more practical. A 1.1 THz design now uses a 12 μm substrate, practical with mechanical thinning, rather than requiring the membrane process. The output waveguide is 25 μm high, which is quite machinable. On this small chip the input waveguide probe can be integrated with negligible loss of wafer area, leaving only the bias to connect.

Doublers for 1200-2700 GHz

At much higher frequencies, balanced doublers are still desirable because they do not require filters, which are quite difficult to implement. The primary drawback is that the typical input power becomes so small that there may not be enough power to drive even the smallest practical diodes, and a balanced doubler doubles this power. A great savings in design effort comes about because at these frequencies varactor mode operation is not possible, due to low input power and very strong velocity saturation in GaAs. Designing in varistor mode is much easier

since the diode load is largely resistive, meaning that impedance matching is simplified, and the bandwidth increased.

In these designs, the diodes are placed in series in the output waveguide, rather than in the input as in the previous designs. A coupling probe in the input waveguide connects to the center point between the diodes. The intent is to minimize losses in the output circuit. With this geometry it is not essential to bias the diodes since with a short circuit at the waveguide walls, both diodes are maintained at zero bias. However, at very low power, doublers work much better with forward bias and so a bias circuit is still desired for the highest frequency devices. Two doublers have been designed for these higher bands to test out the concept, both using membrane construction on 3 μm GaAs, with a 50 μm frame surrounding the membrane.

The predicted performance of the two designs is shown in Figure 10, with an efficiency scale that is arbitrary, except as a guide to what might be possible. Too little is known about THz multipliers to make realistic predictions. Both designs work nearly as well as is theoretically possible near their efficiency peak, so they will serve as a good test of device performance. The manufacture of the blocks can be done entirely by milling, boring and broaching, with no difficult assembly. The chip should just drop in with minimal difficulty in positioning it properly. A bias lead is provided on some chips, and zero bias designs are also available. These chips are in fabrication at this time.

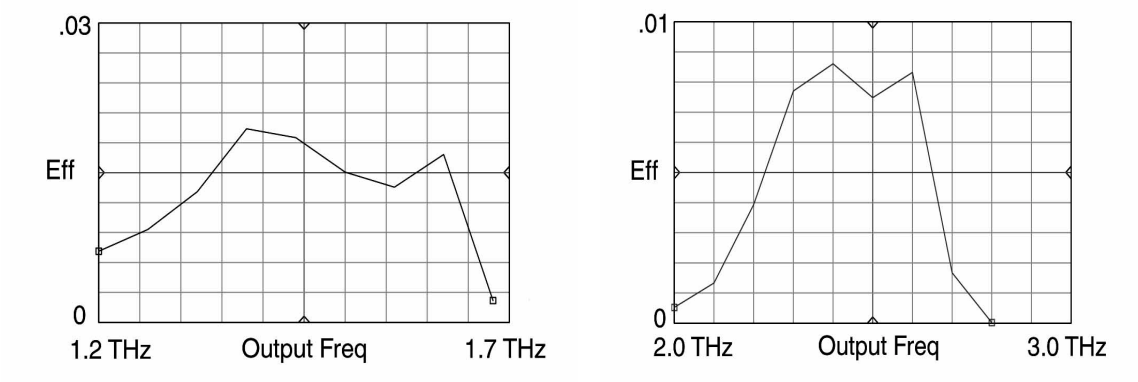

Figure 10. Predicted bandwidth of balanced doublers in two bands to test the feasibility of THz multipliers. The efficiency scale is largely arbitrary, since almost nothing is known about multiplier performance at these frequencies.

Conclusions

Frequency doublers and triplers are being developed for the FIRST mission, using full integration of the circuit onto a GaAs chip. So far progress has been made in developing a doubler of hybrid construction that can readily be converted to a substrate-less MMIC. An output power of 116 mW has been obtained at 140 GHz, and up to 55 mW at 195 GHz. Other doublers of fully monolithic design are in fabrication for much higher frequencies, while designs for 600-900 GHz have been fabricated but not tested.

A fully monolithic tripler has been designed which seems usable for frequencies from 200-1200 GHz. Tests on a prototype near 300 GHz are very encouraging with efficiency and bandwidth superior to the best whiskered designs. Output power is also higher that for any previous designs.

All of these designs indicate that monolithic fabrication is truly the best way to approach the production of submillimeter multipliers and that our goal to reach the THz range is realistic. This will result in much more reproducible, reliable and lower cost LO sources than have been available in the past, and will enable large scale applications.

Acknowledgements

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