

SELF-CONSISTENT PHYSICS-BASED NUMERICAL DEVICE/HARMONIC-BALANCE CIRCUIT ANALYSIS OF HETEROSTRUCTURE BARRIER AND SCHOTTKY BARRIER VARACTORS INCLUDING THERMAL EFFECTS

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Abstract

In order to effectively design millimeter and submillimeter wave frequency multipliers, both the electrical and thermal properties of the device and circuit must be analyzed in a fully self-consistent manner. To facilitate a self-consistent analysis of Heterostructure Barrier Varactor (HBV) and Schottky Barrier Varactor (SBV) frequency multipliers, large-signal time- and temperature-dependent numerical device simulators, with excellent computational speed and convergence properties, have been developed for generic GaAs/InGaAs/AlGaAs HBV and conventional GaAs SBV structures having arbitrary doping profiles. The numerical device simulators are based on the first two moments of the Boltzmann transport equation coupled to Poisson's equation, and combine current transport through the device bulk with thermionic and thermionic-field emission currents imposed at the Schottky interface or heterojunction interfaces. Given the importance of both the active device and its embedding circuit in the design of frequency multipliers, the numerical device simulators have been combined with a novel and efficient harmonic-balance circuit analysis technique to provide unified computer-aided design environments for entire HBV or SBV multiplier circuits. The steady-state thermal properties of frequency multipliers are analyzed based on the amount of power dissipated in the active region of the device and the thermal resistance to heat flow presented by the various elements that make up the circuit. From these quantities, the average temperature across the active region of the varactor can be estimated for use in the appropriate device simulator. The thermal model presented here uses simple geometrical expressions for the various thermal resistances of circuits utilizing both planar and whisker-contacted diode geometries assuming the ambient air is a perfect insulator. For planar diodes, the thermal resistance of the diode substrate is calculated using a three-dimensional finite-element heat flow analysis to account for the substrate's irregular heat flow geometry. Using the numerical device/harmonic-balance circuit simulators, an investigation is undertaken to determine the frequencies at which the widely used quasi-static equivalent circuit varactor models fail, and for what reasons these models fail. A comparison is made between published experimental results and a full analysis, including both electrical and thermal properties, of frequency multipliers utilizing the UVA 6P4 GaAs SBV and a single barrier GaAs/Al_{0.7}Ga_{0.3}As HBV.

I. Introduction

In order to effectively design highly nonlinear circuits such as large-signal amplifiers, frequency converters, and oscillators, both the electrical and thermal properties of the active device and its embedding circuit must be analyzed in a fully self-consistent manner. To achieve such a self-consistent analysis, the electrical interaction between the nonlinear active device and its linear

embedding circuit is typically determined using a harmonic-balance circuit analysis technique. The active device is usually modelled analytically by a lumped quasi-static equivalent circuit. The use of such an equivalent circuit model for the active device, however, has limited validity at high device operating frequencies and power levels, requires significant insight into the operation of the active device in order to develop an accurate equivalent circuit topology, and requires a laborious and often non-unique procedure to determine the elements of the equivalent circuit as functions of bias, frequency, and temperature. The validity of such an active device model is particularly suspect at the millimeter and submillimeter wavelengths where the large-signal nonstationary high frequency dynamics of carrier transport begin to dominate device operation. With this in mind, the development of reliable and efficient circuits operating into the terahertz frequency range clearly requires a much more accurate approach to nonlinear circuit analysis and design.

Our approach to the analysis and design of high frequency nonlinear circuits is to utilize a physics-based numerical device model in conjunction with a harmonic-balance circuit analysis technique. This paper details the simulation and analysis of Heterostructure Barrier Varactor (HBV) and Schottky Barrier Varactor (SBV) frequency multipliers using such an analysis and design approach. To facilitate a fully self-consistent analysis of HBV and SBV frequency multipliers, large-signal time- and temperature-dependent numerical device simulators, with excellent computational speed and convergence properties, have been developed for generic GaAs/InGaAs/AlGaAs HBV and conventional SBV structures having arbitrary doping profiles. The numerical device simulators have been combined with a novel and efficient harmonic-balance circuit simulation technique specifically designed to facilitate the inclusion of a numerical device simulator. The combined numerical device/harmonic-balance circuit simulators provide unified computer-aided design environments for entire HBV or SBV frequency multiplier circuits so that such circuits can be co-designed from both a device and a circuit point of view. Such co-design requires the user to specify the device geometry, doping profile, and alloy composition profile, as well as the parasitic device impedances and embedding impedances of the circuit. In conjunction with the combined numerical device/harmonic-balance circuit analysis, the steady-state thermal properties of frequency multipliers are analyzed based on the amount of power dissipated in the active region of the device and the thermal resistance to heat flow presented by the various elements that make up the circuit. From these quantities the average temperature across the active region of the varactor can be estimated for use in the appropriate device simulator.

The remainder of the paper is outlined as follows. The transport equations, interface conditions, and numerical solution approach used in the large-signal time- and temperature-dependent device simulators are presented in Section II. An overview of the novel harmonic-balance circuit analysis technique and its integration with the numerical device simulator is also given in Section II. Section II ends with a discussion of the frequency-dependent parasitic impedances of whisker-contacted HBV and SBV diodes. Section III details the thermal model used to calculate the average active region temperature of whisker-contacted and planar geometry varactor diodes. A comparison between the thermal properties of a standard whisker-contacted varactor diode and an equivalent planar varactor diode is also presented in Section III. Using the harmonic-balance circuit analysis technique coupled to both the numerical device simulators and lumped quasi-static equivalent circuit models derived from the DC results of the numerical device simulators, we examine at what frequencies the widely used quasi-static equivalent circuit models fail and why they fail in Section IV. A comparison is also made in Section IV between published experimental results and a full analysis, including both electrical and thermal properties, of

frequency multiplier circuits utilizing the UVA 6P4 GaAs SBV and a single barrier GaAs/Al_{0.7}Ga_{0.3}As HBV. Finally, conclusions are given in Section V.

II. Numerical Device/Harmonic-Balance Circuit Simulation Approach

A. Physics-Based Numerical Device Simulation Technique

Carrier transport through the bulk region(s) of an HBV or SBV has been described[1-3] by a set of one-dimensional coupled nonlinear differential equations for electrons based on the first two moments of the Boltzmann transport equation and Poisson's equation. The resulting equations governing DC and time-dependent transport are

$$\frac{\partial n(x, t)}{\partial t} = \frac{1}{q} \frac{\partial J_n(x, t)}{\partial x}, \quad (1)$$

$$J_n(x, t) = -q\mu_n(x) n(x, t) \frac{\partial \phi_n(x, t)}{\partial x}, \quad (2)$$

and

$$\frac{\partial}{\partial x} \left[\epsilon(x) \frac{\partial \psi(x, t)}{\partial x} \right] = q[n(x, t) - N_D(x)], \quad (3)$$

where

$$n(x, t) = n_{i, ref} \exp \left[\frac{q}{kT} (\psi(x, t) + V_n(x) - \phi_n(x, t)) \right], \quad (4)$$

and where J_n is the electron particle current density, n is the electron density, ϕ_n is the electron quasi-Fermi potential, ψ is the electrostatic potential, k is Boltzmann's constant, q is the electron charge, T is the absolute temperature, $n_{i, ref}$ is the intrinsic electron density in the reference material (GaAs), and V_n , μ_n , m^* , N_D , and ϵ are the spatially-dependent alloy potential[4], electron mobility, electron conductivity effective mass, donor impurity concentration, and dielectric permittivity, respectively. Field-dependent electron mobilities are not considered here since electrons in HBVs, or SBVs below the flat-band voltage, are not being heated by the electric field[5]. Furthermore, electrons can not reach a steady state with the local electric field in the short high field regions of these devices[5]. For longer devices or devices operating above about 300 GHz, it becomes imperative to utilize the drift-diffusion equations presented above, in conjunction with the energy balance equations, so that the electron mobility can vary with the local electron energy.

In order to accurately model the current in heterostructure devices, careful consideration of carrier transport across abrupt material discontinuities is required[6,7]. As such, electron transport across the abrupt heterointerfaces of an HBV has been described by a set of nonlinear electron particle current density equations which take into account thermionic emission and thermionic-field emission of carriers over and through the abrupt barrier[3]. Regardless of bias polarity, one of the two heterointerfaces in a single barrier HBV is above flat-band. For this heterointerface, the semiconductor-semiconductor heterointerface analog[1-3] to the boundary constraint of Adams and Tang[8,9] for metal-semiconductor interfaces at high forward bias has been utilized.

Continuity of the electric displacement, electrostatic potential, and electron particle current density complete the set of interface conditions required for a self-consistent solution at a given heterointerface. A complete description of the boundary conditions for HBVs, including tunneling through the barrier, is given in [3]. As a result of this simulation approach, current transport through the heterostructure bulk is self-consistently combined with thermionic and thermionic-field emission currents imposed at the heterointerfaces.

For SBVs, a similar simulation approach is utilized to self-consistently combine current transport through the device bulk with thermionic and thermionic-field emission current imposed at the metal-semiconductor contact in a manner analogous to the analytical thermionic-emission/diffusion theory of Crowell and Sze[10]. Following the work of Adams and Tang[8,9], we have adopted a current density boundary constraint at the metal-semiconductor interface which is derived under the assumption of a drifted Maxwellian electron distribution at the interface. The use of this boundary constraint allows us to avoid the unphysical accumulation of electrons at the Schottky contact above the flat-band voltage. The resulting metal-semiconductor current density interface constraint at $x = 0$ is

$$J(0) = qv_{r,n} [n(0) - n_0] \quad (5)$$

where $n(0)$ is the electron density at the metal-semiconductor interface and n_0 is the equilibrium electron density at this interface. The effective surface recombination velocity for electrons, $v_{r,n}$, is given by

$$v_{r,n} = v_d + \sqrt{\frac{2kT}{\pi m^*}} \left\{ \frac{\exp\left[-v_d^2 \left(\frac{2m^*}{kT}\right)\right]}{1 + \operatorname{erf}\left(v_d \sqrt{\frac{2m^*}{kT}}\right)} \right\} \quad (6)$$

where m^* is the electron effective mass at the metal-semiconductor interface, and the amount of drift in the electron distribution at the metal-semiconductor interface is modelled as

$$v_d = \frac{J(0)}{qn(0)}. \quad (7)$$

The electrostatic potential at the metal-semiconductor interface, assuming the metal is maintained at a potential of zero, is

$$\psi(0) = \frac{\chi_{ref} - \Phi}{q} + \frac{kT}{q} \ln\left(\frac{N_{C,ref}}{n_{i,ref}}\right) \quad (8)$$

where χ_{ref} is the electron affinity in the reference material, Φ is the metal work function, and $N_{C,ref}$ is the total effective conduction band density of states in the reference material. The first term in this equation is the barrier height, ϕ_b , at the metal-semiconductor interface divided by the electronic charge. To account for the image-force lowering of the metal-semiconductor barrier, the barrier height is modified by an amount

$$\Delta\phi_b = \sqrt{\frac{q|\xi(0)|}{4\pi\epsilon(0)}} \quad (9)$$

where ξ is the electric field at the metal-semiconductor interface.

In order to develop robust numerical device simulators which could be efficiently combined with a harmonic-balance circuit analysis technique, careful consideration has been given to developing device simulators with excellent numerical convergence and accuracy properties. Potential problems and inefficiencies have been minimized by the use of finely subdivided, nonuniform mesh structures, a fully implicit finite difference time discretization scheme, and the state variables J_n , ϕ_n , ψ , and D . For an HBV, the four resulting carrier transport equations are solved, in the three regions (one barrier and two modulation) of the device, for a given bias value, and subject to the heterointerface constraints and ideal ohmic contact boundary constraints, via the coupled equation Newton-Raphson method. A full discussion of the solution algorithm for HBVs is given in [3]. A similar solution algorithm, with the appropriate metal-semiconductor interface constraints and ideal ohmic contact boundary constraints, has been utilized for SBVs. For SBVs, the algorithm is simplified by the fact there is only one region of interest as opposed to the three regions of an HBV. In order to derive an entire current-voltage (I-V) curve or time-domain current waveform, as well as to obtain information about the internal physics of the device as a function of bias, the DC or time-dependent bias is incrementally changed from the zero-bias condition. For DC simulations, the device static capacitance-voltage (C-V) relationship is derived by calculating the change in charge with respect to the change in applied bias over the depletion side of the device for sufficiently small bias increments. It is important to note that the use of the Adams and Tang metal-semiconductor current density interface constraint allows us to calculate very accurately the forward bias capacitance of SBVs.

B. Harmonic-Balance Circuit Analysis Technique

The novel harmonic-balance circuit analysis technique employed in this work is derived from the multiple-reflection algorithm[11]. The time-domain current through the device active region is calculated by the appropriate numerical device simulator, for one period, as described in the previous section. The harmonic components of the current are extracted from the time-domain current waveform using a discrete fourier transform; for HBVs, thirteen harmonics plus the DC term have been utilized, while six harmonics plus the DC term have been utilized for SBVs. A fixed-point iterative scheme, derived from the robust multiple-reflection algorithm and termed the Accelerated Fixed-Point (AFP) method[12], is then used to update the total voltage applied directly across the active region of the device in terms of the embedding impedances of the circuit, the harmonic components of the current, and the harmonic components of the voltage from previous iterations. In equation form, the new voltage component $V_{n,k+1}$ at the intrinsic device terminals, for harmonic number n and iteration step $k+1$, is

$$V_{n,k+1} = \left(\frac{Z_n^{TL}}{Z_n^{Linear} + Z_n^{TL}} \right) V_n^{Source} + \left(\frac{Z_n^{Linear}}{Z_n^{Linear} + Z_n^{TL}} \right) (V_{n,k} - I_{n,k} Z_n^{TL}) \quad (10)$$

where Z_n^{TL} , Z_n^{Linear} , V_n^{Source} , and $I_{n,k}$ are the fictitious transmission line characteristic impedance, Thevenin equivalent impedance, and source voltage of the linear embedding circuit at harmonic number n , and the device current component for harmonic number n and iteration step k , respectively. This iterative process is applied until the harmonic components of the voltage converge to their steady-state values, or

$$\left| \frac{(V_n - V_n^{Source})}{I_n} \right| / |Z_n^{Linear}| \quad (11)$$

is within a user-specified tolerance factor of unity for all harmonics; this tolerance factor is typically set to about 0.1 percent.

The novelty in the harmonic-balance algorithm utilized here is that, in deriving the fixed-point iterative voltage update expression (equation (10)), we use *a priori* knowledge, from Kirchhoff's voltage law, that the nonlinear device impedance will equal the negative of the linear embedding impedance of the circuit for each of the undriven harmonics in the steady state. This eliminates the computationally intensive and possibly unstable Runge-Kutta numerical time-integration necessary in the original multiple-reflection algorithm[11], and allows us to calculate complex under-relaxation parameters for each harmonic component of the fixed-point iterative voltage update equation. A Steffenson numerical acceleration scheme for iterative equations, derived from the secant methods of numerical analysis[13], is also utilized to greatly increase the computational speed and convergence properties of the harmonic-balance circuit analysis. The new voltage component $V_{n,k+1}$ at the intrinsic device terminals, for harmonic number n and iteration step $k+1$, then becomes

$$V_{n,k+1} = \tilde{V}_{n,k+2} + \frac{(\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1})(\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1})}{(\tilde{V}_{n,k+1} - V_{n,k}) - (\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1})} \quad (12)$$

where $\tilde{V}_{n,k+2}$ and $\tilde{V}_{n,k+1}$ are intermediate voltage values calculated from two successive applications of equation (10), starting with $\tilde{V}_{n,k} = V_{n,k}$. Overall, the harmonic-balance circuit analysis technique outlined above avoids the laborious numerical calculations needed in Newton-type techniques to assemble Jacobian matrices and solve large linear systems of equations, while maintaining a convergence rate nearly equal to that of Newton-type methods.

Frequency-dependent parasitic impedances, external to the active region of the device and similar to those of [11], are included in the harmonic-balance circuit analysis as additional contributions to the linear device embedding circuit. These parasitic device impedances apply to whisker-contacted geometry diodes, as this geometry is investigated later in the paper. The parasitic impedances utilized here differ from those of [11] as follows: 1) the results of [14] for the purely resistive DC parasitic impedance are used, 2) we include the displacement current and mass-inertial contributions to the parasitic impedance of [15], 3) we include the spreading impedance at the backside ohmic contact as calculated in [16], and 4) the corrected AC spreading impedance expressions given in [17] are used. Given the intrinsic device impedances calculated from the harmonic-balance circuit analysis and the parasitic device impedances, the power generated at each harmonic can, then, be calculated from

$$P_n = \frac{1}{2} \Re e (Z_{n,Device} + Z_{n,Parasitic}) |I_n|^2 \quad (13)$$

where $Z_{n,Device}$ and $Z_{n,Parasitic}$ are the harmonic device and parasitic impedances, respectively, and I_n is the total device current at a given harmonic.

III. Thermal Model of Whisker-Contacted and Planar Varactor Multipliers

In addition to considering the electrical characteristics of HBV and SBV frequency multiplier circuits, the thermal properties of these circuits must also be analyzed due to the large amount of power that can be dissipated in the varactor diode itself. Our analysis of these circuits is a steady-state analysis based on the amount of power dissipated in the active region of the device and the thermal resistance to heat flow presented by the various elements that make up the circuit. From these quantities, the average temperature across the active region of the varactor diode can be estimated for use in the appropriate numerical device simulator.

The thermal model presented here uses simple geometrical expressions for the various thermal resistances of circuits utilizing both whisker-contacted and planar diode geometries assuming the ambient air is a perfect insulator. For heat flow through a bulk section of material surrounded by air (see Figure 1a), the thermal resistance is

$$R_{Thermal} = \frac{t}{\kappa \pi a^2} \quad (14)$$

where t is the thickness of the section, a is an equivalent radius based on the cross-sectional area of the section, and κ is the material's thermal conductivity. Likewise, for heat flow through a heat contact and into a multilayer stack of materials (see Figure 1b), the approximate thermal resistance of the first layer is [18]

$$R_{Thermal} = \frac{t}{\kappa_1 \pi ((a_1 + a_2)/2)^2} \quad (15)$$

where a_1 is an equivalent radius based on the cross-sectional area of the heat contact through which heat flows into the multilayer stack, and

$$a_2 = a_1 + t \tan \theta. \quad (16)$$

Following [18], the heat flux is assumed to be transmitted within a truncated right circular cone of vertex angle θ , and this angle is taken to be 45° . For heat flow into a semi-infinite heat sink (see Figure 1c), the thermal resistance is given by

$$R_{Thermal} = \frac{1}{4\kappa a} \quad (17)$$

where, again, a is an equivalent radius based on the cross-sectional area of the heat contact through which heat flows into the heat sink.

For planar diodes, the thermal resistance of the diode substrate is calculated using a three-dimensional finite-element heat flow analysis [19] to account for the substrate's irregular heat flow geometry. The substrate thermal resistance is calculated from the amount of power required to generate a 1 K temperature gradient between the input and output heat flow "ports" of the substrate assuming a uniform heat flux into and out of the substrate, a constant substrate thermal conductivity, and perfectly insulating chip boundaries. The planar geometry considered here (see Figure 1d) is that of a planar diode pair, with dimensions that correspond to the δ -doped anti-series SBV of [20]. This geometry is of particular interest as a suitable geometry for planar HBVs. Due

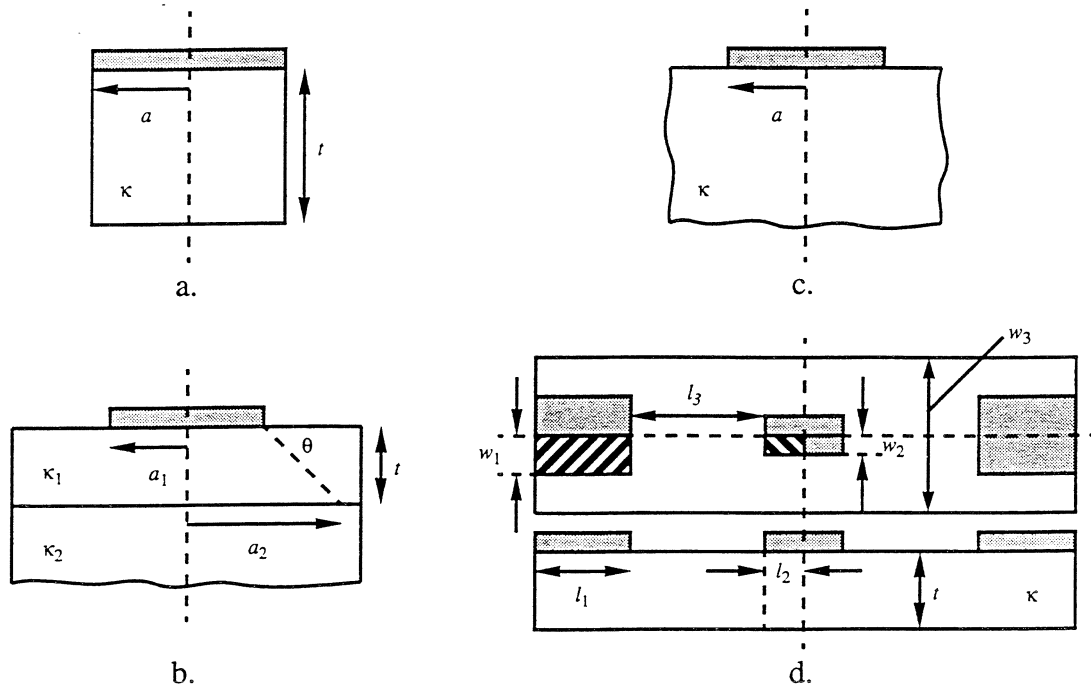


Figure 1. Relevant geometries for constituent elements of multiplier circuits: a. bulk section of material surrounded by air, b. multilayer stack of materials, c. semi-infinite heat sink, and d. planar diode pair substrate configuration (top and side views) with input ($w_1 \times l_1$) and output ($w_2 \times l_2$) heat flow “ports”[20].

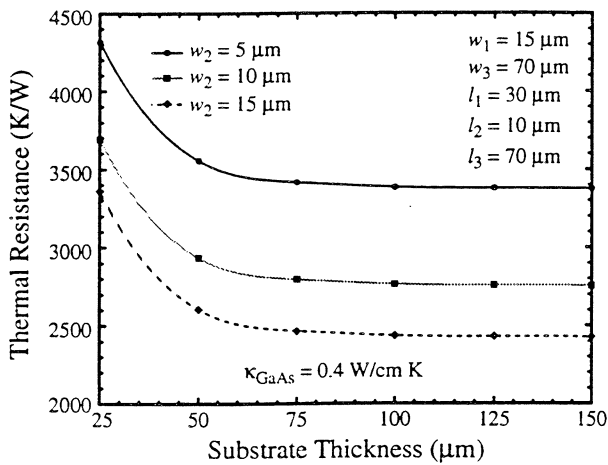


Figure 2a. Thermal resistance versus substrate thickness t and input heat flow “port” width w_2 for half of a planar diode pair.

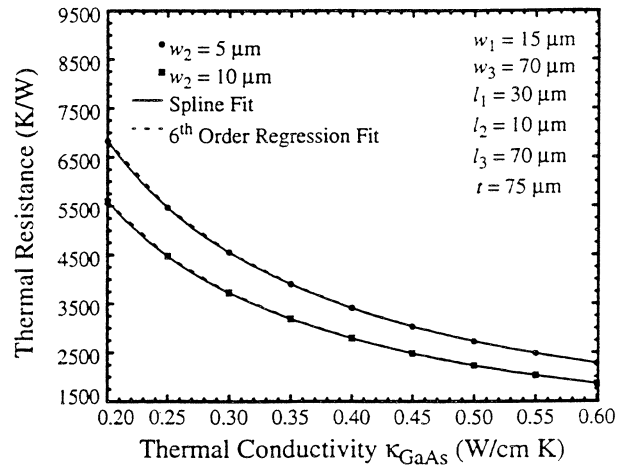


Figure 2b. Thermal resistance versus substrate thermal conductivity and input heat flow “port” width w_2 , for half of a planar diode pair

to symmetry considerations, only a quarter of the actual planar substrate is simulated. Figure 2a shows the calculated planar substrate thermal resistance as a function of substrate thickness t and input heat flow “port” width w_2 . The important result to note from this figure is that, to achieve optimum heat sinking with a GaAs substrate and the typical device dimensions shown, the substrate should not be thinned below about 3 mils. Figure 2b shows the calculated planar substrate thermal resistance, as a function of substrate thermal conductivity and input heat flow “port” width

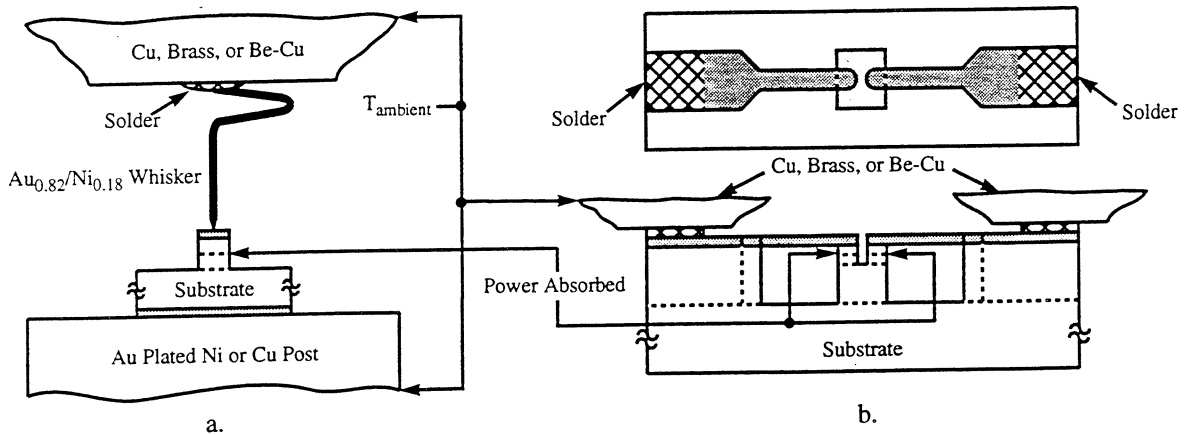


Figure 3. Representative multiplier circuits: a. whisker-contacted geometry and b. planar geometry. Circuit temperature is assumed to reach equilibrium with the ambient air at the locations indicated. The dissipated power is assumed to be absorbed in the center of the diode active region.

w_2 , along with analytical fits to the calculated resistances.

With a known amount of power dissipated in the active region of a varactor multiplier, the steady-state linear temperature gradient across each element of the multiplier circuit is simply the product of the power flowing through the particular element and the thermal resistance of the element. For simplicity, it is assumed that all of the dissipated power is absorbed in the center of the device active region. Representative whisker-contacted and planar multiplier circuits are shown in Figure 3a and 3b. Since these circuits have more than one heat flow path to reach equilibrium with the ambient air, an equivalent circuit representation of the actual circuit's thermal resistances is used to calculate the portion of the total dissipated power that flows through each path of the equivalent circuit. For example, in the planar diode pair configuration, there are four parallel heat flow paths (parallel heat flow through the finger and through the substrate for each diode in the configuration).

To further simplify the analysis, the thermal conductivity of each element in the circuit is taken to be a constant value versus position that is determined by the average temperature across the element. The thermal conductivities of the metallic portions of Figure 3a and 3b vary slowly with temperature; they are essentially equal to their values at 300 K ($\kappa_{\text{Au},300\text{K}} = 3.15 \text{ W/cm K}$, $\kappa_{\text{Ni},300\text{K}} = 0.636 \text{ W/cm K}$, $\kappa_{\text{Cu},300\text{K}} = 3.98 \text{ W/cm K}$, and $\kappa_{\text{Brass/Be-Cu},300\text{K}} = 1.0 \text{ W/cm K}$). On the other hand, the semiconductor portions of Figure 3a and 3b have the largest variation in thermal conductivity with temperature; for GaAs, the thermal conductivity follows a[21]

$$\kappa = \frac{A}{T^{1.2}} \quad (18)$$

law where A varies with doping level. For GaAs doped at $N_D = 1 \times 10^{17} \text{ cm}^{-3}$, $A = 488$ while $A = 366.5$ for highly doped GaAs[21]. Since the thermal conductivity of each element is allowed to vary with the average temperature across the element, the process outlined above is an iterative one. For this work, convergence was achieved when the temperature change, from one iteration to the next and across all of the circuit elements, was less than 0.1 K.

Using this thermal analysis, we examined the thermal properties of two HBV frequency multiplier circuits, one using a whisker-contacted geometry diode (see Figure 3a) and a companion one using a planar geometry diode (see Figure 3b). Both HBV diodes were double barrier

structures (1.5 $\mu\text{m}/\text{barrier}$) with 8 μm diameter anodes and 3 mil thick substrates. The whisker-contacted geometry diode had an n^+ substrate ($A = 488$) while the planar geometry diode had a SI substrate ($A = 544$). The whisker-contacted multiplier circuit utilized a 2.125 mm long, 1 mil diameter $\text{Au}_{0.82}/\text{Ni}_{0.18}$ whisker. Critical dimensions for the planar geometry diode are as follows: n^+ GaAs buffer 4 μm thick, diced chip 220 μm long and 70 μm wide, Au metallized fingers 2.5 μm thick, 50 μm long, and 8 μm wide, and Au metallized bonding pads 2.5 μm thick, 60 μm long, and 30 μm wide. The output heat flow “port” was assumed to be comprised of only half of the bonding pad length and, thus, was assumed to be 30 μm long and 30 μm wide. Figure 4 shows the calculated average active region temperature for these two multiplier circuits. Overall, these initial comparisons of the thermal properties of whisker-contacted and planar geometry varactor diodes indicate that the average active region temperature in planar geometry diodes can be significantly higher than the temperature in whisker-contacted geometry diodes. Such elevated temperatures translate directly into lower carrier mobilities in the device and, thus, lower circuit multiplying efficiencies. Furthermore, for the waveguide-mounted, flip-chip planar diode multiplier circuit configuration considered here, the diode substrate thickness should be no thinner than about 3 mils to insure optimal heat sinking.

IV. Numerical Device and Harmonic-Balance Circuit Simulation Results

In order to investigate the importance of using numerical device simulators in place of the usual lumped quasi-static equivalent circuit device models, the harmonic-balance circuit analysis has been coupled to both the HBV and SBV numerical device simulators, and simple quasi-static device models for HBVs and SBVs. The quasi-static equivalent circuit models have been derived from curve-fits to the DC I-V and static C-V characteristics of the devices as determined by the numerical device simulators. The total device current as an instantaneous function of bias $i(V(t))$ is, thus,

$$i(V(t)) = I_{DC}(V(t)) + C_{Static}(V(t)) \frac{dV}{dt}. \quad (19)$$

While not completely self-consistent and certainly subject to high frequency and high power divergence problems, these quasi-static device models alleviate some of the inaccuracies associated with the device models typically employed in the analysis of frequency multipliers. One such problem is the inaccurate forward bias C-V relationship typically used to describe SBVs operating in a hybrid varactor/varistor mode, i.e. at high frequencies and/or high power levels. For devices such as the HBV, the use of such curve-fit device models is invaluable since the terminal characteristics of such devices are not directly amenable to description by simple analytical expressions. As will be shown below, these vastly improved quasi-static device models still lack complete self-consistency, and do not accurately model the large-signal nonstationary dynamics of carrier transport that dominate device operation at high frequencies and high power levels.

In the remainder of the paper, we examine three specific whisker-contacted frequency multipliers, the UVA 6P4 and UVA 5T1 GaAs SBV doublers of [22], and the single barrier GaAs/ $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$ HBV tripler of [23]. The 6P4 SBV has a 1.0 μm , $3.5 \times 10^{16} \text{ cm}^{-3}$ active region, while the 5T1 SBV has a 0.6 μm active region doped at $1.0 \times 10^{17} \text{ cm}^{-3}$. The measured forward DC bias series resistance of the 6P4 (5T1) SBV is 9.5 (5.3) Ω , while the measured zero-bias capacitance is

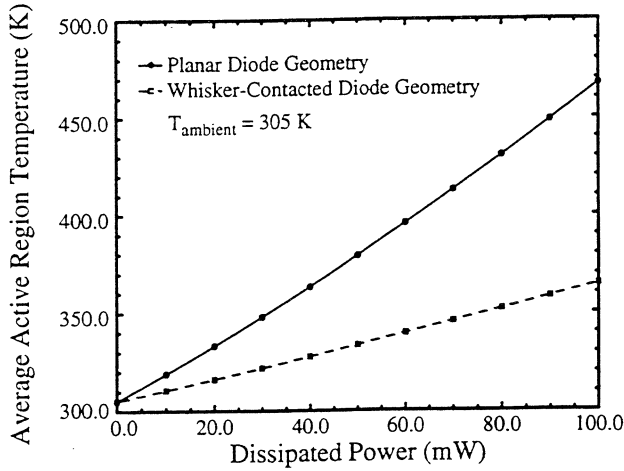


Figure 4. Average active region temperature versus power dissipated in the active region for the whisker-contacted and planar diode geometries of Figures 3a and 3b.

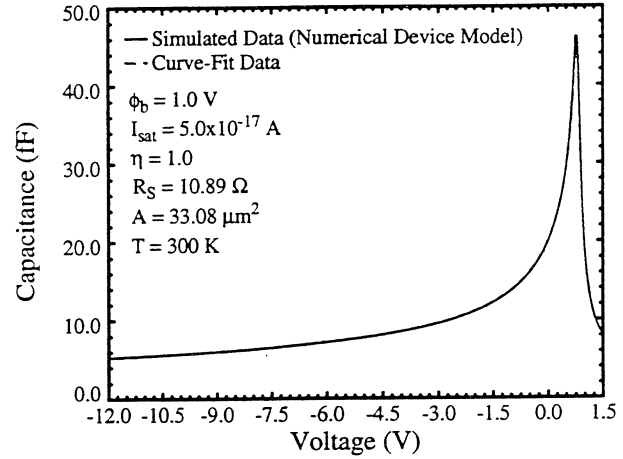


Figure 5. Simulated and curve-fit $C(V)$ characteristics for the UVA 6P4 GaAs SBV of reference [22].

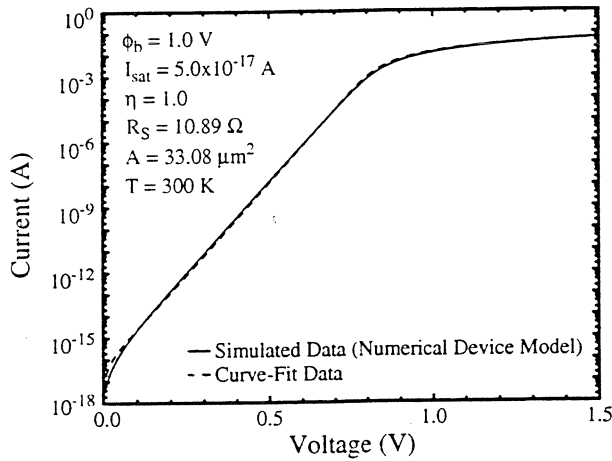


Figure 6. Simulated and curve-fit $I(V)$ characteristics for the UVA 6P4 GaAs SBV of reference [22].

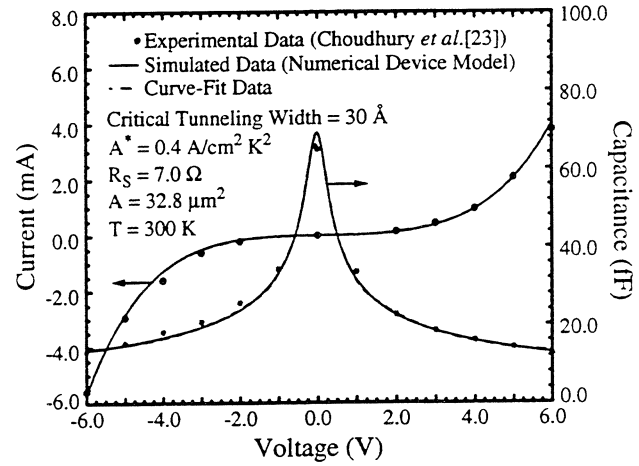


Figure 7. Experimental, simulated, and curve-fit $I(V)$ and $C(V)$ characteristics for the single barrier GaAs/Al_{0.7}Ga_{0.3}As HBV of reference [23].

20.0 (22.0) fF and the measured breakdown voltage is -20.0 (-10.0) V. Again, the quasi-static equivalent circuit model for the SBVs utilized curve-fits to the static $C-V$ characteristics as determined by the SBV numerical device simulator. The static $C-V$ results obtained from the numerical device simulator for the 6P4 SBV are shown in Figure 5 along with the results obtained from the quasi-static equivalent circuit model. Likewise, Figure 6 shows a comparison of the 6P4 SBV DC $I-V$ results obtained from the numerical device and quasi-static equivalent circuit models. Similar results have been obtained for the 5T1 SBV. For the DC $I-V$ characteristics, the quasi-static equivalent circuit model actually utilized the nonlinear diode equation

$$I = I_{sat} \left[\exp\left(\frac{q(V - IR_S)}{\eta kT}\right) - 1 \right] \quad (20)$$

which was solved analytically following the technique of [24]. In this equation, the ideality factor, η , was taken to be unity, the saturation current, I_{sat} , was taken to be 5.0×10^{-17} A, and the series resistance, R_S , was taken to be the calculated resistance of the entire SBV epitaxial layer based on the active layer electron mobility utilized in the numerical device simulator. For the 6P4 SBV, the resistance was 10.89Ω based on a mobility of $4950 \text{ cm}^2/\text{Vs}$; for the 5T1 SBV, the resistance was 4.36Ω based on a mobility of $4200 \text{ cm}^2/\text{Vs}$. A metal-semiconductor barrier height, ϕ_b , of 1.0 V was used in the numerical device simulator for both SBVs. It is important to note that no series resistance term was used in obtaining the numerical device simulator DC I-V results; the correctly simulated linear I-V characteristic in high forward bias is a direct consequence of the resistive nature of a Schottky diode above the flat-band voltage. Furthermore, it should be noted that the forward bias static C-V characteristic of the SBV is properly simulated[8] as a consequence of using the current density-dependent surface recombination velocity in the Schottky contact current boundary constraint.

The Choudhury *et al.*[23] HBV we have investigated consists of a 213 \AA intrinsic $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$ barrier surrounded by 53 \AA intrinsic GaAs spacer layers and 5330 \AA n-type ($1 \times 10^{17} \text{ cm}^{-3}$) GaAs modulation layers. The slight asymmetry evident in the experimental HBV data has been modelled via a slight asymmetry in the modulation layer doping concentrations; one side of the device was assumed to have a doping concentration of $1.0 \times 10^{17} \text{ cm}^{-3}$, while the other side was assumed to have a doping concentration of $1.125 \times 10^{17} \text{ cm}^{-3}$. In the numerical device simulator, the active layer electron mobility was assumed to be $4200 \text{ cm}^2/\text{Vs}$, while an effective Richardson constant of $0.4 \text{ A/cm}^2\text{K}^2$ was assumed for the heterointerface current density boundary constraints[1-3]. The quasi-static equivalent circuit model for this HBV was derived entirely from curve-fits to the DC I-V and static C-V results obtained from the numerical device simulator. Excellent correlation has been obtained between the HBV numerical device simulator and experimental DC I-V and static C-V characteristics[23]. Figure 7 shows the experimental DC I-V and static C-V characteristics of this HBV along with the simulated characteristics from the numerical device and equivalent circuit models. The measured series resistance of 7.0Ω has been utilized in calculating the simulated and curve-fit DC I-V and static C-V characteristics.

For all of the simulations to follow, current waveforms are generated by the numerical device simulators and the quasi-static equivalent circuit models based solely on the harmonic voltages given to them. Although the quasi-static equivalent circuit models utilize a constant “series resistance” that limits the forward conduction of the diode, only the numerical device simulator self-consistently accounts for the bias-dependent parasitic impedance of a simulated device’s undepleted epitaxial layer.

A. Large-Signal Sinusoidal Results

Before examining results from the harmonic-balance circuit analysis technique coupled to the numerical device and quasi-static equivalent circuit models, it is instructive to examine results from these two models when the device under investigation is subject to pure sinusoidal large-signal voltage excitations, i.e. in the absence of harmonic voltages impressed on the device as a consequence of its nonlinear interaction with the embedding circuit. Figures 8a and 8b show the current and voltage waveforms for the 5T1 SBV DC biased at -4.0 V and subject to a 5.0 V sinusoidal excitation voltage at 50 GHz and 100 GHz , respectively. Likewise, Figures 9a and 9b show the current and voltage waveforms for the Choudhury *et al.* HBV DC biased at 0.0 V and subject to a 2.0 V sinusoidal excitation voltage at 10 GHz and 100 GHz , respectively. For the 5T1

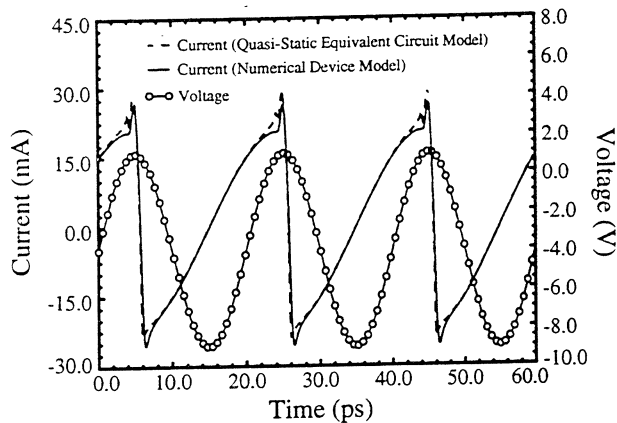


Figure 8a. Current waveforms for the UVA 5T1 GaAs SBV of reference [22] DC biased at -4.0 V and subject to 50 GHz, 5.0 V sinusoidal excitation.

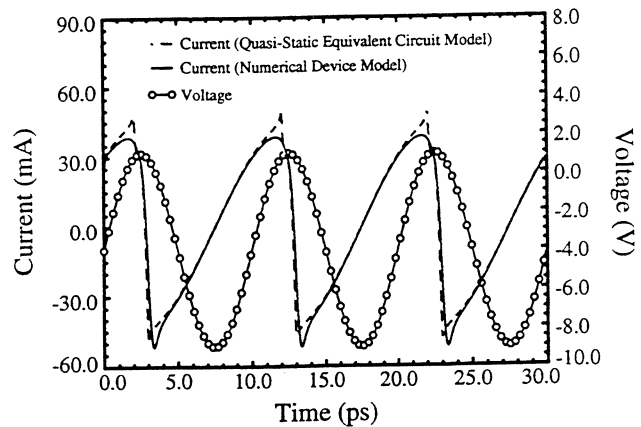


Figure 8b. Current waveforms for the UVA 5T1 GaAs SBV of reference [22] DC biased at -4.0 V and subject to 100 GHz, 5.0 V sinusoidal excitation.

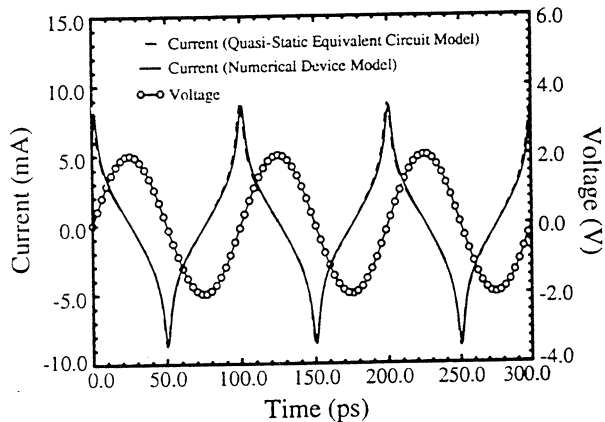


Figure 9a. Current waveforms for the GaAs/ $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$ HBV of reference [23] DC biased at 0.0 V and subject to 10 GHz, 2.0 V sinusoidal excitation.

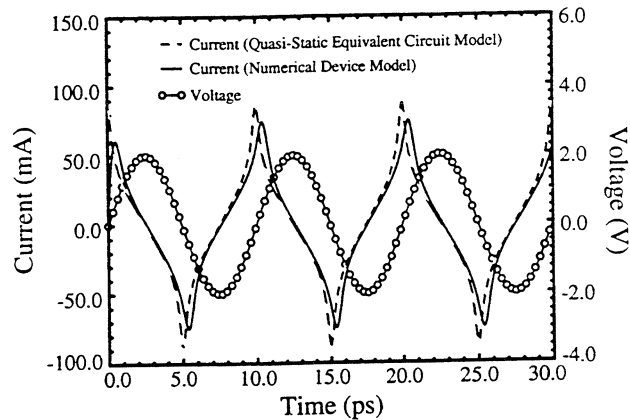


Figure 9b. Current waveforms for the GaAs/ $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$ HBV of reference [23] DC biased at 0.0 V and subject to 100 GHz, 2.0 V sinusoidal excitation.

SBV subject to the specified drive level, the current waveforms from the two device models begin to deviate at about 50 GHz with the deviations increasing with increasing frequency. For the Choudhury *et al.* HBV subject to the specified drive level, the current waveforms from the two device models begin to deviate at about 10 GHz with the deviations, again, increasing with increasing frequency.

At low frequencies (below about 10 GHz in the SBV and about 1 GHz in the HBV), when the current throughout the device is dominated by conduction current, small discrepancies between the results of the two models are observed. These discrepancies are attributed to errors in the curve-fits to the numerical device DC I-V and static C-V results. At higher frequencies, the current is dominated by displacement current in high field regions of the device (near the Schottky barrier or heterostructure barrier) and by conduction current in low field regions of the device (near the ohmic contacts). In the numerical device simulator, the conduction and displacement currents are balanced throughout the device in a self-consistent manner so that the total current versus position is constant. In the quasi-static equivalent circuit model, however, these currents are not self-

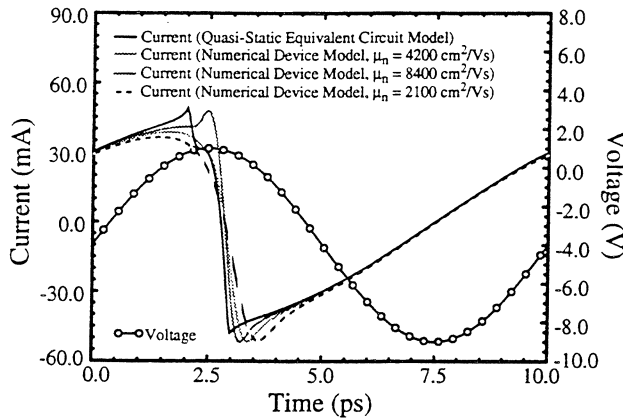


Figure 10. Current waveforms (one steady-state period) for the UVA 5T1 GaAs SBV of reference [22] DC biased at -4.0 V and subject to 100 GHz, 5.0 V sinusoidal excitation. The active region electron mobilities have been varied in the numerical device model as shown in the figure.

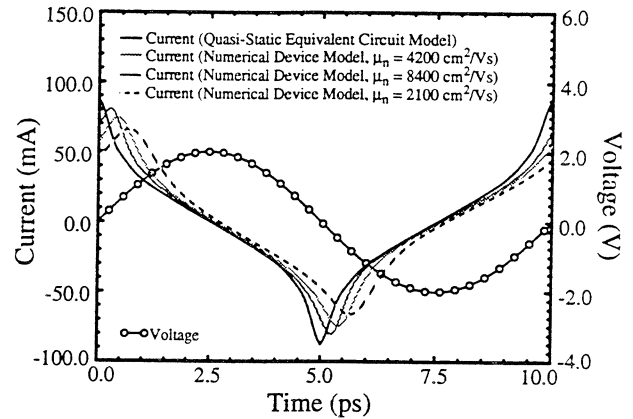


Figure 11. Current waveforms (one steady-state period) for the GaAs/Al_{0.7}Ga_{0.3}As HBV of reference [23] DC biased at 0.0 V and subject to 100 GHz, 2.0 V sinusoidal excitation. The active region electron mobilities have been varied in the numerical device model as shown in the figure.

consistently balanced. As a result, the displacement current in the high field regions of the device can greatly exceed the sustainable conduction current in the (relatively) low field regions of the device. As a result, the increasing current waveform deviations that we have observed with increasing frequency are a direct consequence of the current saturation phenomenon described in [25] and [22]. These deviations also increase with increasing drive level. Although attempts have been made to compensate for this lack of self-consistency in the quasi-static equivalent circuit models [26,27], the resulting models are device-specific, and require empirical fitting parameters and/or an analytical understanding of the device's internal physics.

In essence, the standard quasi-static equivalent circuit models assume an infinite electron mobility such that there is no limit to the allowable displacement current in the device. To further examine this concept, we have compared the quasi-static equivalent circuit models for the 5T1 SBV and the single barrier GaAs/Al_{0.7}Ga_{0.3}As HBV with their respective numerical device models assuming an active region mobility of μ_{n0} , twice μ_{n0} , and one half μ_{n0} . The results are shown in Figures 10 and 11 for drive levels identical to those previously specified. Clearly, as the active region mobility is increased from μ_{n0} , the current waveform from the numerical device simulator approaches that of the quasi-static equivalent circuit model. Alternately, as the active region mobility is decreased from μ_{n0} , the differences between the numerical device simulator current waveform and that of the quasi-static equivalent circuit model increase.

It is important to remember that the phenomenon described here is strictly a current saturation phenomenon. Since a constant, field-independent electron mobility has been utilized, saturation of the electron drift-velocity has not been accounted for. For long diodes, where a field-dependent electron mobility is justified, drift-velocity saturation could be directly incorporated in the numerical device models presented here. A better approach would be to utilize the drift-diffusion equations in conjunction with the energy balance equations to accurately account for saturation of the electron drift-velocity, even in relatively short diodes.

B. Harmonic-Balance Results

The differences in the sinusoidally pumped results, presented in the last section for the quasi-static equivalent circuit and numerical device models, are relatively small, at least below 100 GHz for the specified drive levels. Again, it is important to note that the differences increase with increasing frequency and drive level, and can be quite substantial above about 150 GHz. These relatively small differences, however, are magnified by the nonlinearity of the device when it is embedded in a circuit.

We investigate this phenomenon for the UVA 6P4 GaAs SBV doubler pumped at 100 GHz and the single barrier GaAs/Al_{0.7}Ga_{0.3}As HBV tripler pumped at 64 GHz using the harmonic-balance circuit analysis technique in conjunction with the two device modelling approaches[28-30]. Parasitic impedances for these frequency multipliers, external to the active regions of the devices, have been calculated using estimated chip parameters (ohmic contact resistivities of $2 \times 10^{-6} \Omega \text{cm}^2$, total device thickness of 4 mils, and square chip side lengths of 250 μm). For the 6P4 SBV doubler pumped at 100 GHz, the DC impedance is 0.614Ω and the impedances at the fundamental and second-harmonic frequencies are $1.491 + j1.016 \Omega$ and $1.924 + j1.549 \Omega$, respectively. For the HBV tripler pumped at 64 GHz, the DC impedance is 7.021Ω and the impedances at the fundamental and third-harmonic frequencies are $7.685 + j0.788 \Omega$ and $8.298 + j1.537 \Omega$, respectively.

At the incident pump powers of interest, near-optimum fundamental and third-harmonic circuit impedances for the zero DC biased HBV tripler have been estimated from [23] for a device DC parasitic impedance of 7.0Ω . The optimum fundamental impedances vary from $8.75 + j46.75 \Omega$ to $19.25 + j92.50 \Omega$ for incident pump powers ranging from 0 mW to 40 mW; the optimum third-harmonic impedances vary from $10.75 + j15.75 \Omega$ to $17.50 + j35.50 \Omega$ over the same pump power range. For the 6P4 SBV doubler, experimental DC bias values have been utilized[31]. Near-optimum fundamental and second-harmonic circuit impedances have been obtained for this doubler from the harmonic-balance circuit simulator coupled to the quasi-static 6P4 SBV equivalent circuit model. For simplicity, these SBV doubler circuit impedances have been optimized subject to the following constraints: 1) the real parts of the two harmonic impedances are equal and 2) the imaginary part of the second-harmonic impedance is half of the impedance at the fundamental. The optimized fundamental impedances vary from $23.5 + j207.0 \Omega$ to $48.0 + j223.0 \Omega$ for incident pump powers ranging from 7.5 mW to 47.0 mW. For both frequency multipliers, the high order harmonic circuit impedances are set to short-circuit impedances of $0.001 + j0.0 \Omega$. For the 6P4 SBV simulations, a DC circuit impedance of 1.0Ω has also been utilized.

The steady-state current and voltage waveforms for the 6P4 SBV doubler subject to a 100 GHz, 18.8 mW pump excitation are shown in Figure 12; similar waveforms for the HBV tripler subject to a 64 GHz, 20 mW pump excitation are shown in Figure 13. As previously noted, the relatively small differences in the results obtained from the two device modelling approaches are magnified by the nonlinearity of the device when it is embedded in a circuit. This is clearly evident from the harmonic-balance results shown in these figures. Although the current and voltage waveforms generated by the two device models have the same general shape, the sharpness, magnitudes, and phases of the waveforms differ substantially. As a result, the predicted absorbed powers, output powers, and multiplying efficiencies are substantially overestimated by the quasi-static equivalent circuit/harmonic-balance circuit simulation approach. For the 6P4 SBV doubler,

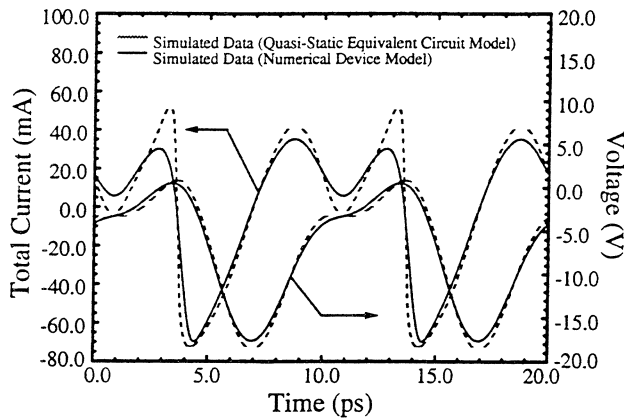


Figure 12. Steady-state harmonic-balance current and voltage waveforms for the UVA 6P4 GaAs SBV doubler of reference [22] DC biased at -7.03 V and subject to 100 GHz, 18.8 mW pump excitation.

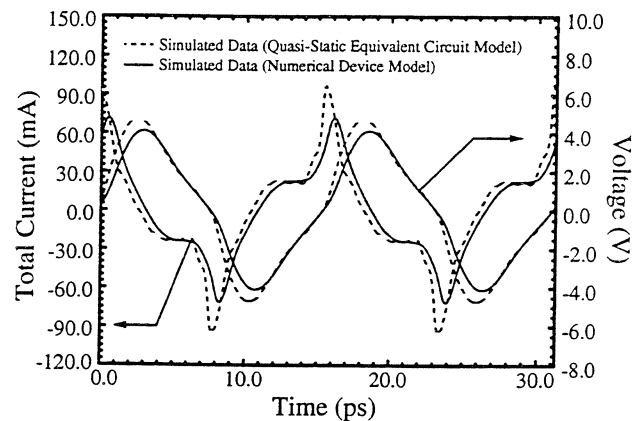


Figure 13. Steady-state harmonic-balance current and voltage waveforms for the single barrier GaAs/Al_{0.7}Ga_{0.3}As HBV tripler of reference [23] DC biased at 0.0 V and subject to 64 GHz, 20 mW pump excitation.

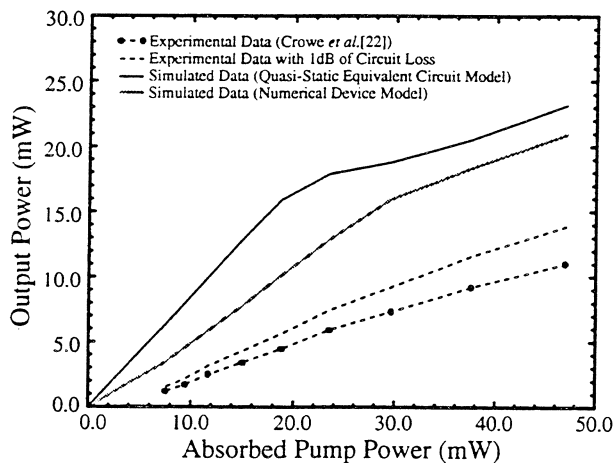


Figure 14. Experimental and simulated output power versus absorbed pump power results for the UVA 6P4 GaAs SBV doubler reference [22] subject to 100 GHz pump excitation.

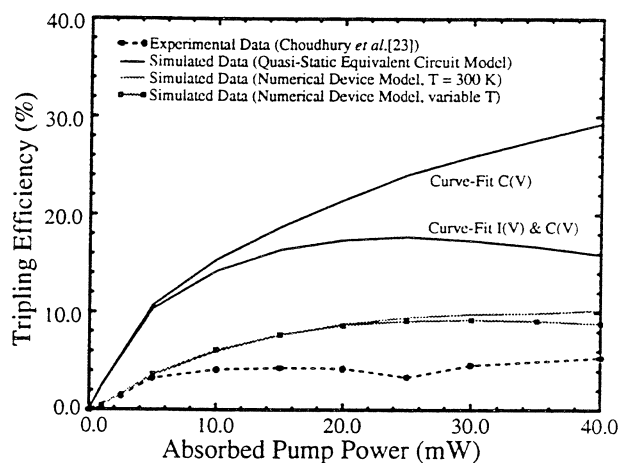


Figure 15. Experimental and simulated tripling efficiency versus absorbed pump power results for the single barrier GaAs/Al_{0.7}Ga_{0.3}As HBV tripler of reference [23] DC biased at 0.0 V and subject to 64 GHz pump excitation.

this can be seen clearly in Figure 14. This figure shows the experimental output power versus absorbed pump power results for this circuit, along with the simulated results obtained from the harmonic-balance circuit simulator coupled to the two device models. Similarly, Figure 15 shows the experimental tripling efficiency versus absorbed pump power results for the HBV tripler, along with the two simulated results. Also shown in Figure 15 is simulated data that includes thermal effects. For this particular whisker-contacted HBV tripler, the average active region temperature was estimated to be about 332 K at an incident pump power of 40 mW; this temperature translates into an active region electron mobility of about $3850 \text{ cm}^2/\text{Vs}$ which is about 92 percent of the 300 K mobility. Simulations including thermal effects have not been undertaken for the 6P4 SBV doubler since the average active region temperature was only found to reach about 320 K at an incident pump power of 50 mW. It is important to note that circuit losses have been incorporated

into the experimental tripling efficiency data shown in Figure 15[23]. For the 6P4 SBV doubler, the raw output power data has been plotted along with output power data assuming 1 dB of circuit loss. For all of the harmonic-balance simulations presented here, neither the breakdown voltage nor the critical breakdown field has been exceeded. For the 5T1 SBV doubler, however, it was found that the breakdown voltage is exceeded at relatively low incident pump power levels when near-optimum circuit impedances are assumed. This result indicates that careful modelling of avalanche breakdown may be required to accurately simulate the performance of the 5T1 SBV doubler.

Overall, the harmonic-balance results presented here indicate that the physics-based numerical device models for SBVs and HBVs provide significantly improved correlation to experimental data when compared to typical quasi-static equivalent circuit models. The remaining discrepancies between simulation and experiment are attributed mainly to the inaccurate assumption that the multiplier circuits present optimum impedances to the active devices. The accurate determination of active device embedding impedances would be of great benefit to the analysis and design of frequency multipliers as well as other highly nonlinear circuits.

V. Conclusions

In conclusion, accurate and efficient simulations of the large-signal time- and temperature-dependent characteristics of SBV and HBV frequency multiplier circuits have been obtained by combining a novel harmonic-balance circuit analysis technique with physics-based numerical device simulators. This approach to the analysis and design of highly nonlinear millimeter and submillimeter wave circuits allows for the careful examination of the internal physical phenomena occurring in a wide array of highly nonlinear active devices. This is particularly important at high frequencies and for devices whose terminal characteristics are not amenable to description via analytical expressions. Even when such an analytical description is possible or when curve-fit DC results from a physics-based numerical device simulator are utilized, the resulting quasi-static equivalent circuit model lacks self-consistency and neglects important high frequency nonstationary carrier dynamic effects. Only the general approach presented in this paper adequately addresses these issues and allows for the accurate and self-consistent modelling of phenomena such as current saturation, the bias-dependent parasitic impedance and shunting capacitance of device undepleted regions, electron velocity saturation, and electron mass-inertial effects[25]. It is our belief that analysis and design approaches as advocated in this paper are essential to the development of efficient and reliable circuits operating into the terahertz frequency range.

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