

A NEW SIS MIXER FOR THE 2-MM BAND

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ABSTRACT

This paper describes a tunable SIS mixer for the (non-standard) 124-190 GHz waveguide band. The mixer uses a series array of Nb/Al-Al₂O₃/Nb junctions in a suspended stripline on a quartz substrate. At each end of the substrate, the stripline is coupled to a full-height waveguide. The signal and local oscillator power enter from one waveguide, while the other contains a non-contacting short-circuit which directly tunes out the series inductance of the array of junctions. Separate integrated tuning circuits on the individual junctions tune out the junction capacitance.

The dimensions of the substrate and stripline are such that the SIS junctions can either be fabricated with the stripline as a single integrated circuit, or separately on a small (0.005" x 0.010") flip-chip which is subsequently soldered in place on the stripline. The design should be suitable for scaling to ~400 GHz.

A receiver using this mixer has given an overall receiver noise temperature of 21-30 K DSB over the 130-170 GHz radio astronomy band. Typical values of mixer noise temperature and conversion loss are $T_M = 6.5$ K (DSB) and $L = -0.1$ dB (DSB).

By adding a tuner in the input waveguide behind the transition to stripline, it is possible to tune the mixer for single sideband operation. Mixers of this type are now in operation on the NRAO 12-m telescope at Kitt Peak.

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INTRODUCTION

Integrated tuning circuits are now widely used to tune out the capacitance of the junctions in superconductor-insulator-superconductor mixers. However, the series inductance of the junction (or array of junctions) can also limit the performance of a mixer. This inductance is usually tuned out as part of the overall impedance matching by one or two adjustable waveguide tuners [1, 2], although designs without adjustable tuners have also been successful [3, 4, 5]. In the present work we have attempted to design a versatile SIS mixer in which a mechanical tuner specifically allows the series inductance of the junctions to be tuned out, while the junction capacitance is tuned out by integrated tuning elements. Additional design requirements for this mixer were as follows:

- (i) The mixer should be able to use SIS junctions on a small chip (e.g., 0.005" x 0.010") or fabricated directly on a larger RF substrate. This requirement is a reflection of the fact that SIS device fabrication is still not a highly reproducible process, and when a successful wafer is made, it is desirable to have a large number of useful devices. (To this end, we normally include on each mask set a number of small SIS chips in addition to larger fully integrated designs.) A practical consequence of using small SIS chips is that the RF circuit must include bonding pads, typically 0.003" x 0.004".
- (ii) Full-height waveguide should be used in the mixer block. This simplifies fabrication and allows the use of dumbbell-type tuners which have low loss and are free of resonances across the full waveguide band [6].
- (iii) For compatibility with NRAO's existing SIS receivers, the tuner(s) should emerge from the face of the mixer block opposite that containing the input waveguide.
- (iv) This mixer should also serve as a low-frequency prototype for future higher frequency designs. The mixer design should therefore be suitable for scaling for operation up to at least 400 GHz.

Most of these requirements are met by one or other of two existing SIS mixer designs, the GISS Type-D mixer and the NRAO 401 mixer [7, 1], and the new design incorporates the desirable aspects of each. The principal disadvantage of the Type-D design is its use of reduced (1/4) height waveguide, which is necessary to provide an acceptably low and frequency-independent embedding impedance across the waveguide band when the SIS junctions are mounted across the waveguide [8, 9, 10]. The NRAO 401 mixer's significant shortcoming is the difficulty of mounting its cantilevered stripline probes on the substrate with sufficient precision.

The new NRAO-581 mixer is shown in Fig. 1. The incoming signal and LO power are coupled into the suspended stripline from the input waveguide via a broadband probe type of transducer [3]. To accommodate future applications up to 183 GHz, a non-standard waveguide size was chosen,

0.058" x 0.029", whose nominal operating band is 124-190 GHz. (Using an extension of the EIA waveguide numbering system, we refer to this as WR-5.8 waveguide³.)

Waveguide tuner 1 provides an adjustable reactance in series with the junctions. The two-section matching circuit just below the chip in the figure compensates for the equivalent circuit of the chip and, in conjunction with waveguide tuner 1, provides the desired embedding impedance at the SIS array. The design was originally intended to have a fixed waveguide short-circuit in place of tuner 2. However, it was found that the second tuner allowed the mixer to be tuned for true single-sideband operation, which can be of great benefit in spectral line radio astronomy.

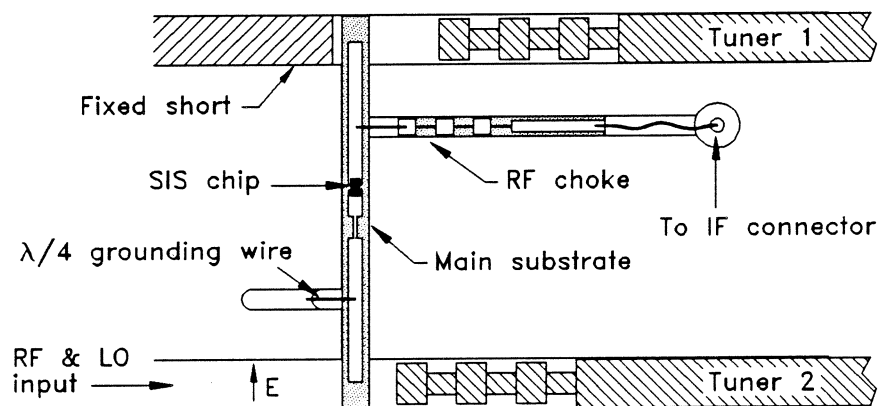


Fig. 1. NRAO-581 130-170 GHz SIS mixer. The waveguide size is WR-5.8 (0.058" x 0.029").

IF and DC connections to the SIS junctions are made via quarter-wavelength gold wires soldered to the suspended striplines either side of the chip. One wire is grounded to the block, and the other is connected to a microstrip RF choke on a second quartz substrate.

The 0.005" x 0.010" SIS chip is initially fabricated on a 0.010" thick quartz wafer, and is reduced to a thickness < 0.002" during the dicing process. It is then soldered to the stripline on the main substrate.

³In the EIA WR-# scheme, # is the inside width of the waveguide in hundredths of an inch, rounded to a whole number. For small non-standard waveguides it is logical to add a decimal point, allowing #.# to indicate the waveguide width to the nearest thousandth of an inch.

DESIGN OF THE MIXER

The choice of embedding impedances follows the procedure described in [1]. The RF source impedance, R_S , and IF load impedance were chosen, for convenience, as 50 ohms. For junctions with a given J-V curve (J is the current per unit area), it is then possible to find a value of normal resistance for which the mixer noise temperature is near its minimum, the conversion loss close to unity, and the input VSWR moderately low.

SIS junction design

For typical Nb/Al-Al₂O₃/Nb SIS mixers, this optimum normal resistance⁴ $R_N = 2.4 R_S (100/f(\text{GHz}))^{0.72}$. Accordingly, the present design assumes $R_N = 90$ ohms (for the series array of junctions). Following [1], a target value of $\omega R_N C = 2.7$ was used, corresponding to a critical current density $J_C = 2900$ A/cm² (this assumes stray (overlap) capacitance to be small compared with the junction capacitance). Following [11], the specific capacitance of the junctions is taken as 45 fF/ μm^2 .

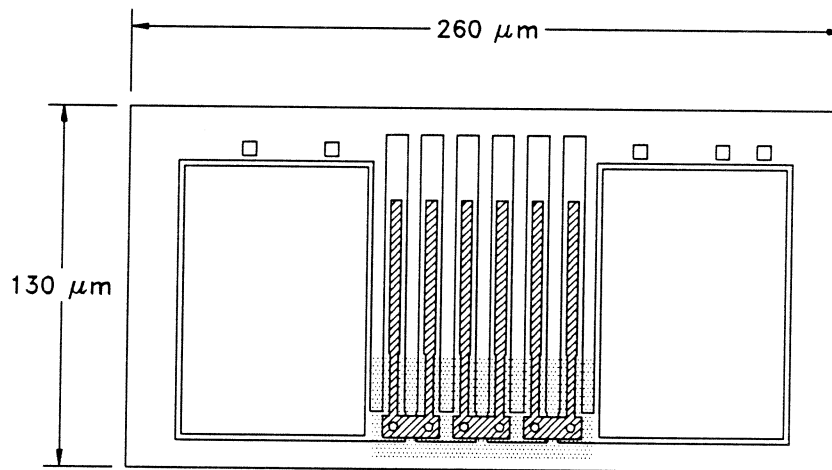


Fig. 2. Details of the SIS chip. Dotted shading indicates a 450 nm thick layer of SiO between the base electrode and the interconnection layer.

Details of the SIS chip are shown in Fig. 2. The capacitance of each junction is tuned out by a short (inductive) parallel-plate transmission line terminated in a quarter-wave open-circuit stub of very low characteristic impedance [12]. The six junctions each have a diameter

⁴In [1] it was found that $R_N = 2.5 R_S (100/f(\text{GHz}))$. A more accurate mixer analysis, including five small-signal sidebands, has since shown that the formula given in the text is a better approximation [5].

of $2.3 \mu\text{m}$ and normal resistance of 15 ohms. The quarter-wave open-circuit stubs are $57 \mu\text{m}$ long and have a characteristic impedance of 2.6 ohms. The tuning inductors are each $31 \mu\text{m}$ long, with a 450 nm thick SiO dielectric over 85 nm of Nb_2O_5 , and have a characteristic impedance of 19 ohms. Their electrical length is only 16° , so they can be regarded as lumped-element inductors.

Equivalent circuit of the SIS chip

The equivalent circuit of the SIS chip mounted in the suspended stripline was determined from measurements on 69 x scale models using a vector network analyzer. The measurements are well approximated up to ~ 200 GHz by the circuit in Fig. 3, where both reference planes TT' are at the center of the chip. The form of the equivalent circuit was chosen so its elements would represent the physical energy storage mechanisms in the actual circuit, thereby making the element values independent of frequency from DC to the highest frequency of interest. The dominant element in this circuit is the inductance, whose reactance at 150 GHz is 58 ohms.

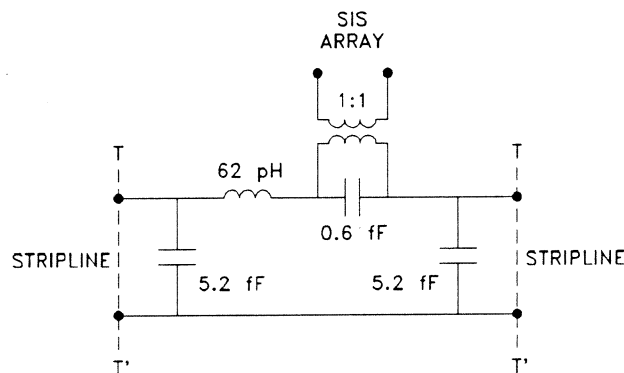


Fig. 3. Equivalent circuit of the SIS chip in suspended stripline. (Element values are for the real mixer, not the scale model.)

Main substrate

The RF circuit on the main fused quartz substrate is a Cr-Au suspended stripline, as shown in Fig. 4. Using the chip equivalent circuit in Fig. 3, the characteristic impedances Z_1 and Z_2 , and lengths L_1 and L_2 , were chosen to give a good match to the RF resistance of the SIS array over the desired 130-170 GHz band. Fig. 5 shows the expected input reflection coefficient as a function of frequency under the following assumptions: (i) Tuner 1 (Fig. 1) is adjusted at each frequency to tune out the series inductance of the array of junctions. (ii) Tuner 2 is set

to match the waveguide to the 50-ohm stripline⁵. (iii) When operating as a mixer, the RF small-signal impedance of each junction is 8.3 ohms (50 ohms for the whole array) in parallel with the junction capacitance.

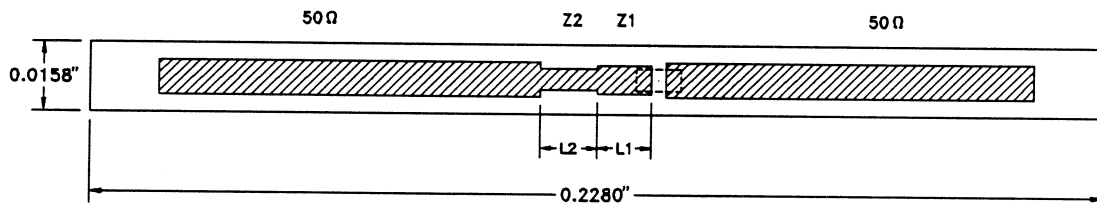


Fig. 4. The main substrate is 0.005" thick fused quartz with Cr-Au metallization. The SIS chip is soldered across the gap as indicated by the dashed outline. For this design $Z_1 = 60 \Omega$, $Z_2 = 70 \Omega$, $L_1 = 351 \mu\text{m}$, and $L_2 = 325 \mu\text{m}$.

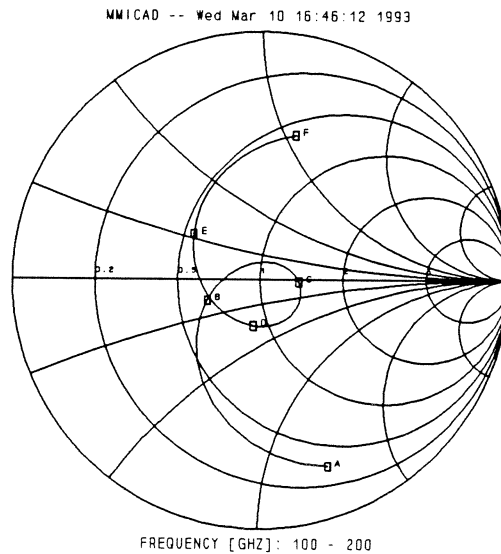


Fig. 5. Input reflection coefficient from 100 to 200 GHz when tuner 1 is adjusted to tune out the series inductance of the array of SIS junctions. $Z_0 = 50 \Omega$. Markers are every 20 GHz.

⁵With a fixed short-circuit, the transducer has a return loss > 20 dB over the whole waveguide band.

JUNCTION FABRICATION

The Nb/Al-Al₂O₃/Nb trilayers were deposited on Infrasil 301 fused quartz wafers 0.010 inches thick using a process similar to that described in [11, 13], but with the following differences: (i) During Nb deposition, the DC magnetron power was held constant while the Ar pressure was adjusted to maintain constant current. This results in a constant deposition rate and uniform film stress from wafer to wafer over the life of the sputtering target. (ii) Nb₂O₅ was formed in the desired regions by anodization *before* patterning the trilayer. This obviates the need for the anodizing lines required to interconnect all the areas to be anodized if the trilayer is patterned before anodization.

EXPERIMENTAL RESULTS

For the mixer whose results are described here, a series array of six junctions was used, each of nominal diameter 2.8 μm . The I-V curve with and without LO power applied is shown in Fig. 6, from which a normal resistance of 58 ohms is deduced. Based on the nominal diameter, $J_c = 2800 \text{ A/cm}^2$.

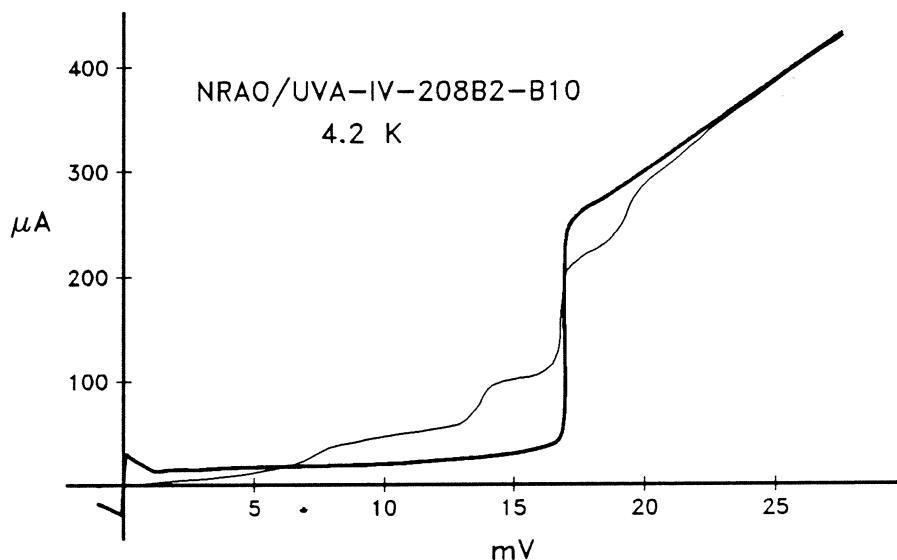


Fig. 6. I-V curve of the mixer with and without LO power. The LO frequency is 140 GHz.

The mixer was tested in a liquid helium cooled vacuum cryostat [14] containing 4.2 K IF calibration components, similar to that described in [7]. The incoming RF signal enters the cryostat through a plastic film

vacuum window supported by polystyrene foam [15]. It passes through a PTFE infrared filter at 77 K into a scalar feed horn at 4.2 K. LO power is injected through a 20 dB branch-line directional coupler, also at 4.2 K. A 1.4 GHz IF was used, and all measurements were made with a 50 MHz bandwidth. The IF noise temperature, including a coaxial switch, two isolators, and a directional coupler, was 6.5 K. No IF impedance transformer was used, and no external magnetic field was applied to the mixer.

Using a chopper wheel to switch the input beam between room temperature and 77 K loads, and a Y-factor meter synchronized to the chopper wheel, the two waveguide tuners, LO power and mixer bias voltage were adjusted for minimum receiver noise temperature at each frequency. Fig. 7 shows the DSB receiver noise temperature as a function of frequency. The dashed curve in this figure is for a receiver using the same type of mixer block with an SIS chip of comparable normal resistance but with integrated tuners designed for 90-120 GHz. The comparison demonstrates the effectiveness of the integrated tuning circuits.

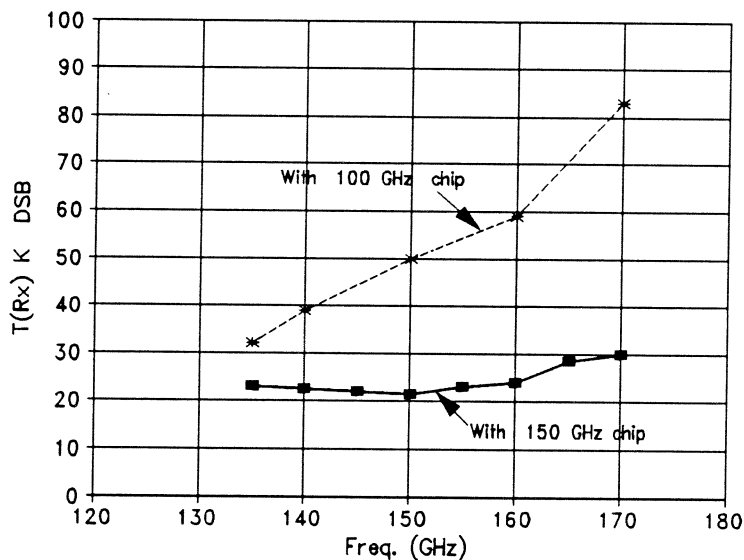


Fig. 7. DSB receiver noise temperature measured outside the cryostat. The dashed curve is for a receiver with the same type of mixer but with an SIS chip designed for 90-120 GHz.

The mixer's conversion loss, noise temperature, and output resistance were deduced from measurements with RF hot and cold loads outside the cryostat at the input of the receiver, and with IF hot and cold loads inside the cryostat connected to the input of the IF amplifier by the coaxial switch. Typical values are: $L = -0.1$ dB (DSB), $T_M = 6.5$ K (DSB), and $R_{IF} = 145$ ohms.

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