

SUBMICROMETER DEVICES AND MONOLITHIC FUNCTIONS USING  
InAlAs/InGaAs HETEROSTRUCTURES

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ABSTRACT

A monolithic integrated circuit technology is reported using submicrometer HEMT's made with InAlAs/InGaAs heterostructures. The maximum oscillation frequency measured for  $0.25\mu\text{m}$  devices is 148GHz. Good characteristics are also shown for devices subjected to all the steps of the integrated technology.

Monolithic heterostructure oscillators, doublers and mixers have been fabricated with this technology. They are designed for fundamental signal generation at 90GHz, frequency doubling to 180 GHz and mixing at 90 GHz. An analysis of the design procedures and characteristics is presented.

This first generation novel heterostructure monolithic circuits are designed for implementation in receiver/sensor components operating in the THz region.

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## 1. Introduction

$\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  High Electron Mobility Transistors (HEMT's) have demonstrated extremely high cutoff frequencies ( $f_T$ ) and very low noise figures [1]. The addition of excess Indium in the channel results in strained devices with better carrier confinement and improved characteristics [2]. Double-heterojunction strained  $\text{InAlAs}/\text{In}_{0.65}\text{Ga}_{0.35}\text{As}$  HEMT's with  $1\mu\text{m}$  long gates showed even further enhancement in carrier confinement and demonstrated lower output conductance than single channel devices with the same In content [3]. This paper, presents the technology and electrical characteristics of submicron strained  $\text{InAlAs}/\text{InGaAs}$  HEMT's and heterostructure monolithic integrated circuit functions made with them. Double and single heterojunction designs were used for these studies.

Monolithic integrated circuits use primarily conventional MESFET technology on GaAs. Recently  $\text{AlGaAs}/\text{GaAs}$  and pseudomorphic  $\text{AlGaAs}/\text{InGaAs}/\text{GaAs}$  devices have been implemented in integrated designs and very encouraging results were obtained in terms of bandwidth [4] and noise figure characteristics [5]. Unlike these GaAs based approaches,  $\text{InAlAs}/\text{InGaAs}$  designs are based on InP substrates and as mentioned already, discrete components made with them demonstrate excellent properties. Their integrated characteristics have not, however, been fully explored. Only few reports exist on this subject [6] which could lead to new avenues for analog applications.

First integrated designs using  $0.8\mu\text{m}$  long-gate  $\text{InAlAs}/\text{InGaAs}$  HEMT's have demonstrated the possibility of building high gain amplifier blocks at X-band [7] and broadband control circuits up to 26.5 GHz [8]. Submicron HEMT's with optimized design and technology characteristics are, however, expected to perform

up to frequencies which lie in the submillimeter frequency region. A maximum oscillation frequency ( $f_{max}$ ) of 405 GHz [9] already has been reported for discrete devices and it is expected that the  $f_{max}$  limits could be pushed above 500 GHz. These devices are consequently potential candidates for building basic functions such as oscillators, multipliers and mixers operating at extremely high frequencies. Space based sensor applications where gas molecule resonances are studied at several hundred GHz could consequently take direct advantage of monolithic integrated circuits made with InAlAs/InGaAs. Circuits of this type are currently under study and first results on their technology and design are reported in this paper.

Section 2 describes the technology of submicron discrete and integrated monolithic circuits. Integrated designs for oscillators, doublers and mixers are reported in Sections 3, 4 and 5, respectively.

## 2. Technology and Electrical Characteristics of Submicron InAlAs/InGaAs HEMT's for Monolithic Integrated Applications.

A cross section of  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_x\text{Ga}_{1-x}\text{As}$  InAlAs/InGaAs HEMT's is shown in Fig.1. The design corresponds here to the double heterojunction (DH) scheme [3] which is found to show larger carrier occupation in the strained quantum well and therefore better carrier confinement than single channel designs. The channel where the Two-Dimensional Electron Gas (2DEG) is formed has a high Indium composition ( $x$ ) which exceeds the lattice matched ( $x=0.53$ ) value. Unlike single channel designs employing only one donor layer between gate and channel, the DH-HEMT has a second donor layer in the bottom. This provides more carriers

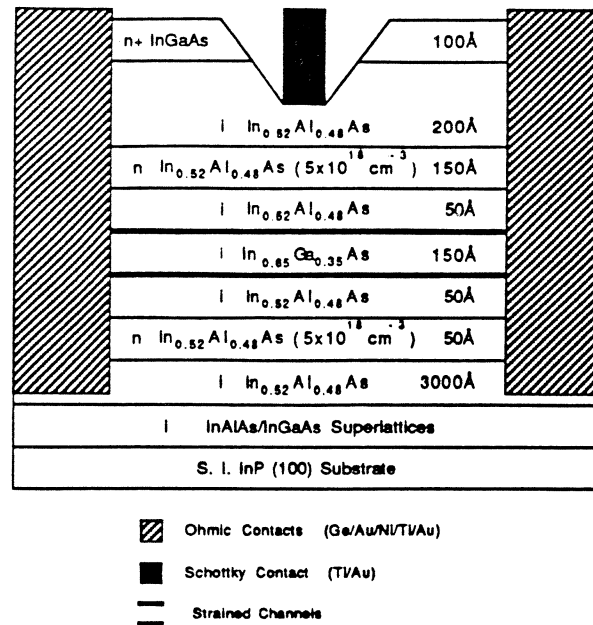


Figure 1 Cross section of double-heterojunction InAlAs/InGaAs HEMT.

and requires special attention in its design (smaller thickness than the top donor layer and appropriate doping) to avoid parasitic conduction.

The introduction of additional Indium in the channel improves the device properties. A transconductance and cutoff frequency improvement has already been reported by increasing the In content from 53% to 65% [2]. Further increases of Indium do not seem to enhance further the device properties. Our recent studies have for example demonstrated that devices with 75% or more In have smaller  $f_T$  and  $f_{max}$  values. By way of example an increase of In from 60% to 80% in 5% steps shows  $f_{max}$  values of 40GHz, 52GHz, 62GHz, 47GHz and 50GHz, respectively. The degradation of device characteristics with In content above certain value is related to their growth mode and the resulting interface characteristics.

Based on the above analysis, it was concluded that a 65% Indium content in the channel is a good compromise for improved electrical characteristics and controlled growth conditions suitable for integrated applications. The latter demand good

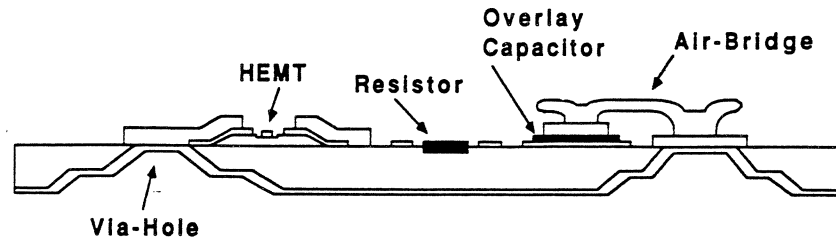


Figure 2 Cross section of heterostructure Monolithic Integrated Circuit using InAlAs/InGaAs HEMT's.

wafer uniformity and reproducibility to guarantee the compliance of performance with the predicted design characteristics.

A cross section of a InAlAs/InGaAs heterostructure monolithic integrated circuit is shown in Fig.2. Their technology of fabrication uses wet-etched ( $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}-1:1:38$ ) mesas for isolation. This solution has an etch rate of  $20\text{\AA}/\text{sec}$  and results in small orientation dependence and no undercut. The quality of ohmic contacts (Ge/Au/Ni/Ti/Au) was improved from  $0.3\Omega\text{mm}$  in first runs to  $0.1\Omega\text{mm}$  by increasing the cap doping density ( $5 \times 10^{18}\text{cm}^{-3}/100\text{\AA}$  instead of  $3 \times 10^{18}\text{cm}^{-3}/200\text{\AA}$ ), and reducing the i-layer thickness of InAlAs from  $400\text{\AA}$  to  $200\text{\AA}$ ; the smaller thickness helps also in increasing the device transconductance. An image reversal lithography (Shipley 5214) was used for better reproducibility, edge definition and uniformity of the ohmic contacts; the chlorobenzene based lift-off originally employed, was eliminated for this step.

The submicron gate was defined using single  $4500\text{\AA}$  thick PMMA layer exposed by E-beam at  $5.5\text{nC}/\text{cm}$ ,  $25\text{kV}$ . A citric acid etchant was used for gate recess in a mixture of 11:1:44 with  $\text{H}_2\text{O}_2$  and  $\text{H}_2\text{O}$ . This results in relatively low etch rates

( $\sim 300\text{\AA}/\text{min}$ ) and acceptable control of recess depth. The HEMT gates (Ti/Au) fabricated in this way have a length of 0.2 to  $0.25\mu\text{m}$ .

The reticle for the investigated monolithic integrated functions was relatively large ( $6.3\text{mm} \times 6.7\text{mm}$ ) to allow simultaneous fabrication and comparison of characteristics of several functions. Submicron devices of different topology were necessary in order to satisfy the distinct requirements of each function. The reticle was for this reason subdivided in 11 subfields and some layout optimization was necessary to comply with the E-beam subfield size while maintaining the appropriate circuit topology.

Following the gate definition, a TiAu layer was deposited for the bottom plates of overlay capacitors. A thick  $\text{SiO}_2$  layer  $\sim 2500\text{\AA}$  was deposited by lift-off for the overlays. The sputtered lift-off technique developed specifically for the MMIC's allows selective overlay fabrication without deposition on the active area of the device and therefore no influence on its characteristics.

Active bias resistors for gate bias were recessed separately from the devices in order to control their values in the  $5\text{K}\Omega$  range. Air-bridges were fabricated in a two-step process. The wafers were then thinned down to  $100\mu\text{m}$  (thickness for which all microstrip stubs were designed) and diced. The integrated circuits were finally mounted and bonded in a specially designed test fixture operating from 70 to 100 GHz.

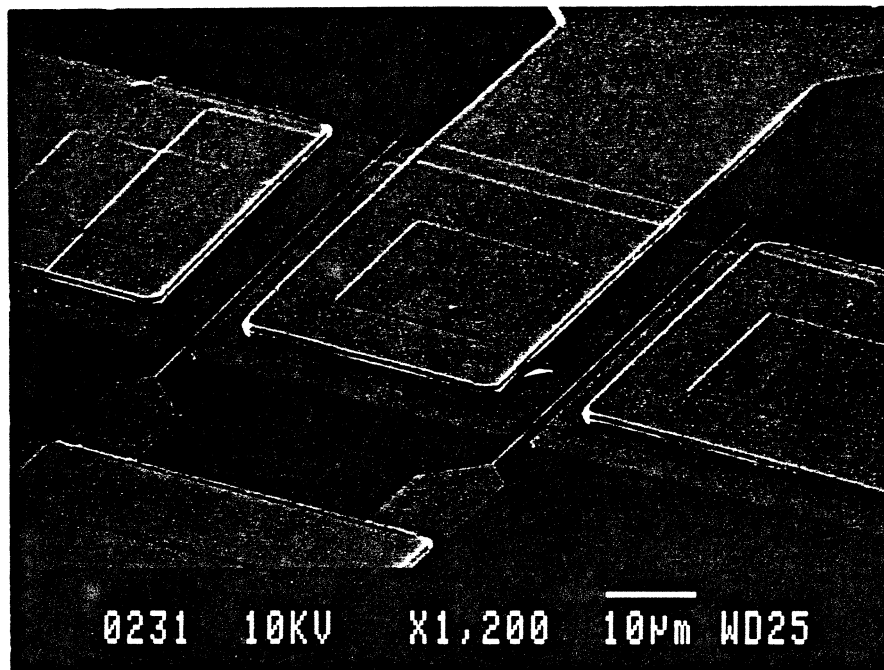


Figure 3 Photograph of submicron InAlAs/InGaAs HEMT in a monolithic integrated circuit.

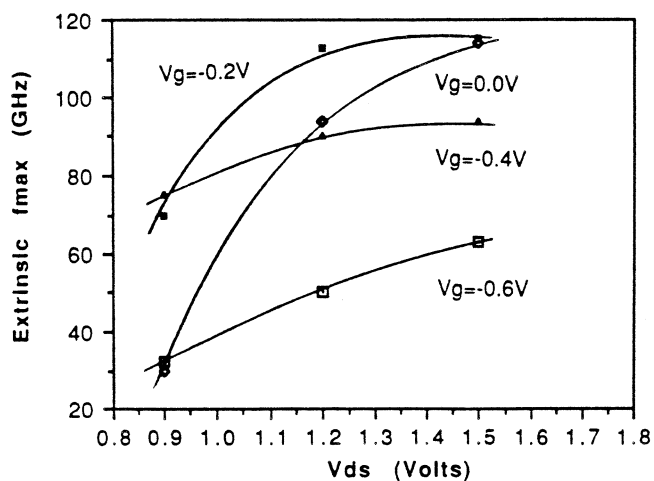


Figure 4 Bias dependence of current gain cutoff frequency ( $f_T$ ) and maximum oscillation ( $f_{max}$ ) frequency of a single channel (60%) HEMT from “integrated-circuit” wafer.

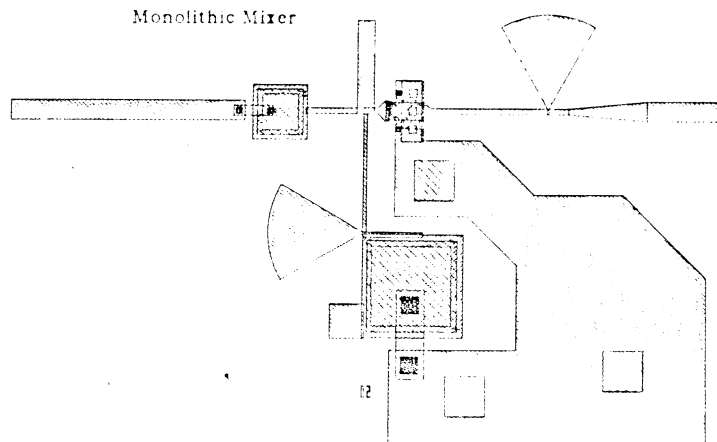
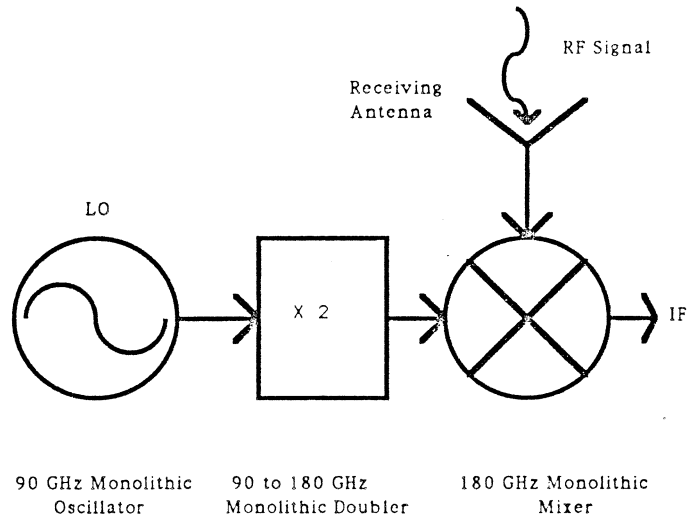
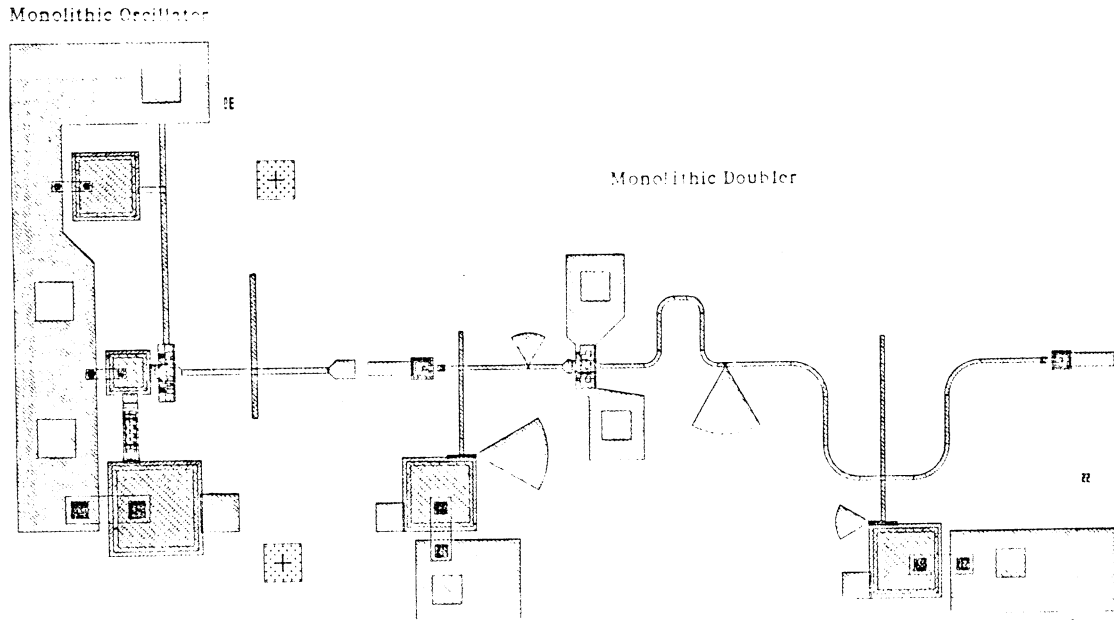
A photograph of the submicron InAlAs/InGaAs HEMT of an integrated circuit is shown in Fig. 3. Its gate is  $0.2\mu\text{m}$  long. Fig. 4 shows the bias dependant  $f_T$  and  $f_{max}$  characteristics of such an integrated device fabricated with single channel (60% In) design. The maximum  $f_T$  and  $f_{max}$  values are 100GHz and 115GHz respectively. The device had 12dB gain at 26.5GHz. Better performance ( $f_T = 82\text{GHz}$ ,  $f_{max} = 148\text{GHz}$  with 14dB of gain at 26.5GHz) could be obtained with a double heterojunction design of 65% In composition in the channel.

### 3. 90GHz Monolithic Oscillator Design Using InAlAs/InGaAs HEMT Technology.

The monolithic oscillator design was intended for implementation in a more complex integrated function as shown in Fig. 5. The frequency of the local source (monolithic oscillator) is doubled and subsequently mixed with the receiving signal. The resulting IF lies in the microwave region (1.0GHz to 10.0GHz) and can be processed using conventional existing technologies. Although fundamental oscillation frequencies should in principle be feasible in the several hundred GHz region using this technology, the design frequency of this first iteration was selected to be 90 GHz. This allows immediate use of presently available monolithic device characteristics and allows identification of possible problems related with such realizations.

The oscillator design was based on measured small-signal characteristics of submicron HEMT's. A common source topology was selected with capacitive feedback in the gate and a combination of capacitive-inductive feedback in the source to induce oscillation conditions.





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Figure 5 Schematic and layout of monolithic integrated sensor module.

Oscillation can be initiated if the following conditions are satisfied:

$$|\Gamma_{in}| \times |\Gamma_{osc}| \geq 1$$

$$\leq \phi_{in} + \leq \phi_{osc} = 0$$

where  $|\Gamma_{in}|$ ,  $\phi_{in}$  and  $|\Gamma_{osc}|$ ,  $\phi_{osc}$  denote magnitude and phase of the reflection coefficient at a reference plane looking towards the load and oscillator, respectively. This condition, is equivalent to a total resistance ( $R_{tot} = R_{in} - R_{osc}$ ) and reactance ( $X_{tot} = X_L + X_{osc}$ ) equal to zero. Additionally to guarantee sustained steady-state oscillation it is necessary to satisfy the following conditions:

$$\frac{\partial R_{tot}}{\partial \omega} > 0 \quad , \quad \frac{\partial X_{tot}}{\partial \omega} > 0$$

As in every monolithic realization it is particularly important to aim towards process tolerant designs where the oscillation and steady-state conditions can be satisfied over a broad enough frequency range independent of active or passive element variations in their characteristics.

The integrated oscillator chip was fabricated using the monolithic submicron HEMT technology described in Section 2. A photograph of the fabricated monolithic chip is shown in Fig. 6.

The inductive feedback elements were realized using  $16\mu\text{m}$  wide microstrips with  $90\Omega$  characteristic impedance on  $100\mu\text{m}$  thick substrates. A  $50\Omega$  output port was considered and integrated matching was provided using again microstrip stubs. Overlay capacitors are used either for feedback or for RF grounding the bias pad of the gate. This pad was connected to the gate through an integrated  $5\text{k}\Omega$  resistor. Via holes are finally incorporated in the design for reducing parasitic inductances

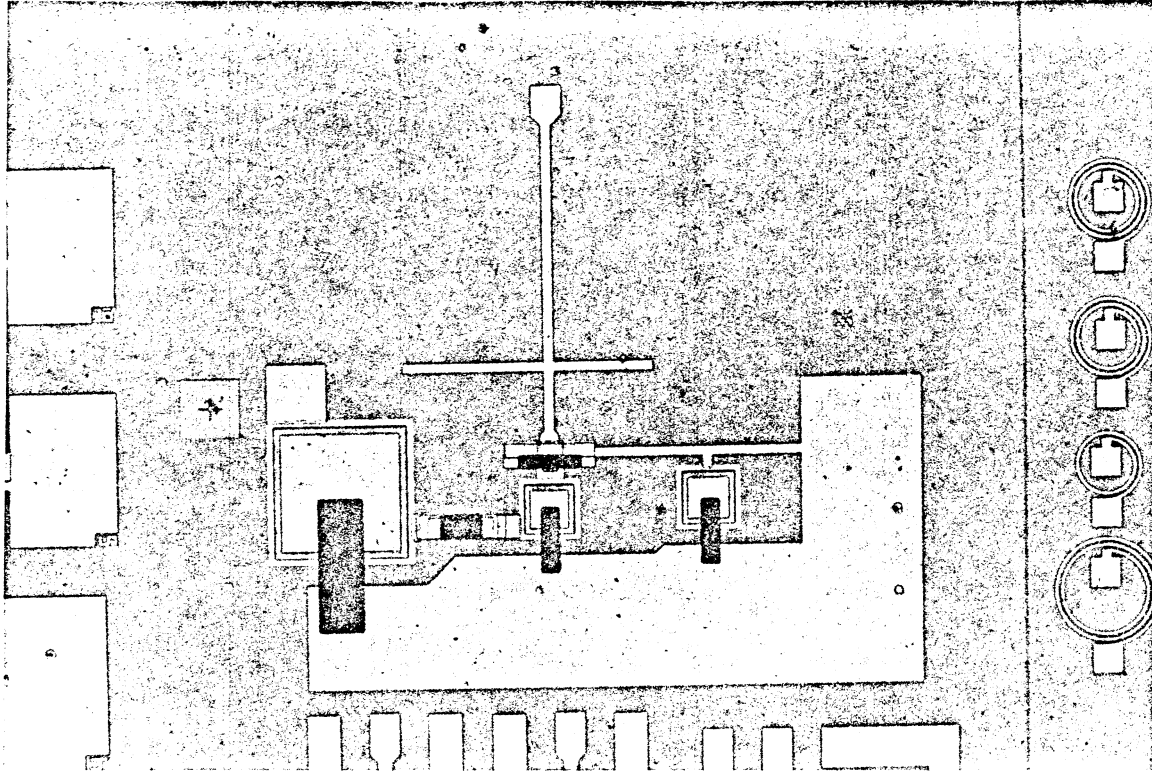


Figure 6 90GHz Monolithic Integrated Oscillator chip.

of the chip to ground.

#### 4. 90GHz to 180GHz Monolithic Doubler using InAlAs/InGaAs HEMT Technology.

Signal multiplication is usually performed using two-terminal multiplier diodes. The high frequency characteristics of HEMT's suggest the possibility of three-terminal devices too for such applications. In fact, the transistor approach can allow larger bandwidth and better DC to RF efficiency than diodes which normally require relatively high power drive levels.

For multiplier applications, similarly to high efficiency power amplifiers, the HEMT's are operated with dc gate bias voltage ( $V_{gb}$ ) close to pinch-off ( $V_p$ ), i.e. under class B conditions. To obtain a high frequency harmonic at the output, the load is tuned at the desired harmonic. Suitable networks need to be incorporated at the gate and drain terminals to short-circuit all out-of-band harmonics.

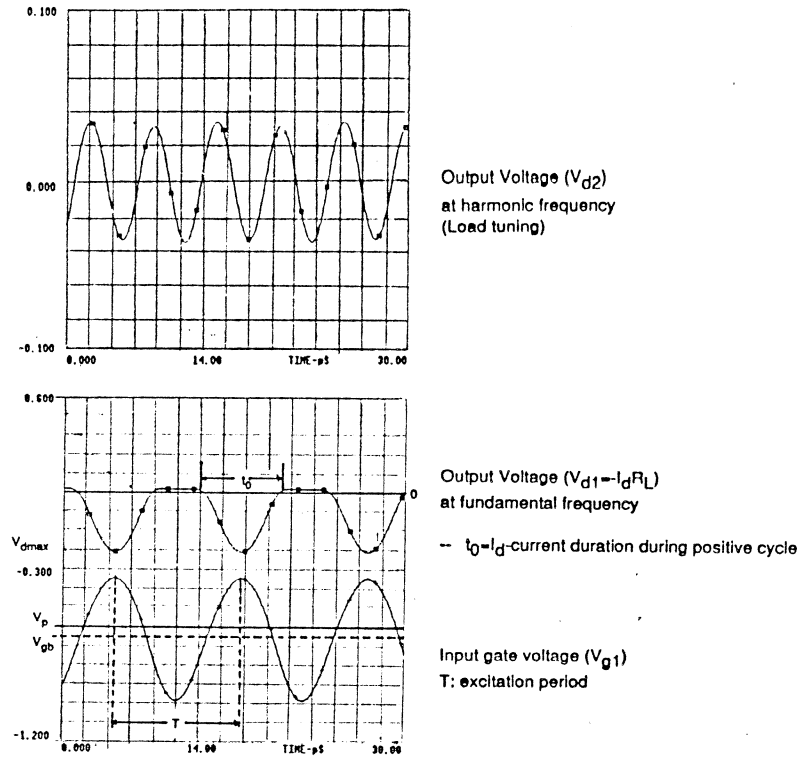


Figure 7 Voltage waveforms at various terminals of a 90GHz to 180GHz doubler.

A harmonic-balance technique (LIBRA<sup>R</sup>) was used to analyze the doubler characteristics. The time domain characteristics of the output/drain voltage  $V_{d1}$ ,  $V_{d2}$  at the fundamental and doubled frequency respectively, as well as, the input/gate voltage ( $V_{g1}$ ) are given in Fig. 7; the frequency of the  $V_{d2}$  waveform across the load is consequently 180GHz. The amplified input voltage  $V_{g1}$  results in a waveform  $V_{d1}$  which ideally should be set to zero during the negative voltage ( $V_{g1} \geq V_p$ ) excursion. This is not, however, true in practice, due to the high frequency operation displacement current which leaks through the gate capacitance and contributes to a  $V_{d1}$  “parasitic” signal (positive “square-like” waveform in Fig 7). The time duration of the  $V_{d1}$  cycle  $t_o$  where the transistor is conductive and more precisely the ratio  $t_o/T$ , where  $T$  is the period of the excitation signal  $V_{g1}$ , need to be optimized in order to achieve a good conversion efficiency i.e. large  $I_{ddoubler}(2f)/I_{dmax}(f)$  value. If  $t_o$  is made too small compared to  $T$  then the magnitude of the resulting  $I_d(2f)$

current is small. On the other hand, very large  $t_o$  values risk to produce  $I_d(2f)$  signals with small harmonic content and are therefore undesirable.

The dc gate voltage is selected close to pinch off so that good class B operation is possible. Furthermore, the large signal swinging of  $I_d$  from zero to its  $I_{dmax}$  value (in response to maximum  $V_{g1}$  excursions), can result under  $V_{g1} \sim V_p$  bias condition in more efficient high harmonic generation. In fact, by exceeding slightly  $V_p$  one can ensure that not only  $I_d$  is set closer to zero but also  $C_{gs}$  reaches its minimum value. The  $V_{g1} \geq V_p$  condition is, however, incompatible with the small gate leakage requirement for reduced risk of device breakdown. InGaAs HEMT's have unfortunately high gate leakage compared to other devices (typically  $100\mu A$  at  $-6.5V$  for a  $1.0\mu m \times 75\mu m$  device) and risk therefore to be sensitive to this bias requirement for multipliers. Except this, gate leakage is not a real fundamental limitation in the circuit performance because its level at the input gate terminal turns out to be small compared to the displacement current in the gate capacitance at high frequency operation.

For increased power levels the conversion loss is seen to reduce and subsequently increase. This is due to the initially larger amplitude of signal  $I_d$  at the output due to the increased input gate voltage  $V_{g1}$  and larger transconductance  $g_m$ . At higher  $V_{g1}$ 's approaching forward operation  $I_d$  reaches a maximum  $I_{dmax}$  and does not therefore, improve any more. Furthermore  $g_m$  starts reducing considerably in HEMT's due to parasitic "MESFET"-type conduction. The conversion loss vs. input power characteristics depend on the selected gate bias and are minimum for  $V_{g1} \sim V_p$ . A different gain power tendency is observed for diode doublers where the conversion loss improves over a larger range of input power levels. Due to the

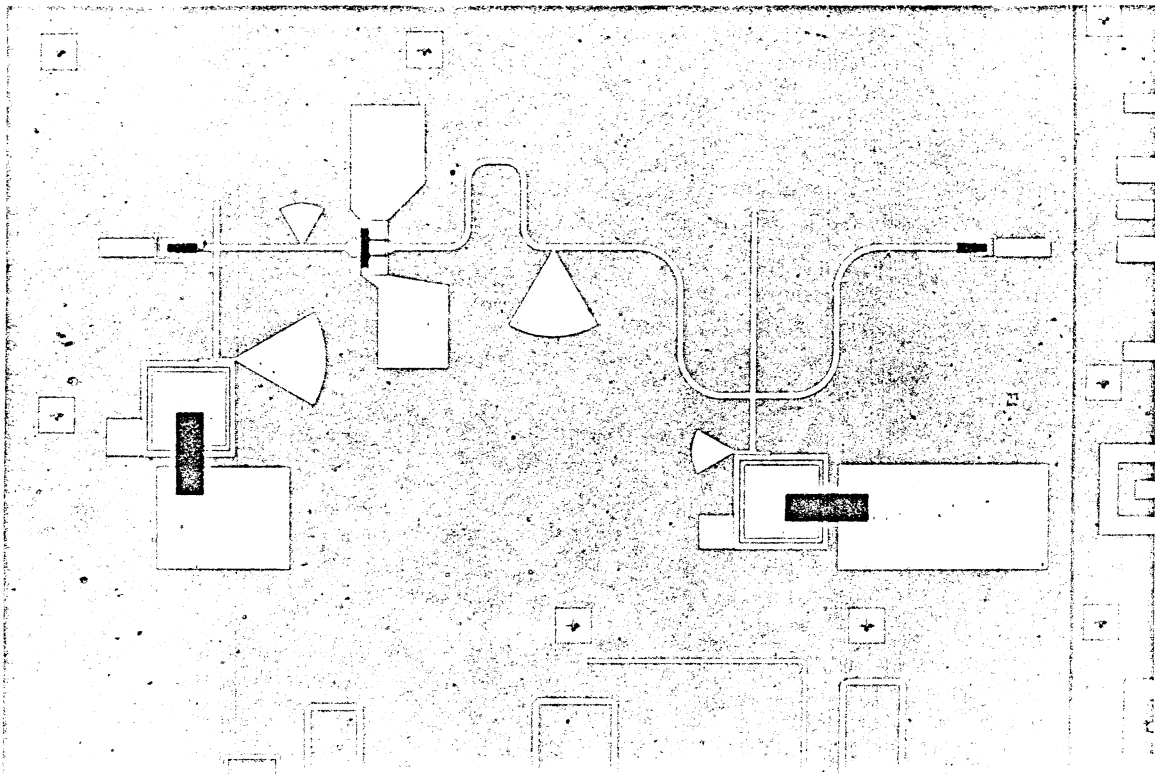


Figure 8 90GHz to 180GHz Monolithic Integrated Doubler chip.

gate-leakage increase with input power this should be selected for the best possible compromise of conversion loss and leakage.

A photograph of the fabricated monolithic doubler chip is shown in Fig. 8. Right next to the HEMT one distinguishes two radial stubs used to realize band-reject filter characteristics. The left stub acts as a 180GHz resonator prohibiting the doubled signal from leaking towards the input, while the right one is a 90GHz resonator cutting off the fundamental 90GHz from the output terminal. Gate bias is achieved through an overlay capacitor connected to 90GHz radial stub which is  $\lambda/4$  transformed to yield perfect open conditions at the input line. A matching network with a  $\lambda/4$  stub (180GHz) is finally incorporated at the output for drain

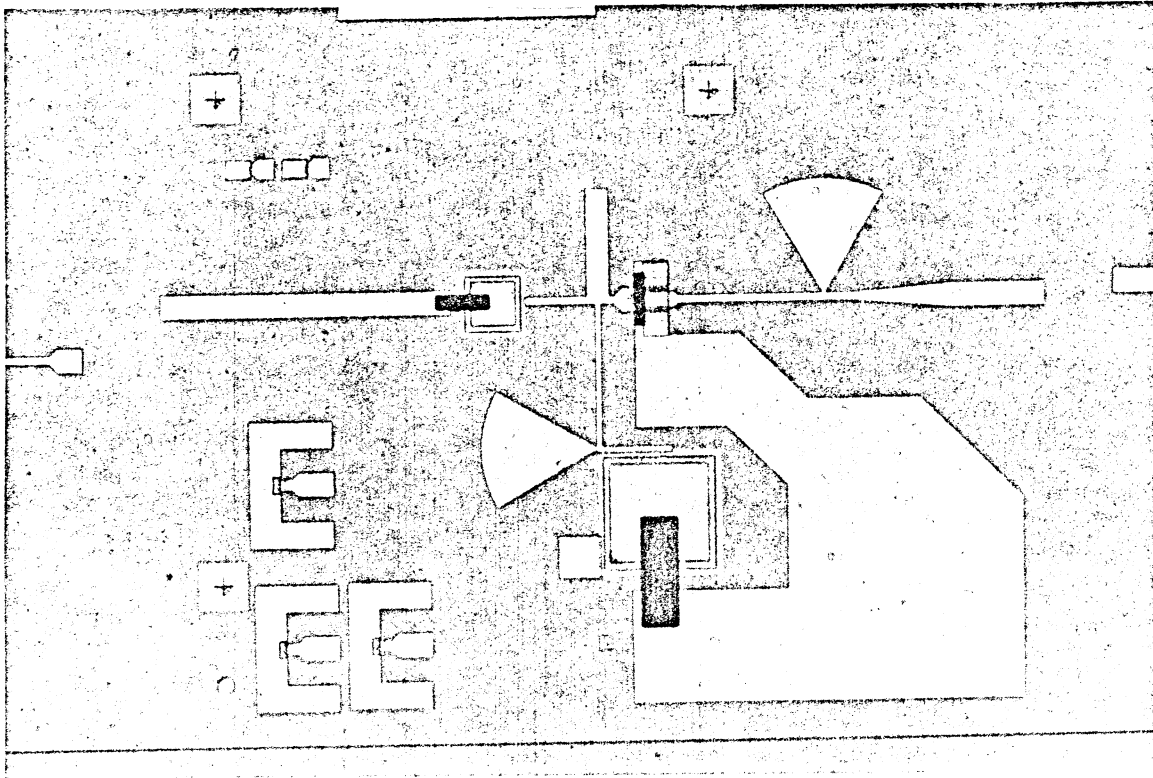


Figure 9 90 GHz Monolithic Integrated Mixer chip.

bias. The monolithic doubler is designed for 13.5dB conversion loss with 1dBm LO power level. The fundamental frequency rejection at the output is of the order of 38dB.

##### 5. 90GHz Monolithic Mixer using InAlAs/InGaAs HEMT Technology.

Monolithic mixers can be built using InAlAs/InGaAs HEMT's instead of diodes. The transistor approach allows lower conversion loss and lower power levels for the LO signal. Unless a balanced design is used, various responses generated by nonlinearities and LO noise cannot be rejected to a satisfactory level. The balanced approach becomes of particular importance in monolithic integrated designs where the oscillator is built without any resonator stabilizing networks. Frequency conversion is achieved by the nonlinearity of the transconductance-input-voltage ( $V_g$ )

characteristics. Best characteristics are obtained when other  $V_g$  dependent parameter, such as for example output conductance shows less nonlinear characteristics. HEMT's are consequently ideally suited for such applications due to the very nonlinear  $g_m$ - $V_g$  characteristics.

A photograph of the fabricated 90GHz monolithic chip is shown in Fig. 9. The RF and LO signals are applied simultaneously at the input. Matching is achieved by the same input network for both LO and RF with best characteristics in the center of the LO-RF band (92.5GHz). A  $\lambda/4$  transformer connects a radial stub to the input line for gate bias. The overlay capacitor enhances the short circuit conditions of the  $\lambda/4$  transformer at its end (90 GHz design). Furthermore, it short-circuits the IF signal by series resonance with the stub and eliminates consequently the IF from the input port. A radial stub design is also used at the output to filter out the RF and LO signals.

In addition to the 3GHz IF, a signal response is also found at  $\sim 6$ GHz. This is eliminated by a low pass filter design employing lumped elements and being integrated onto the same chip. Matching of the complete circuit to  $50\Omega$  load is finally achieved by the same integrated lumped network. The conversion loss of the circuit is 10dB using 91GHz(LO)/94GHz(RF) signals and 5dB of LO power.

### Conclusions

An submicron monolithic integrated technology is reported for receiver/sensor applications in the THz region. The results of the first study are obtained using 0.20-0.25 $\mu\text{m}$  long HEMT's made with InAlAs/InGaAs heterostructures. Maximum oscillation frequencies of 148GHz were obtained and good performance was



demonstrated for devices subjected to all the monolithic integrated process steps. The technology steps used for monolithic fabrication have also been discussed.

Monolithic integrated functions using the submicron HEMT's have been studied and circuits were fabricated. Fundamental signal generation is at first attempted at 90GHz. Signal doubling from 90GHz to 180GHz and mixing at 90GHz is also studied using the submicron HEMT's.

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