High Power Impulse Generation Using Lateral Stacked Nonlinear Transmission Lines

H. Shi*, C. W. Domier**, and N. C. Luhmann, Jr.**

Abstract

Our modeling studies predict that a nonlinear transmission line employing heterojunction stacked barrier devices and a novel lateral stacking configuration can produce impulses with up to 45 V pulse amplitude (equivalent to 20 W for a 50 Ω line) with 8.5 ps FWHM pulse duration. Two 45-section tapered coplanar wave guide lines have been designed and are currently being fabricated for proof-of-principle experiments.

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I. Introduction

In work reported by other researchers, it has been experimentally demonstrated that pulses with picosecond duration and ~ 12 V peak value can be obtained on a nonlinear transmission line (NLTL) utilizing Schottky varactors as the nonlinear element [1]. More recent theoretical studies by our group predict that the use of heterojunction stacked barrier devices [2] such as the Multi-Quantum Barrier Varactor (MQBV) and the Schottky Superlattice Quantum Barrier Varactor (SSQBV) can significantly improve the performance of an NLTL [3], especially the voltage level. However, the increase in leakage current at large signal levels for these GaAs quantum barrier devices (due to the low barrier height) makes it difficult to improve the signal level beyond ≈ 20 V for a total of six barriers [4]. It is possible to further increase the signal level. by using InP based material which has a higher barrier height, or by increasing the number of barrier. But they increase fabrication difficulty as well. On the other hand, the symmetric C-V characteristics of these new devices, naturally fit a back-to-back layout configuration [5], make it possible to lateral, rather than vertical as mentioned above, stacking devices to further improve the signal level. This lateral stacking configuration can double or triple the voltage handing capability of the device. The degree of the multiplication depends upon the final signal pulse width required.

II. Design of lateral stacked NLTLs and simulation results

In applications such as wide band radar, magnetic fusion plasma diagnostics and current sources for diode lasers, picosecond duration pulses with amplitudes of tens, or even hundreds of, volts, are required. The lateral stacking design can double or triple the signal amplitude, depending upon the level of lateral stacking introduced. However, as the stacking number, M, increases, the required device layout area increases by a factor of M^2 which introduces parasitic capacitance, C_p.

Therefore, the effective minimum device capacitance in the line with lateral stacking structure is $C_{min} + C_p$, where C_{min} is the device minimum capacitance without the line effect. Since the device cutoff frequency,

$$f_d = \frac{1}{2\pi C_{min}}\left(1/C_{min} - 1/C_{max}\right),$$

is inversely proportional to $C_{min,eff}$, f_d is degraded by approximately a factor of $(1 + C_p/C_{min})$. For a pulse generating NLTL, the highest Bragg cutoff frequency, f_B, that can be designed is three to five times smaller than f_d. Therefore, the highest value of f_B is reduced by approximately a factor of $(1 + C_p/C_{min})$ as well. Since the final pulse width is inversely proportional to f_B, the narrowest pulse which can be obtained on a line with the lateral stacking structure is increased by approximately a factor of $(1 + C_p/C_{min})$. For M=2 and a line with f_B=120 GHz, following the NLTL design procedures in [6], the required device layout area can be found. Assuming that an interdigitated configuration, as shown in Fig. 1, is utilized in the device layout, C_p is computed. In this case, C_p/C_{min}=0.45 and the final pulse width is increased from 8.4 ps to 11.8 ps. This shows that for an NLTL with a final pulse duration of > 8.5 ps, we can laterally stack up to a factor of two without introducing significant parasitics.

Two 45-section tapered lines utilizing SSQBVs and lateral stacking of two devices have been designed and are currently being fabricated for proof-of-principle experiments. Coplanar waveguide is chosen to suit the test system described in Sec. III. Figure 1 shows the layout of a single section of the lines. The unloaded line impedance is 90 Ω and the loaded line impedance is 50 Ω to match the instrumental impedances. A tapered structure is applied to these lines to obtain smooth pulse compression. From what we have achieved in making the ohmic contact in our previous multiplier array and Schottky diode imagine mixer array fabrications, the device cutoff frequency is assumed to be 1.6 THz, the line Bragg cutoff frequency is increased geometrically nine times, the relative increment is the same in each step, for every five sections from 20 GHz to 125 GHz for Line (1) and to 50 GHz for Line (2). For an input signal of 20 V amplitude and 50 -100 ps pulse duration, the predicted output is a pulse of 45 V amplitude and 8 ps pulse duration and 20 ps pulse duration for Line (1) and Line (2), respectively. Figure 2 shows the equivalent

circuit model used in the simulation. Figures 3 and 4 show the simulation results for Lines (1) and (2), respectively.

III. Test Arrangement

The test system involves the use of as input pulse with a 15-20 V amplitude and 50-100 ps duration. Here, a circuit was built which employs a step-recovery diode as the output device . The circuit can compress a slow input signal into a step-like signal with a fall time of approximately the diode cutoff time (≈50-100 ps) and a amplitude of 50 V. Finally, the output is differentiated into a pulse with a duration of the diode cutoff time and a amplitude ≈ 15-20 V. The rest of the testing system includes Cascade Microtech probe holders with WPH-405 probe heads (65 GHz) and a Tektronix 11802 digital sampling oscilloscope with 50 GHz sampling plug-in. The input and output signals will be brought onto and off the chip by cascade probes.

IV. Acknowledgment

We thank Tom McEwan and Greg Dallun of LLNL for giving us the ideal of the step-recovery diode circuit and many help in building the circuit. This work is supported by Department of Energy under contracts DE-FG03-86-ER53225 and W-7405-ENG-48, and the UCLA Joint Services Electronics Program under contract F49620-C-0055.

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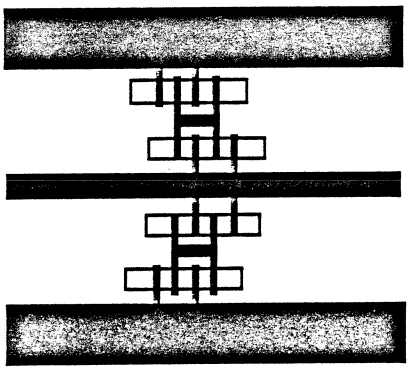

Figure 1. Layout for lateral stacking of two devices. Each solid rectangle includes a pair of back-to-back connected SSQBVs.

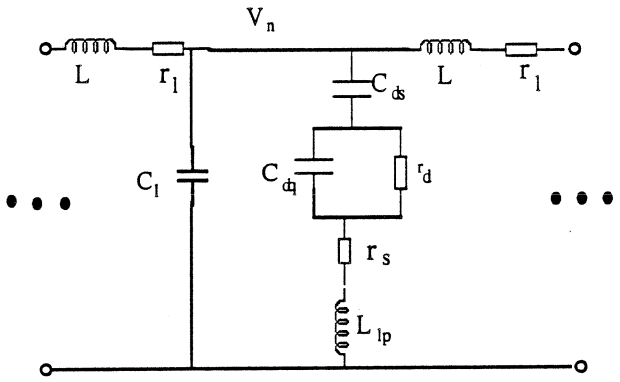

Figure 2. Equivalent circuit model employed in simulations.

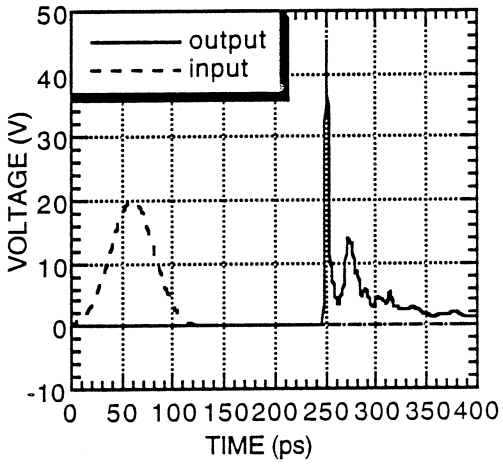

Figure 3. Simulation result for the input and output waveforms on Line (1).

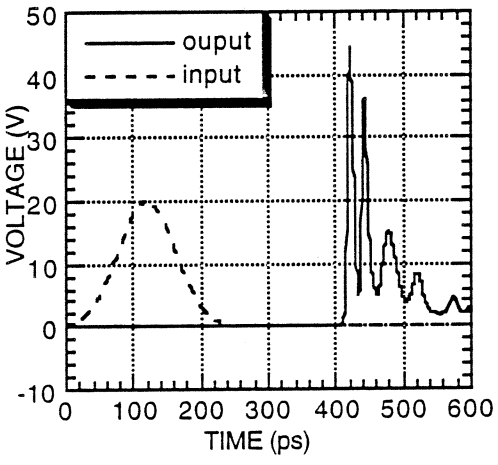

Figure 4. Simulation result for the input and output waveforms on Line (2).