CONCEPT OF A SUPERCONDUCTING INTEGRATED RECEIVER WITH PHASE-LOCK LOOP

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Abstract — A new chip for the sub-millimeter quasioptical heterodyne receiver with an externally phase-locked superconducting local oscillator is designed and being studied. An integrated circuit of the chip contains an ultra-low-noise SIS mixer, FFO, a harmonic SIS mixer and a SIS multiplier (optional). A scheme of the chip is presented along with numerical simulation of the circuitry. The first experimental samples that were pre-tested did show encouraging performance.

INTRODUCTION

Integration of a free-running flux-flow oscillator (FFO) and a SIS mixer into a single-chip Superconducting Integrated Receiver (SIR) is a proven technique. The receiver noise temperature below 100 K (DSB) and a good beam pattern of the double-dipole antenna (sidelobes below –16 dB) have been measured at 500 GHz [1]. To estimate the ultimate performance of the receiver, the detailed tests on a reference

chip which contained only the lens-antenna SIS mixer showed a noise temperature of about 40 K at 470 GHz [2]. A densely packed imaging array seems to be the natural niche for a SIR. The feasibility of such an imaging array was demonstrated as well [1]. Since a SIR is a complicated multi-device chip, a special acquisition system IRTECON has been developed for effective test and optimal control of both the local oscillator and the SIS mixer [1, 3].

To be useful in practice as a narrow-band spectrometer, SIR has to have a narrow linewidth of its internal local oscillator (LO). A technique to stabilize the superconducting integrated oscillators [4] was developed recently into the real PLL circuit using room temperature electronics. An externally phase-locked FFO was realized *in Fiske mode* ($f_{LO} < 440$ GHz) with a measured linewidth as narrow as 1 Hz in the frequency range 230 – 440 GHz for samples of special design [5, 6]. The experimental data on spectra of the locked FFO are presented in Fig. 1. Taking into account that Fiske steps (FS) are almost overlapping at higher voltages, a complete tuneability might be achieved. In summary, it seems possible to use such LO for radio astronomy now already. A PLL circuit for the FFO operation in so-called flux-flow mode ($f_{LO} > 500$ GHz) still has to be developed and studied.

SCHEMATIC OF THE CHIP

To combine a SIS mixer and a *phase-locked* FFO on the same substrate, a new design of the chip has been developed; its scheme is presented in Fig. 2. The chip contains a combination of circuits which principles have been tested already, namely, a PLL circuit to narrow the linewidth of the FFO [5, 6] and a quasioptical SIS mixer with the integrated circuit for LO power injection (see Fig. 3). The harmonic SIS mixer and the SIS multiplier (not shown in Fig. 2) are parts that are added to the chip of the earlier SIR [1, 3].

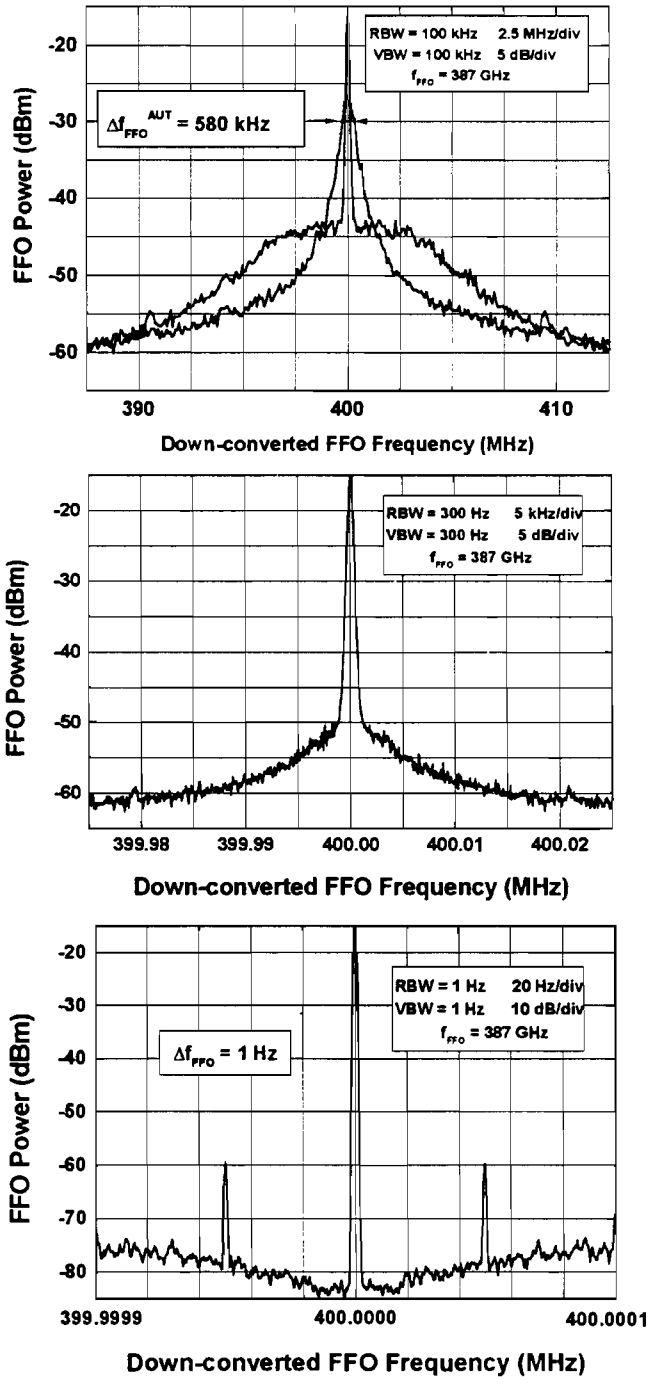

Fig. 1. *IF* power spectra of FFO phase-locked at 387 GHz recorded at different frequency spans.

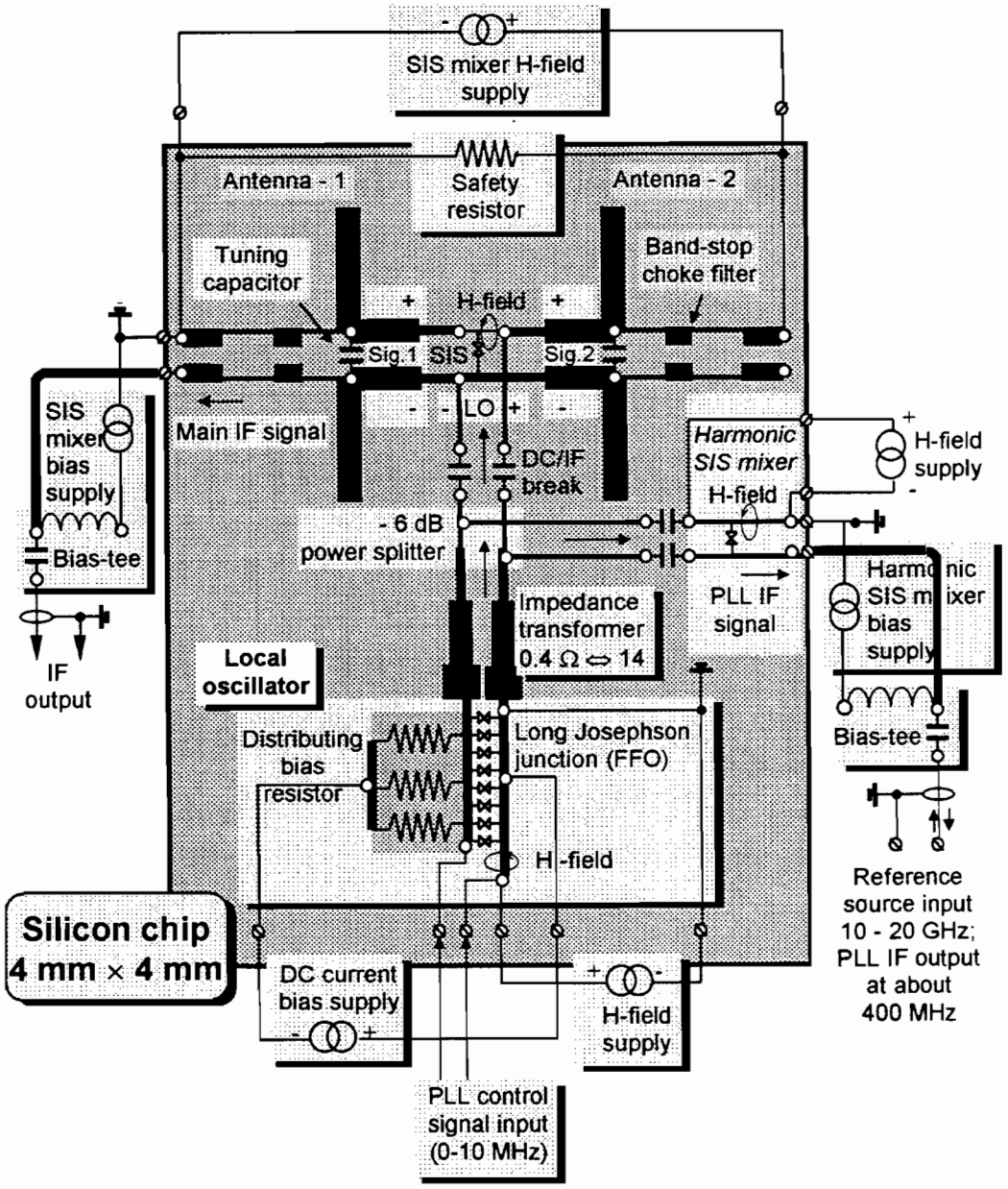

Fig. 2. Simplified equivalent diagram of external supplies and connections necessary to operate the chip of Superconducting PLL Receiver.

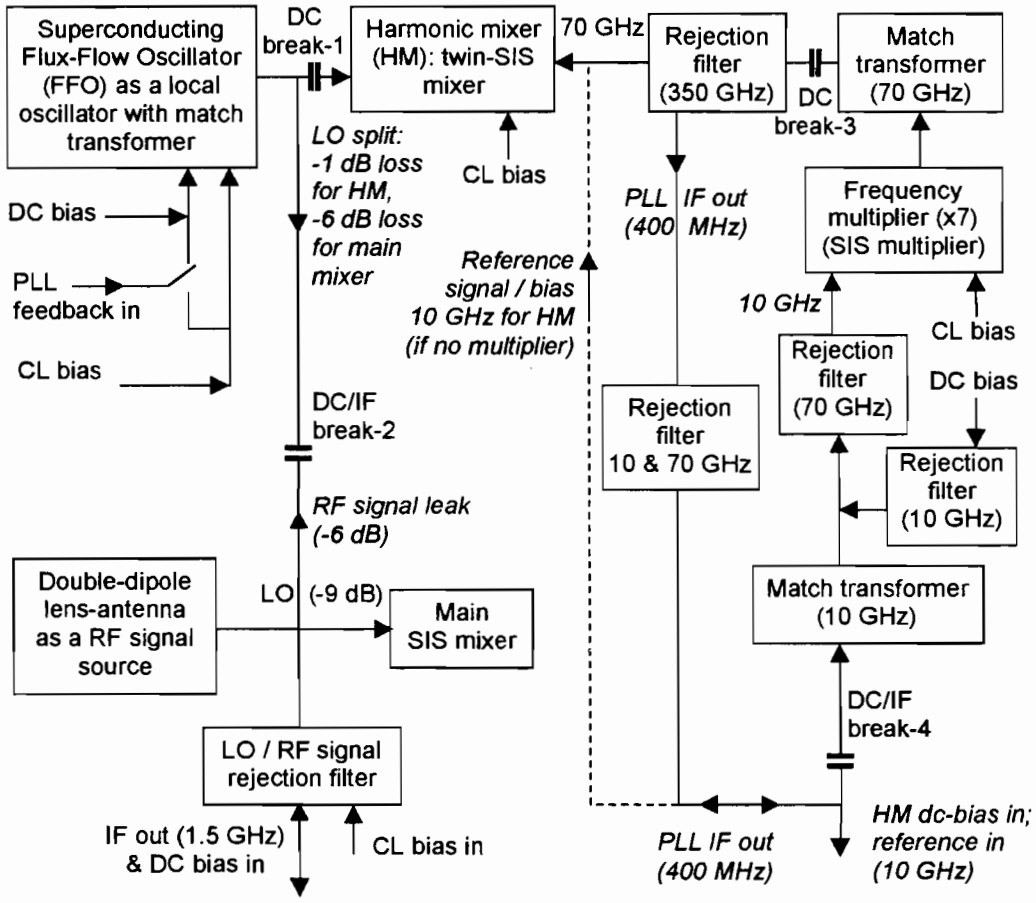

Fig. 3. Simplified block-diagram showing elements located at the chip of Superconducting PLL Receiver (parameters indicated for operation at 350 GHz).

A. Power Balance of Local Oscillator

When one FFO feeds two devices the balance of LO power is very important. The power from the FFO is split unequally between the harmonic mixer and the receiver part. To avoid too much signal loss towards the LO source, only 25-30 % of the power that is available from FFO can be coupled to the receiver SIS mixer. Taking into account that the mixing SIS junction and FFO are coupled effectively to the antenna and the harmonic mixer respectively, the portion of FFO power available at the receiver SIS junction is further reduced to about 12-15 %. This is twice as low in comparison with the previous SIR design [1, 3]. A result of numerical simulation on distributing of the signal and LO power is presented in Fig. 4. To make the level of LO power sufficient for both mixers, either more powerful FFO or smaller receiver SIS junction has to be employed in the PLL receiver.

B. Layout of the Chip

To avoid a reduced yield due to the growing complexity of the chip, special attention was paid not to use micron-sized elements which were present in the earlier SIR design [1, 3]. The narrowest strip width now is about 4 micrometers and the smallest gap is about 3 micrometers. However, the receiver SIS junction has to be small enough, proportional to the available LO power. The area of SIS junctions for both the receiver mixer and the harmonic mixer is chosen to be 1.5 by 1.5 micrometers, so a reasonable reproducibility can be expected.

C. Design of FFO

The power available from FFO seems to be proportional to the width of the long junction. Since characteristic impedance of such a Josephson transmission line (JTL) is reduced with increasing width, the coupling circuit (mainly the impedance transformer) has to provide higher ratio, that may narrow the coupling bandwidth. The increase of the FFO width is restricted because of a transverse mode can be generated

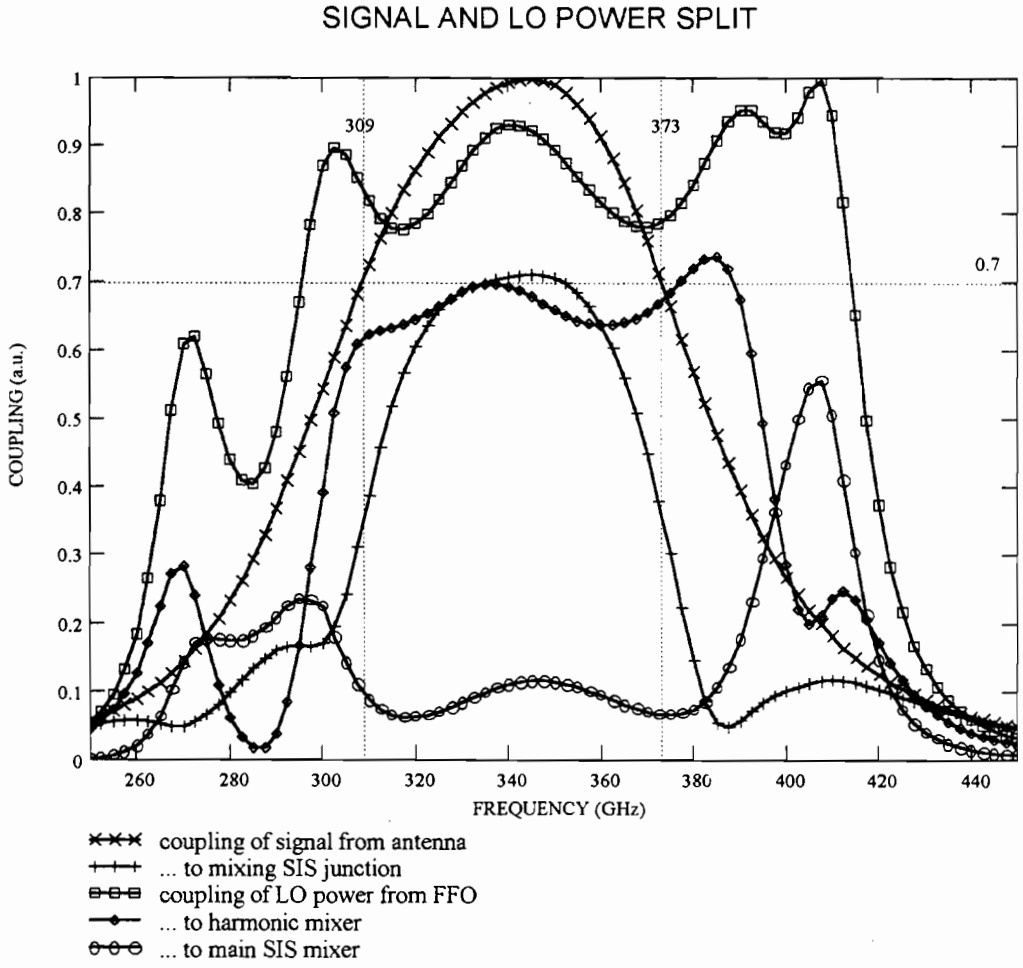

Fig. 4. Example of calculated distribution of signal (x's and +'s) and local oscillator power (box's and dimond's) in the PLL receiver circuitry. Fraction of LO power used by main SIS mixer presented at the bottom by o's. The data calculated for central frequency of 350 GHz.

in the JTL. Three different FFO widths are used in experimental samples: 4, 6 and 9 micrometers. A compact single-section impedance transformer is used.

The PLL receiver will be tested first at about 350 GHz in the Fiske mode. The length of FFO is chosen in the range of 600 ± 50 micrometers that provide voltage separation of FS small enough for continuous coverage of the RF signal band using a 4 GHz IF amplifier and picking different side-bands. The experimental samples for 350 and 560 GHz are fabricated, and preliminary tests are showing reasonable pump level at about 500 GHz.

D. Harmonic Mixer

It was demonstrated that the most efficient regime of the harmonic mixer (tested up to 50^{th} harmonic) can be realized in the Josephson mode using high order Shapiro steps [4 - 6]. However, Josephson mixing is known to be quite noisy [7] and can be the reason for the unwanted noise floor in the experimental PLL loop. Unfortunately, the experimental harmonic mixer operated in a low-noise SIS mode (Josephson effect was suppressed by magnetic field) appeared to be inefficient, at least at high order harmonics. To try mixing at lower harmonics (5th or 8th), a SIS multiplier was integrated on the chip as a source of LO power at 70 GHz. A SIS junction of area 10 by 10 micrometers is used in the multiplier. The part of the chip relevant to the multiplier is shown in Fig. 5.

Use of the multiplier essentially complicates the chip circuitry demanding a few selective filters. Since a reference signal (10 GHz) is applied via IF coaxial cable of the harmonic mixer (see Fig. 2), leak of the reference power has to be suppressed well below the level of its 7^{th} harmonic generated by the SIS multiplier. The multiplier feed circuits (both RF and dc bias) are arranged to provide a good coupling of the reference signal and avoid loss of the harmonic at about 70 GHz. A fragment of the multiplier-related circuit and its numerical simulation are presented in Fig. 5 and Fig. 6 respectively. The calculation demonstrates a reasonable match to the IF port at 400 - 1000 MHz, good rejection of 10 GHz reference signal, reasonably wide

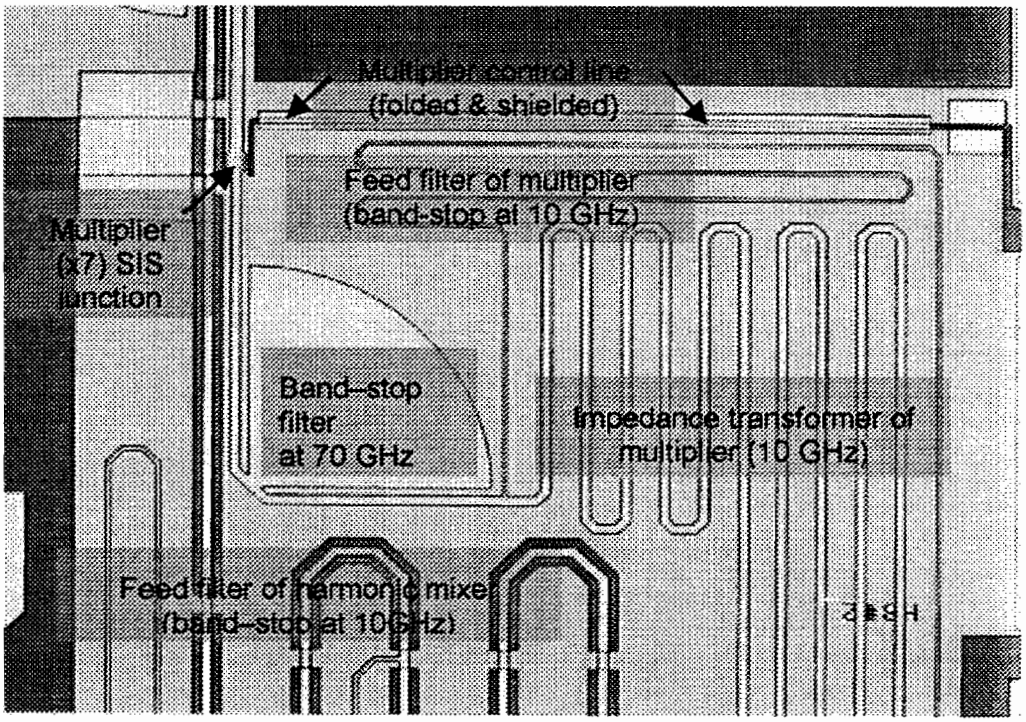

Fig. 5. Partial view of the integrated receiver chip. Folded striplines are feed filters at 10 GHz and 70 GHz used for the SIS multiplier and for the harmonic mixer. Field of view is about 900 x 600 micrometers.

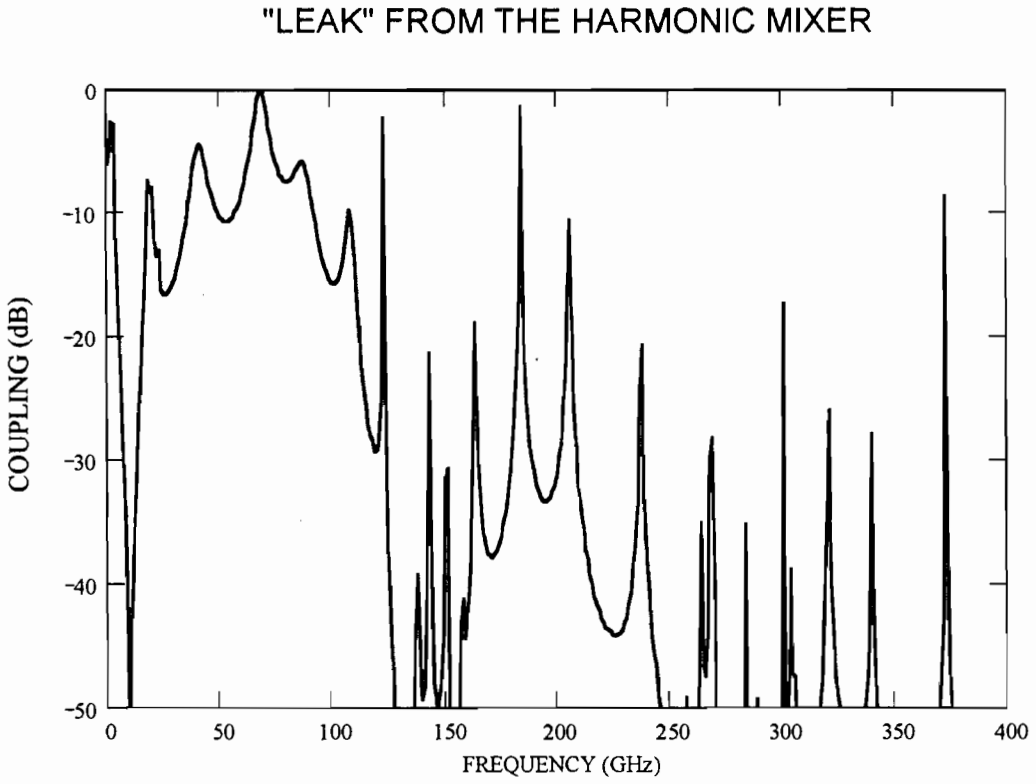

Fig. 6. Reflection loss at the harmonic mixer towards its IF port and towards the SIS multiplier (if used). Coupling to FFO that is, by definition, strong *excluded* from this calculation.

coupling at about 70 GHz and no essential leak within LO/signal range at about 300 – 400 GHz.

CONCLUSION

The concept of a superconducting integrated receiver with phase-lock loop is developed, has passed extensive numerical simulation and is implemented in experimental devices on the basis of recent progress on quasioptical SIS mixers and locked FFO. Preliminary test of experimental samples is, so far, encouraging: sufficient pump level is obtained at about 500 GHz for both mixers. More experimental details are expected soon.

ACKNOWLEDGMENTS

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