# FINITE ELEMENT ANALYSIS OF A PLANAR DIODE DOUBLER

**Jussi Tuovinen and Neal R. Erickson**

Five College Radio Astronomy Observatory
Department of Physics and Astronomy
University of Massachusetts
Amherst, MA 01003

**Abstract**

Finite element analysis of the input circuit of a planar diode multiplier from 85 to 170 GHz is described. In the analysis, the High Frequency Structure Simulator program (HFSS) by Hewlett-Packard was used. To optimize the diode design the de-embedded diode terminal impedance was studied. The analysis revealed that the matching of the diode impedance to the waveguide impedance can be improved by thinning the GaAs substrate, and that 100 $\mu$m of quartz gives better matching than 25 $\mu$m of GaAs. The effect of air bridges in the diode is only marginally beneficial for large capacitance diode junctions, and a slight power imbalance between the diode junction was found.

## 1 Introduction

Solid-state local oscillator sources in the THz range are needed for a wide range of applications including laboratory spectroscopy, spaceborn radio astronomy and observations of the earth's atmosphere. This source can be made using a low frequency fundamental oscillator followed by a chain of frequency multipliers. One possibility to realize a source for 1 THz would be to have a Gunn-oscillator at 83 GHz, followed by a frequency doubler, another doubler and finally a tripler. To obtain 0.1 mW output power at 1 THz it is important that the first doubler have an output power of about 50 mW. This much output power can not be obtained with a single diode, because of the limited power handling, both due to breakdown voltage and saturation effects. Therefore, an array of diodes is needed. Recent tests at the University of Massachusetts have proved the usefulness of an array of planar diodes in series over a single diode in high power multiplication at 174 GHz [2]. The planar structure with four diodes on a single GaAs substrate has been developed at the University of Virginia. Figure 1 shows the multiplier and diode that was used in the tests. The diode was designed without any benefits of modeling. To improve the planar diode design, good modeling of the device is now highly desirable, which must include the interaction of the diode circuit with a waveguide mounting structure. This is particularly important because the manufacturing of a planar diode is a time consuming and expensive process. In this paper we describe the finite element analysis we have carried out on a planar diode doubler from 85 to 170 GHz.

Conventional scaled model measurements, because of the wide range of sizes (> 1000/1), are difficult when one considers the smallest important features on the diode relative to the size of a waveguide mount. Another major problem is how to provide the small coaxial probes to the diode locations. Also, manufacturing of the model includes mechanical inaccuracies, for example, with attaching metal tapes as are often used [1]. We have chosen instead to do numerical electromagnetic simulations on the multiplier. The advantages of the numerical analysis are that they make it easy to study dielectric thickness effects, optimum inductances in the diode package, power balance between the diodes, and the origin of the parasitic effects. Other advantages are the provision for multiple probe ports, and the ease with which the structure can be split into pieces and with which parts of the structure can be added or deleted to see their effects.

# 2 Approach to the analysis

In the analysis, the HP85180A High Frequency Structure Simulator program (HFSS) by Hewlett-Packard was used. This program performs finite element analysis on closed arbitrary geometries with lossy and lossless metals and dielectric materials. The HFSS includes only linear analysis, while a varactor diode is a very nonlinear load. The non-linear analysis to determine optimum source and load impedances was done separately with a harmonic-balance analysis program of the HP85150B Microwave Design System circuit simulator (MDS) by Hewlett-Packard.

Figure 1 shows the doubler from 85 to 170 GHz that was analyzed. In our finite element analysis, the non-linear parts of the doubler were treated in two ways. 1) Small probes were connected to the diode locations in a similar way to that which would be done in scaled model measurements. 2) The non-linear Schottky contact was substituted with a linear lossy capacitor, which had a series resistance and reactance equivalent to the diode impedance at the frequency of the analysis. Figure 2 shows schematically these two cases.

In both cases, the diode impedance was calculated with the harmonic-balance analysis, by finding the optimum input and output embedding impedances under optimum bias conditions. In the electromagnetic analysis the equivalent input and output circuits of the multiplier were used. Figure 3 shows the equivalent input circuit of the multiplier shown in Figure 1. Due to the symmetry, only half of the circuit is needed. To reduce computational requirements in the finite element analysis, it is important to take full advantage of electric and magnetic field symmetries. However, this should be done with care since physical symmetry of the structure does not necessarily imply electrical symmetry. The input waveguide $TE_{10}$-mode does not couple to the TEM-mode in the coaxial line between input and output waveguides. Therefore, the input circuit ends at the fixed curved backshort of the input waveguide. Comparison of the results showed that the backshort can be included either in the finite element analysis or later in the circuit analysis. Because the latter alternative was chosen, the equivalent input waveguide circuit is just a simple piece of waveguide with a port in each end. This approach is more flexible from the de-embedding point of view. The equivalent input circuit, as well as Figure 1, does not include a waveguide step, which is part of the $\lambda/4$ impedance transformer in the actual doubler.

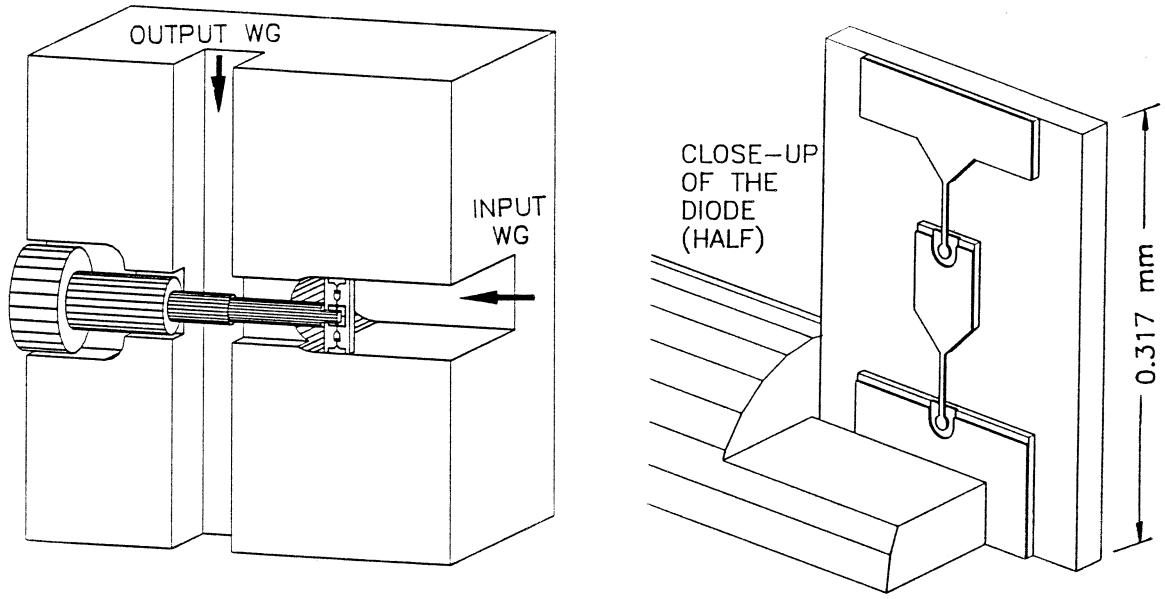
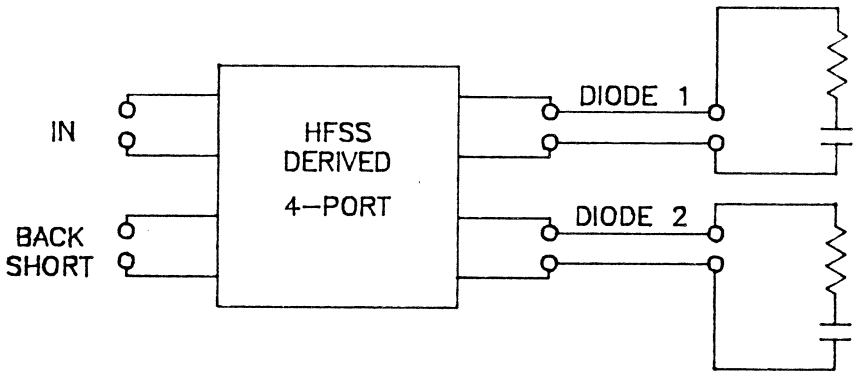
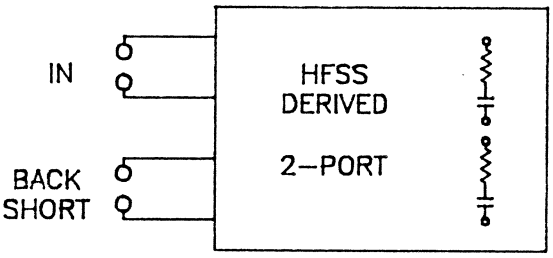



Figure 1: *The planar diode frequency doubler from 85 to 170 GHz used in the tests and in the finite element analysis.*




(a)




(b)

Figure 2: *Theoretical analysis circuit with (a) small probes to the diode locations and (b) lossy capacitor approach.*

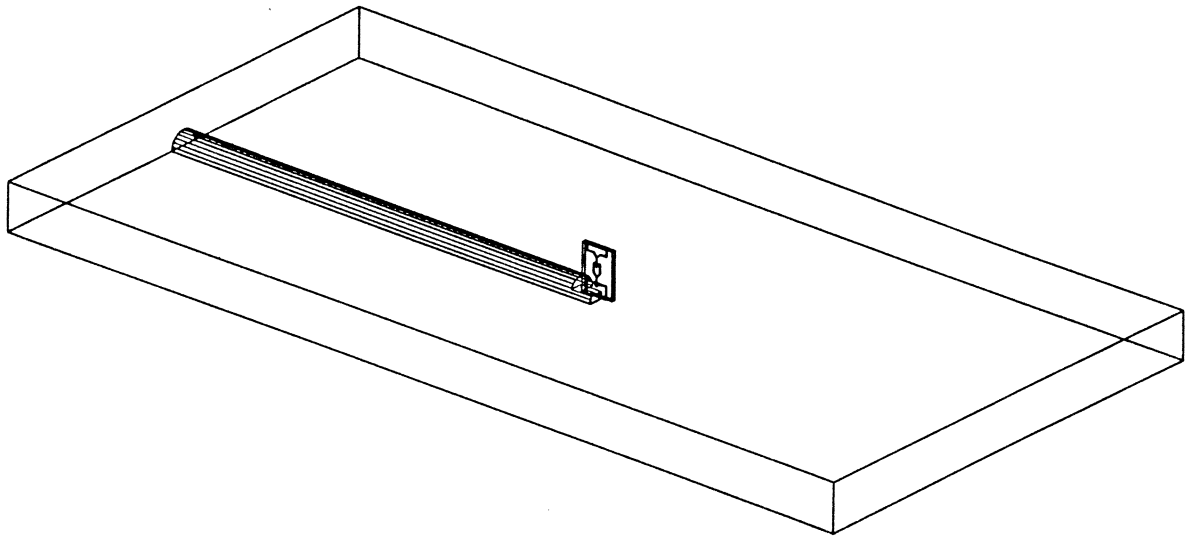


Figure 3: *Equivalent input circuit.*

*Probe ports to the diode locations*

Figure 4 shows schematically the theoretical analyzing process in the case when small probe ports are used to the diode locations and Figure 5 shows the cross-section of a diode location with a small probe. The output of the finite element analysis is a generalized 4-port $S$-matrix. There is one port to each diode location and one port in each end of the input waveguide with the $S$-parameters of each port normalized to the impedance of the cross section at the port. The 4-port $S$-matrix is combined into an embedding circuit in a circuit simulator, where diode impedances from the harmonic-balanced analysis are connected to the diode ports. To enable de-embedding and variation of the backshort position in the circuit simulator, circuits corresponding to the waveguide are connected to the waveguide ports. The waveguide circuit with the center bias pin is terminated with a backshort. The input impedance of the structure can now be calculated at the end of the other waveguide circuit.

De-embedding process, to obtain the diode terminal impedance, includes addition of waveguides with negative length and correct dispersion and impedance characteristics to the ports. Furthermore, the backshort is substituted with an open circuit. Balance between the absorbed power of the diodes can also be easily calculated from the currents and voltages in the diode ports of the $S$-matrix.

*Diodes modeled as lossy capacitor*

Instead of leading small probes to the diode locations in the finite element analysis, the correct load impedance may be placed at the diode location with a series $RC$ circuit. In the finite element analysis, the $RC$ circuit is easiest to realize by using a capacitor with lossy dielectric. Figure 6 shows the overall analyzing process in this case. The cross-section of the diode location, where a lossy capacitor has been placed is shown in Figure 7. The

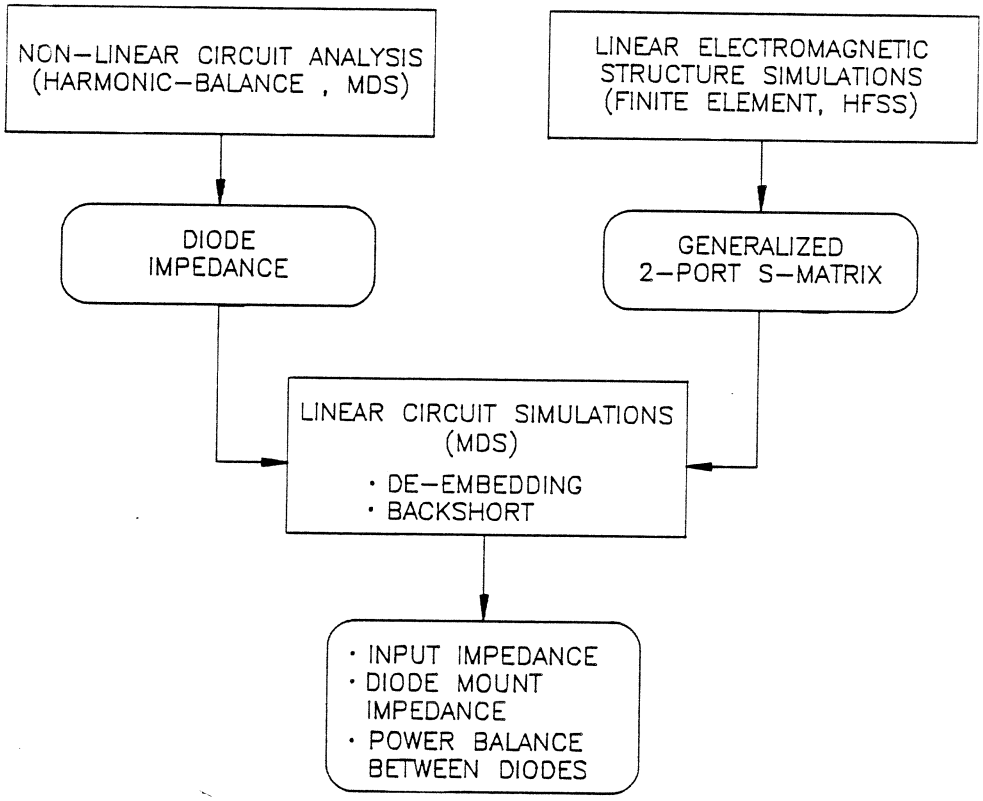



Figure 4: *Theoretical analyzing process with small probes to the diode locations.*

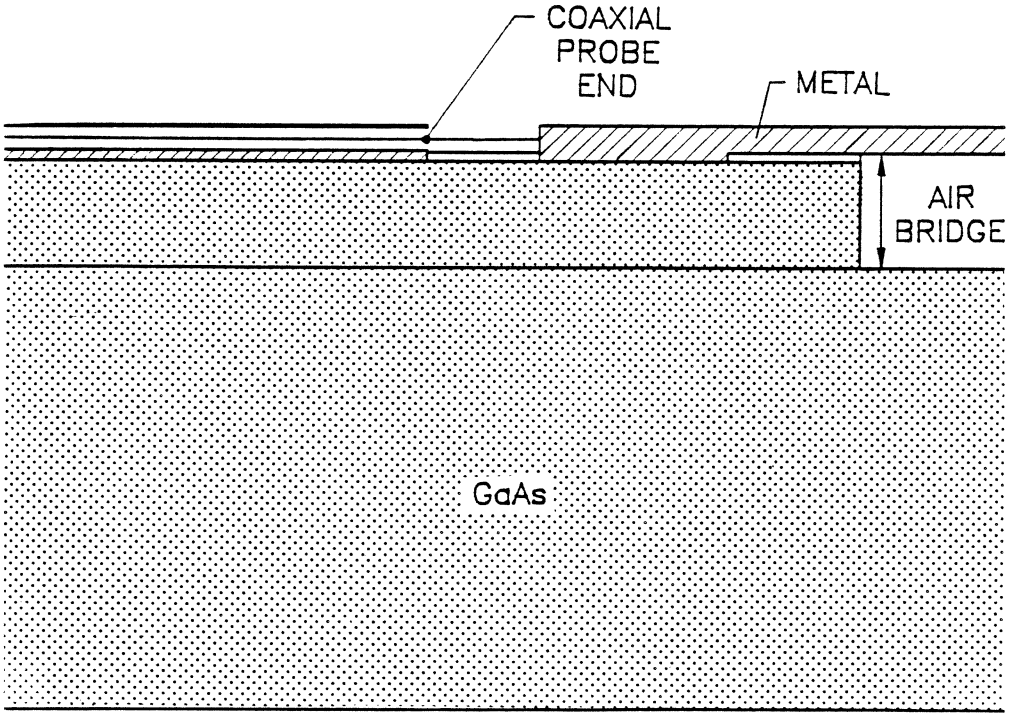



Figure 5: *Cross-sectional view of the diode junction area with a small coaxial probe.*

capacitor thickness is 2 $\mu$m, which is about two times the thickness of the $n$-type epilayer of a real Schottky contact. The heavily doped $n^+$-substrate, under the epilayer, is modeled as a perfectly conducting metal. The equivalent circuit for a lossy capacitor is shown in Figure 8. Losses in the dielectric can be expressed through a complex dielectric constant

$$\hat{\epsilon}\epsilon_0 = (\epsilon' - j\epsilon'')\epsilon_0 \tag{1}$$

where $\epsilon' = \epsilon_r$ is the real part of relative dielectric constant, $\epsilon''$ is the imaginary part and corresponds to the losses in the material, and $\epsilon_0$ is the dielectric constant of a vacuum. The equivalent series capacitance $C_s$ is

$$C_s = C_0 \frac{\epsilon'^2 + \epsilon''^2}{\epsilon'}, \tag{2}$$

and the equivalent series resistance $r_s$ is

$$r_s = \frac{\epsilon''}{\omega C_0(\epsilon'^2 + \epsilon''^2)}, \tag{3}$$

where $C_0 = \epsilon_0 A/d$ for a plate capacitor, $A$ is area of the plates and $d$ is the separation between the plates, $\omega$ is the angular frequency.

The advantage of using lossy capacitors over the small probes is that physically the model corresponds better to a real diode. Due to this, for example, fringing fields around the diode pad can be calculated more accurately. Also, the number of finite elements in the analysis is smaller with a lossy capacitor. This can be a significant advantage, because the complexity of the analysis is limited by the computer memory resources.

The disadvantage of the lossy capacitor approach is that the analysis relies on the assumption that the frequency dependence of the lossy capacitor impedance is the same as that of the diode, which is true only over a limited bandwidth. Another disadvantage is that the calculation of the division of the absorbed power by each diode junction is not as easy as with the diode probe ports. With lossy capacitors the power division can be obtained by calculating the pointing vector over a closed surface covering the lossy dielectric.

# 3 Numerical considerations

Even with the relatively large capabilities of present workstation computers, finite element analysis are often limited by the memory and processing speed of the computers. The discussion given here on the numerical limitations and requirements, and on how the analysis is done is based only on the experience with the HFSS finite element program. However, it may be assumed that the discussion serves as a general guide line to this type of analysis.

In the finite element analysis, the 2-D and 3-D structures are divided into triangular and tetrahedral sections, respectively. Figure 9 shows an example of the mesh associated with the volume in front of the diode. The structure must be closed with a metal surface. Inputs and outputs to the structure are obtained through ports on the outside surface. In each port the desired number of propagating modes are calculated, based on the cross-section of the port. Usually, the port is designed so that only the lowest order mode is supported at the frequency of the analysis. The waveguide attached to each port should extend far enough from the structure with the same cross-section so that all the evanescent modes have

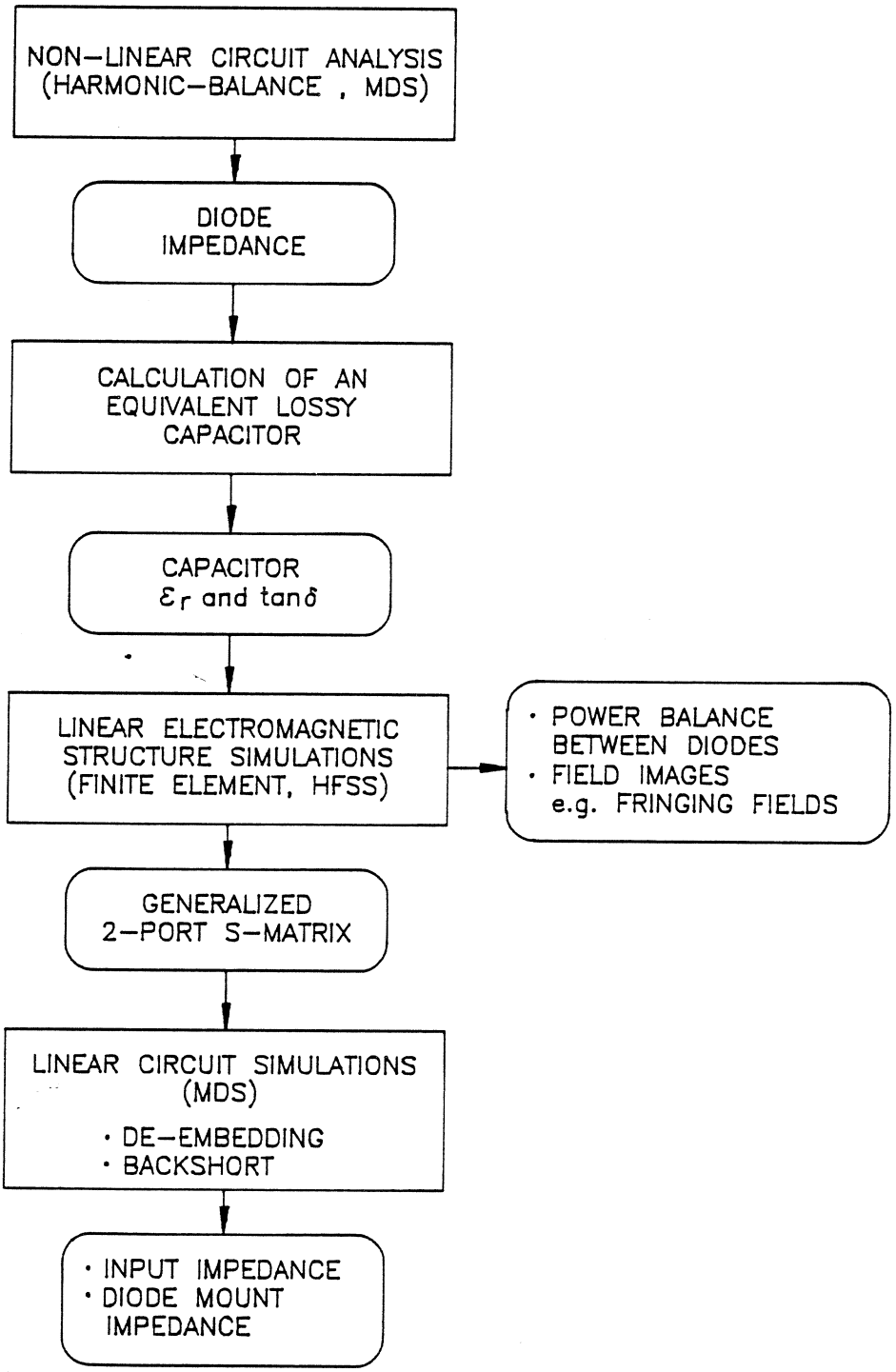



Figure 6: *Theoretical analyzing process with lossy capacitors.*

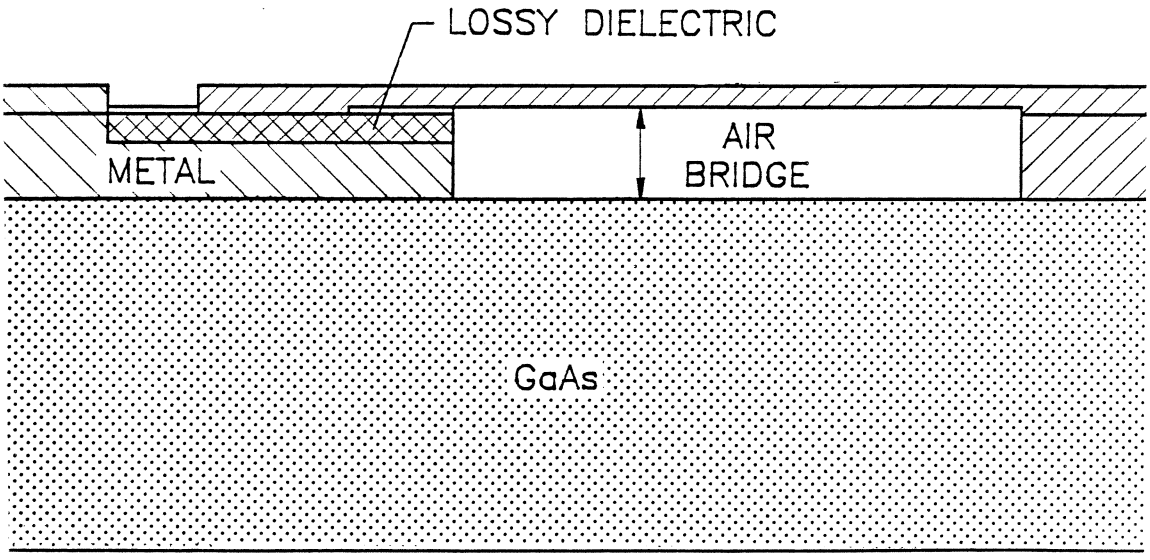



Figure 7: *Cross-sectional view of the diode junction area modeled as a lossy capacitor.*

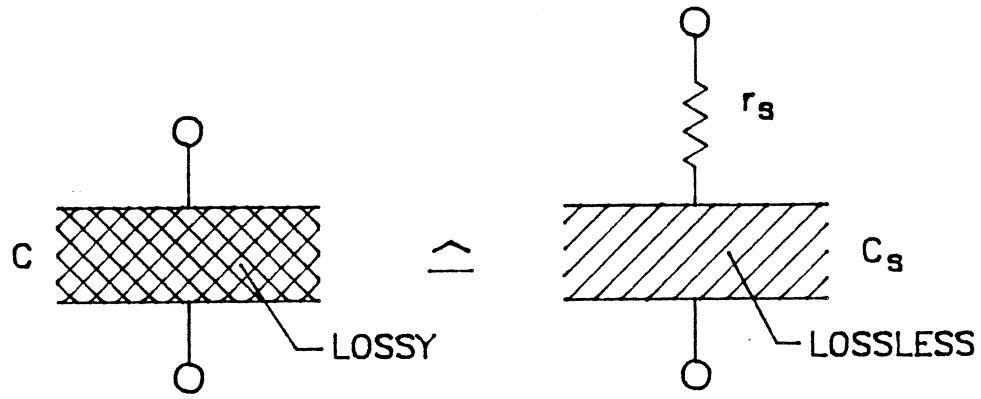



Figure 8: *Equivalent circuit of a lossy capacitor.*

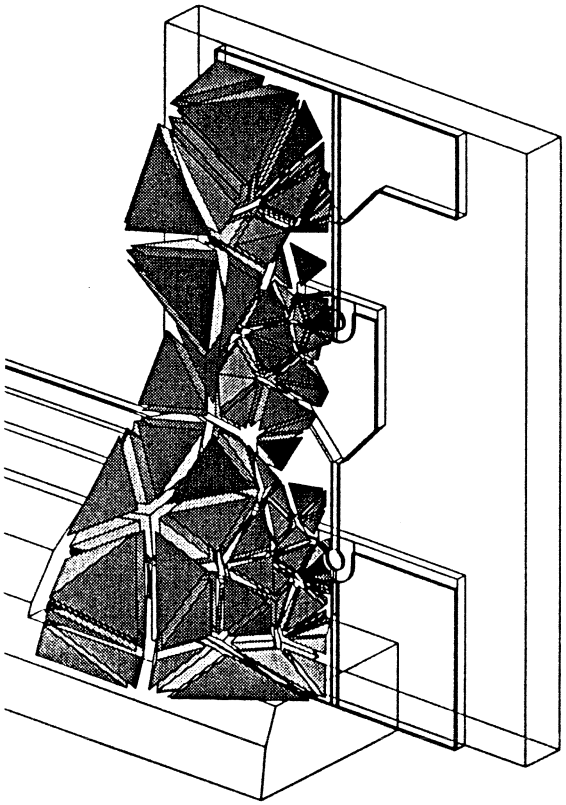


Figure 9: *Shaded view of a part of the finite element mesh in front of the diode.*

been attenuated at least 30–40 dB. This typically means that the length of the waveguide should be at least 1–3 times its width. After the mode(s) in the ports are calculated and the mesh generated, the full electromagnetic field pattern inside the structure, resulting from an excitation wave from one port is computed. This field solution is based on solving the wave equation inside the structure. The $S$-parameters are obtained by calculating coupling of the field inside the structure to the propagating mode(s) of each port.

From the point of view of numerical computations, the size of the mesh, i.e., the number of tetrahedra, is the most significant limiting factor. To save computer resources, the mesh is adaptively refined until the desired accuracy (convergence) for the $S$-parameters is obtained. In the process the mesh points are added iteratively so that the size of the tetrahedron is small compared to the length along which the field changes. Usually, 5-7 adaptive passes were used to obtain $\Delta S = 0.01$ (change of $S$-parameters compared to the previous adaptive pass).

The computer used in the analysis, was Sun Sparc II, with 64 MB of RAM, 219 MB of SWAP space, and a 1.5 GB harddisk. With this configuration the maximum mesh size was 34000 tetrahedra and 9 adaptive passes could be carried out for the input circuit shown in Figure 3. The memory requirement during the analysis when the matrix was solved was over 200 MB (of the RAM/SWAP memory area). In addition to these, over 350 MB of temporary file space was needed on the harddisk.

Analysis of the input circuit, was carried out from 75–95 GHz, and the mesh was generated in the middle of the band at 85 GHz. Practically no difference was observed in the results as mesh was generated at 75 or 95 GHz. In a circuit with strong resonances the mesh generated at one frequency might not be useful at another frequency. Convergence

and repeatability of the analysis were good: starting from different initial mesh gave the same results.

# 4 Results of the analysis

*Effect of the thickness of the GaAs substrate*

Experimental tests showed [2] a mismatch between the diode and waveguide mount impedances. This was due to the real part of the diode impedance being lower than that of the mount. Furthermore, the tests showed that better matching was obtained by using a thinner GaAs substrate. The original and thinner substrate were about 100 and 25 $\mu$m thick, respectively. For the comparison, finite element analyses were carried out for these two cases as well as for the imaginary extreme case of no substrate at all.

The results for the de-embedded diode terminal impedances are shown in Figure 10. This figure shows that a higher real part of the impedance is obtained as the substrate is made thinner. Therefore, better matching can be obtained with a thinner substrate. The slope of the curve of the imaginary part of the impedance indicates the resonance between the diode capacitance and the inductance of the embedding circuit of the diode junction. We see that the extra capacitance due to the thicker substrate lowers the resonance frequency of the chip, but also increases the $Q$ of this resonance. For best bandwidth, the imaginary part of the impedance should go to zero near the midband of operation while the $Q$ should be as low as possible. Therefore, the thinner substrate would ideally require more inductance in the package. This argument does not consider the matching at the second harmonic, which may require a lower inductance for the best results.

*Quartz vs. GaAs substrate*

Another possibility to improve diode matching to the waveguide impedance is to use substrate with a lower dielectric constant than that of GaAs ($\epsilon_r$=13.0). Quartz ($\epsilon_r$=3.8) is one such a material. Quartz is, however, more difficult than GaAs to make thin. The thinnest GaAs substrate that is reasonable to fabricate and to handle is about 25 $\mu$m. The question is what thickness quartz substrate would be better than this thinnest GaAs substrate. To find this out, the analysis was carried out for a quartz thickness of 100 $\mu$m (which would be also a very reasonable thickness to realize in practice). Figure 11 shows the de-embedded diode terminal impedance for 25 $\mu$m GaAs and 100 $\mu$m quartz substrates.

Comparison of the impedances shows that a 100 $\mu$m quartz substrate gives a slightly higher real part of the impedance. Therefore, if the quartz is used it should be made thinner than about 100 $\mu$m. The smaller thermal conductivity of the quartz over GaAs is one limitation for the use of a quartz substrate.

*No air bridge*

Planar diodes are generally designed with an air bridge as a lead to the Schottky contact pads. The air bridge provides a break in the $n^+$ substrate to avoid a dc short circuit across the diode, a need which would otherwise require a proton isolation of the region. An additional

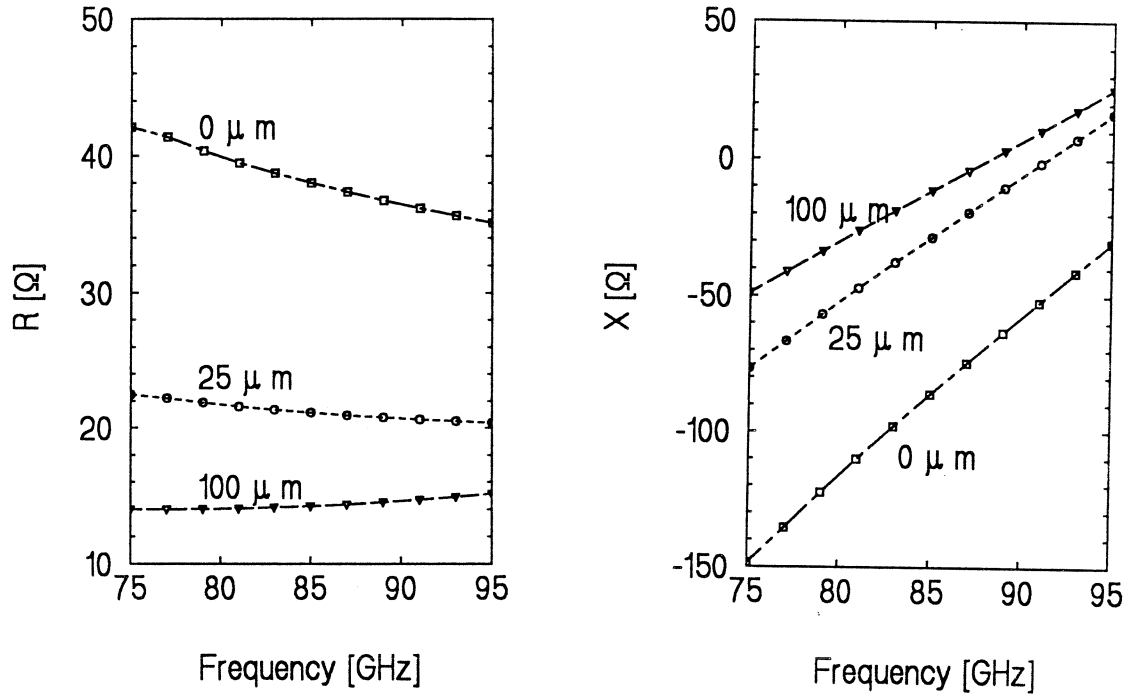



Figure 10: *Real and imaginary part of the de-embedded diode terminal impedances with 0, 25 and 100 μm GaAs substrate thicknesses.*

advantage is that air bridges reduce the shunt capacitance over the planar diode junction. However, most of the shunt capacitance is due to the fringing field between the relatively large contact pads through the high dielectric constant GaAs [3]. To study the electrical advantage of the air bridge geometry, analysis was carried out with the space under the air bridge filled with GaAs.

Figure 12 compares the de-embedded diode terminal impedances with and without the air bridge. The substrate is a 25 $\mu$m thick GaAs in both cases. The comparison shows that electrically the air bridge is only marginally effective with high capacitance varactors ($C_{j0} \approx 40$ fF). For lower capacitance planar diodes, used for example in mixers, the effect of the air bridge can be more significant. Avoiding the use of an air bridge would improve the handling and mechanical strength of the diode. Also the length of the inductive finger would not be limited, for example, when contact pads are brought further apart to reduce fringing capacitances.

*Power balance between the diodes*

To enable efficient use and biasing of all four diodes on the same chip, the absorbed power should be equal for each of them. For all the structures that were analyzed, the power balance between the diodes (inner diode, which is closer to the bias pin, and outer diode, which is closer to the waveguide wall) was practically frequency independent. However, depending on the structure, the power imbalance varied from 2.7 to 12.2 %. Table 1 summerises the

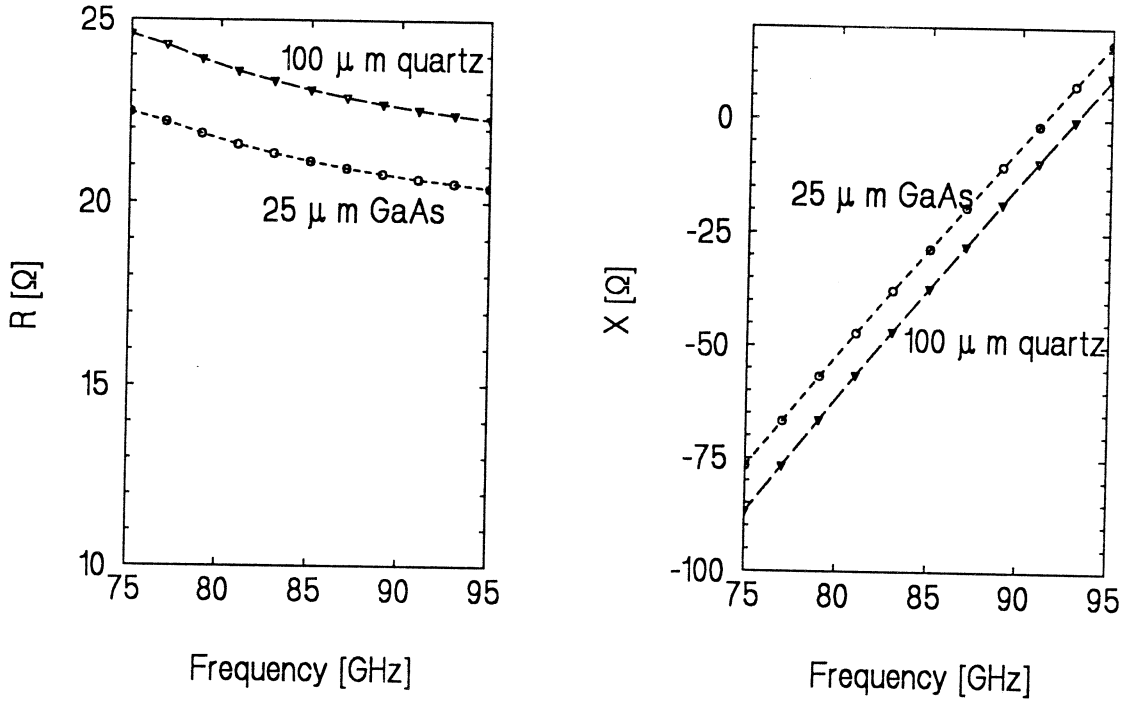



Figure 11: *Real and imaginary part of the de-embedded diode terminal impedances with 25 μm GaAs and 100 μm quartz substrates.*

power imbalance observed in different cases. The power imbalance is defined here as

$$\Delta P = \frac{P_{\text{outer}} - P_{\text{inner}}}{P_{\text{inner}}}. \tag{4}$$

A positive percentage value means, therefore, that the outer diodes are absorbing more power than the inner diodes.

The values in Table 1 imply that the environment of the diodes are not symmetric and to optimize the diode operation the symmetry should be improved. The primary contribution to the imbalance is the different sizes of the metallization areas around the diodes. A larger metallization area around the diode junction increases the shunt capacitance and therefore decreases the absorbed power. The addition to the shunt capacitance of the inner diodes due to the bias pin is less than afew percent, even though size of the pin is large compared to the center contact pad. This can be understood by realizing that the fringing fields are concentrated in the high dielectric substrate material.

# 5 Conclusions

Finite element analysis was shown to be useful in analyzing a planar diode multiplier structure from 85 to 170 GHz.

The diode that was fabricated and analyzed here is a good first step. To optimize the diode design, the de-embedded diode terminal impedance in the input circuit was studied.

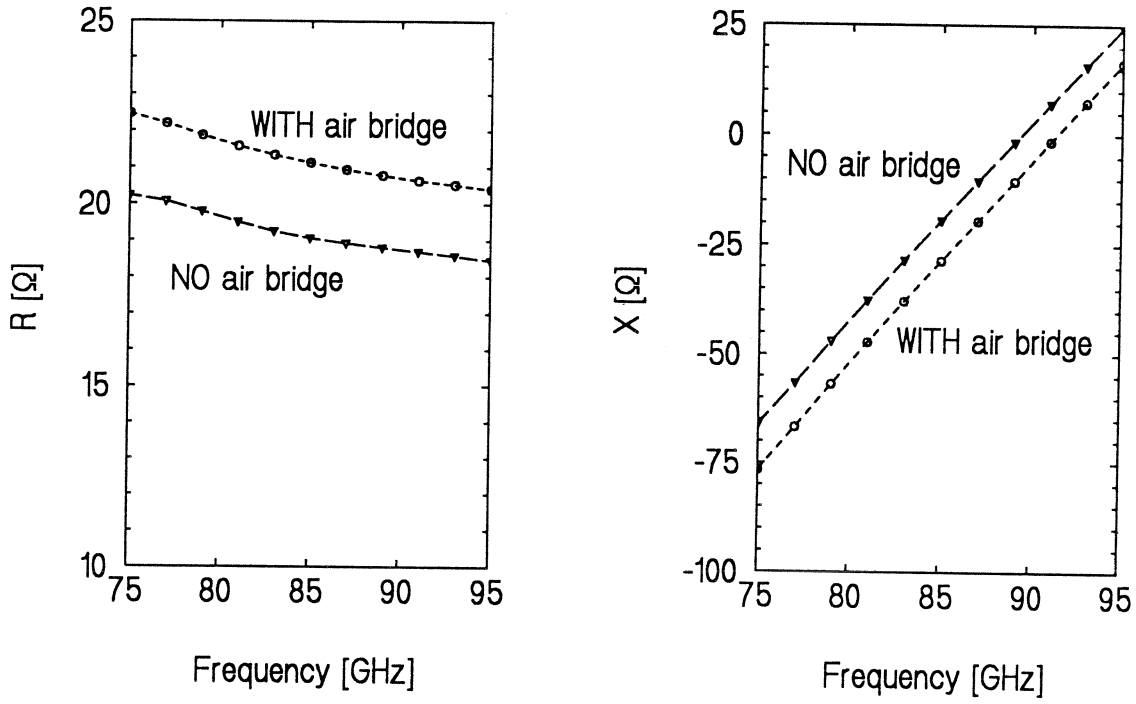



Figure 12: *Real and imaginary part of the input and diode mount impedances with and with out air bridge (25$\mu$m GaAs substrate).*

Table 1: *Absorbed power imbalance between the inner and outer diode junctions. A positive percentage means that the outer diode junctions are absorbing more power than the inner diode junctions.*

| Substrate | Power imbalance $\Delta P$ |
|---|---|
| GaAs 0 $\mu$m | 2.7 % |
| GaAs 25 $\mu$m | 8.9 % |
| GaAs 100 $\mu$m | 9.2 % |
| GaAs 25 $\mu$m (no air bridge) | 12.2 % |
| GaAs 25 $\mu$m (no bias pin) | 7.4 % |
| Quartz 100 $\mu$m | 3.1 % |

The analysis showed that thinner substrate thickness gives a better matching for the diode impedance to the waveguide impedance. If quartz substrate is used instead of GaAs, to improve the matching, it has to be thinner than 100 $\mu$m. This is based on the assumption that GaAs substrate can not be made thinner than 25 $\mu$m.

The analysis revealed that from the electrical point of view air bridges in the diode were only marginally effective for high capacitance varactors.

A slight absorbed power imbalance was also found between the diodes. To improve the power balance, the symmetry of the environment of the diodes has to be improved by changing the diode metal pad sizes.

# Acknowledgment

We acknowledge the financial support of the European Space Agency through a ESA Fellowship for one of the authors and the National Aeronautics and Space Administration under grant NAGW2430.

# References

[1] R. F. Bradley, "The application of planar monolithic technology to Schottky varactor millimeter wave frequency multipliers ," Ph.D. dissertation, University of Virginia, May 1992.

[2] N. R. Erickson, B. J. Rizzi, T. W. Crowe, "A 174 GHz high power doubler using a planar diode array," This proceedings.

[3] B. J. Rizzi, J. L. Hesler, H. Dossal, T. W. Crowe, "Varactor diode for millimeter and submillimeter wavelengths," *Proc. Third Int. Symp. Space Teraherz Tech.*, Ann Arbor, pp. 73–92, March 1992.