

Outline of an upcoming book titled:

Dynamic Random-Access Memory Circuits by Pinaki Mazumder

(with the assistance of S.R. Li) to be published

This book discusses circuit design techniques for various types of DRAM chips, namely, graphics DRAM, synchronous DRAM, Rambus DRAM, and video DRAM. The book gives the actual circuit implementation of a multi-megabit DRAM chip with parallel test capability. The line-mode parallel testing of DRAM arrays was invented by Pinaki Mazumder in 1987 and it is adapted for JEDEC parallel test standards. Full explanation along with some simulation results will be provided for the following circuits in the upcoming DRAM book.

I. Row Address Circuits

1. Row Clock Logic Circuit.
2. RAS Before CAS Circuit, and RAS Before CAS Reset Circuit.
3. Row Address Driver Circuit.
4. Row Decoder Driver Circuit.
5. Row Decoder Circuit.
6. Row Redundancy Address Circuit.
7. Row Redundancy Decoder Circuit.
8. Row Redundancy Quadrant Select Circuit.
9. Write Before RAS Circuit.
10. Read Before Write Pulse Circuit.
11. Write Before RAS Pulse Circuit.

II. Sense Amplifier and Column Address Circuits

12. Master Sense Clock Circuit.
13. Sense Clock Circuit
14. Sense Amplifier Circuit.
15. Column Address Buffer Circuit.
16. Y Decoder Circuit.
17. Column Redundancy Coder Enable Circuit.
18. Column Redundancy Row Address Circuit.
19. Column Redundancy Address Circuit.
20. Column Redundancy Decoder Circuit.
21. Column Redundancy I/O Select Circuit.
22. Column Address Transition Detector Circuit.
23. Quadrant Select Circuit.
24. Global Amplifier Select Circuit.

III. Input/Output Circuits

25. Data Write Enable Signal Circuit.
26. Write Clock Circuit.
27. Read Write Logic Enable Circuit.

28. Local I/O Amplifier Circuit.
29. Global I/O Amplifier Circuit.
30. I/O Multiplexor Circuit.
31. Output Buffer Circuit.
32. Input Buffer Circuit.
33. I/O Control Logic Circuit.
34. ESD Circuit.

IV. Pump and Oscillator Circuits

6. Low Power Oscillator Circuit.
7. VBB Low Power Pump Circuit.
8. High Power Oscillator Circuit.
9. VBB High Power Pump Circuit.
10. Power up Boost Oscillator Circuit.
11. VBB Booster Pump Circuit.
12. VBB Detector Circuit.
13. Level Detector Circuit.
14. Power Up Detector Circuit.

V. Power Supply Circuits

15. Voltage Burn In Circuit.
16. Voltage Clamp Circuit.
17. Voltage Level Multiplier.
18. Voltage Array Buffer Circuit.
19. Voltage Periphery Buffer Circuit.
20. Voltage Array Driver Circuit.
21. Voltage Periphery Driver Circuit.
22. Voltage Regulator, Level Detector Circuit Zero Level Detector Circuit.
23. Voltage Bit Line Reference Circuit.
24. Voltage Top Plate Generator.
25. VDD Reference Circuit.
26. Top Plate Hold-off Circuit.
27. Voltage Bandgap Reference Generator Circuit.

VI. Design-for-Testability Circuits

28. DFT Over Voltage Circuit.
29. DFT initialized Circuit.
30. DFT JEDEC Mode Circuit.
31. DFT Row Address Latch Circuit.
32. DFT Mode Circuit. .
33. DFT Parallel Test Circuit.
34. DFT Word Line Comparator Circuit.
35. Test Mode Data Enable Circuit.

The following patents were ANALYZED, SIMULATED, and COMPARED with related patents for Word-line booster circuit and high power, low power and booster pump circuits with built-in pump oscillators as described previously in the book.

Word Line Booster Circuits:

Patent Number: 5,751,643
Date: May 12, 1998
Title: Dynamic Memory Word Line Driver Scheme
Inventor: Valerie Lines
Assignee: MOSAID Technologies Incorporated

Patent Number: 5,822,253
Date: Oct 13, 1998
Title: Dynamic Memory Word Line Driver Scheme
Inventor: Valerie Lines
Assignee: MOSAID Technologies Incorporated

Patent Number: 6,278,640 B1
Date: August 21, 2001
Title: Dynamic Memory Word Line Driver Scheme
Inventor: Valerie Lines
Assignee: MOSAID Technologies Incorporated

Pump Circuits

Patent Number: 5,406,523
Date: April 11, 1995
Title: High Voltage Boosted Word Line Supply Charge Pump and Regulator for DRAM
Inventors: Richard Foss, Valerie Lines, et al.
Assignee: MOSAID Technologies Incorporated

Patent Number: 5,828,620
Date: October 27, 1998
Title: High Voltage Boosted Word Line Supply Charge Pump and Regulator for DRAM
Inventors: Richard Foss, Valerie Lines, et al.
Assignee: MOSAID Technologies Incorporated

Patent Number: 6,236,581 B1
Date: May 22, 2001
Title: High Voltage Boosted Word Line Supply Charge Pump and Regulator for DRAM
Inventors: Richard Foss, Valerie Lines, et al.
Assignee: MOSAID Technologies Incorporated