

## COURSE INFORMATION

**Instructor**

Instructor: Dr. Michael S. McCorquodale  
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 Office Hours: (1 hour before and 1 hour after MW lectures)  
 Monday 11:00am - 12 noon / 1:30pm - 2:30pm  
 Wednesday 11:00am - 12 noon / 1:30pm - 2:30pm

**Lectures**

MW:	12 noon - 1:30pm	1303 EECS	(Full term)
*F:	12:30pm - 1:30pm	1018 DOW	(Jan. 5th only)
*Tu:	6:00pm - 7:00pm	1303 EECS	(Beginning week of Jan. 8th)

\*Note: After the first lecture, Friday lectures will be moved to Tuesday.

**Office Hours**

Office hours are the primary mechanism for individual contact with the instructor. All students are strongly encouraged to make use of office hours if they have questions on the course material.

**Course Description: Lecture only; 4 credit hours**

Integration density and performance of digital integrated circuits have undergone an astounding revolution in the last couple of decades. Over this time period, clock frequencies of microprocessors have doubled every three years, and they show no signs of slowing down. For both logic IC's and memories, integration complexity and density has doubled every ~2 years, in line with Gordon Moore's famed "law." Although innovative circuit and system design can account for some of these performance increases, technology has been the main driving force. This course will examine the process technology that has enabled the digital revolution and investigate new technologies and layout/circuit techniques aimed at sustaining the current rate of progress in digital integrated circuits. The goal is to achieve a working knowledge of the driving and limiting factors in circuit performance, of the design techniques employed, and of likely future trends.

There will be approximately four hours of lecture per week. The lectures will be supplemented by reading assignments (indicated on the COURSE SYLLABUS), additional reading material to be distributed throughout the course, problem sets (one every week or two), two midterm exams, and a final exam. Although much of the material covered in the lectures and in the reading is fundamentally the same, this will not always be the case. In addition, the perspectives between book and lecture material will often differ, and you are strongly encouraged to attend both the lecture and complete your reading assignments. Furthermore, there will be occasional announcements in lectures that will affect your problem sets and exams.

**This is not a circuits course.** This is, and has always been, a technology course. We recently changed the course title to "Digital Integrated Circuit Technology," in part since recent advances in digital integrated circuits have been dominated by advances in technology. Circuit design concepts will be discussed, but will not dominate the course content.

**Prerequisites**

Theoretically: EECS 311, 320, and 423 or 425. Practically: The basic assumption is that you are familiar with the following topics:

Transistor level design and analysis of common digital circuits (EECS 311/312), including logic circuits (e.g., inverters, NOR/NAND, and similar gates) and simple memory structures (e.g. flip-flops). An understanding of circuit simulation using SPICE with level 1 and 2 models is also expected.

Basic solid-state device operation and physics (EECS 320): diodes, bipolar junction transistors, and MOS field-effect transistors.

Very little familiarity with integrated circuit processing techniques is actually required. We review the topics of oxidation, diffusion, ion implantation, deposition, and etching so the 423/425 requirement is not enforced.

**Texts**

Required: S. Wolf, Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET. Sunset Beach, CA: Lattice Press, 1994.

R. C. Jaeger, Introduction to Microelectronic Fabrication (Vol. V of the Modular Series on Solid State Devices), 2nd edition, New York: Addison-Wesley, 2002.

Various material to be distributed throughout the semester

References: (on reserve at engineering library in Media Union)

S.A. Campbell, The Science and Engineering of Microelectronic Fabrication, 2nd edition, Oxford University Press, New York, 2001.

J.D. Plummer, M.D. Deal, and P.B. Griffin, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Prentice Hall, Upper Saddle River, NJ, 2001.

S. M. Sze, ed., VLSI Technology. New York: McGraw-Hill, 1983.

S. M. Sze, ed., Physics of Semiconductor Devices. New York: John Wiley, 1981.

G. S. May and S.M. Sze, Fundamentals of Semiconductor Fabrication, New York: John Wiley, 2004.

**Reading Assignments**

Reading assignments include sections of the required textbook, distributed readings, and supplementary notes handed out in lecture. Reading assignments are indicated in the COURSE SYLLABUS and will also be included in problem assignments where appropriate. Supplementary notes will be handed out for topics where lecture coverage is substantially different from the textbook. Students are responsible for all material in the reading. In particular, the scope of coverage for problem sets, the midterms, and the final examination includes the reading assignments as well as lecture material.

**Problem Sets**

There will be approximately 6-7 homework assignments during the semester. They will require anywhere from 1 to 2 weeks and as such the days of the week they will be assigned/due can fluctuate from assignment to assignment. No late homework will be accepted except under unusual circumstances. Solutions will be handed out in class.

**Midterms**

The approximate dates of the midterm exams in this course are indicated in your COURSE SYLLABUS. We will try to adhere to these dates as much as possible. The midterms will be held in class and will be 1.5 hours each.

**Final Exam**

The final exam will take place during the Examination period as indicated in your Time Schedules, and will cover all of the material in the course. This includes everything covered in problem sets, lectures, and readings.

**Grading Policy**

Course grades will be assigned according to the following grading formula. Please note that this formula is tentative; you will be informed of any changes.

Problem Sets:	25%
Midterm Exams:	40% (20% each)
Final Exam:	35%