

Final Exam: April 19, 2007

Instructions

Read all of the instructions before beginning the exam.

You must sign the Honor Pledge below to receive credit for the exam.

There are 3 problems on this final exam (with numerous sub-problems), totaling 100 points. The credit for each problem is given to help you allocate your time accordingly. Points for sub-problems are shown in boxes to the right of the problem. You have a total of 120 minutes to finish this exam. Do not spend all of your time on one problem. As always, focus on concepts and the framework for the solution to the problem. Significantly more partial credit will be awarded for properly framed solutions while little, if any, partial credit will be awarded for arbitrary computational effort.

This is an open-book, open-notes exam.

Please place a circle or box around your answers (both quantitative and qualitative ones). Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the back of the pages) for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions. Note that there are extra pages at the end of this exam. Lastly, reasonable assumptions can be made as long as they are justified.

Turn in the entire exam, including this cover sheet.

Put your name on any additional material that you submit.

Be sure to provide units where necessary.

Note that the last few pages of this exam provide data that may be useful.

Honor Pledge: I have neither given nor received any aid on this exam.

Signed: _____

Problem 1 Total: 30 points

Short Answer and Multiple Choice

(a) An nMOS gate is faster than a CMOS gate because the gate and S/D capacitive load is less by topology. This implies that nMOS technology is faster than CMOS. However, is nMOS faster than CMOS for high chip complexity? Why or why not? 2

(b) For very short thermal oxidation times and under fixed conditions, the oxide growth rate is limited by what (circle one)? 1

- (i) surface reaction rate
- (ii) mass transfer rate
- (iii) the mass transfer and surface reaction rates equally
- (iv) reactant concentration

(c) Considering anisotropic etch chemistries, why is overetching often required in MOS processing? 2

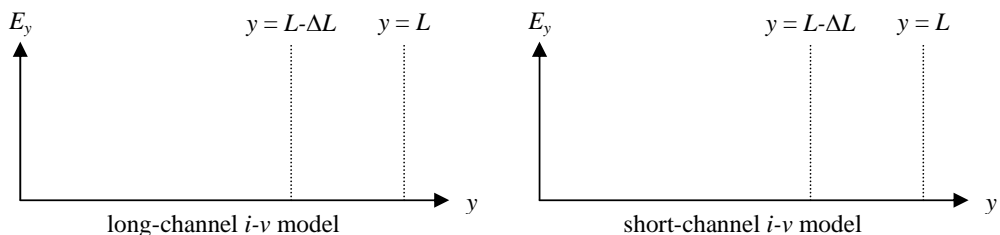
(d) Where is the channel-stop implant applied and what is its purpose? 2

(e) Propose at least 3 techniques by which punchthrough can be reduced in pMOS devices? 3

(f) In the development of the **short-channel** $i-v$ model for the VSR, which factors below had to be considered to develop a continuous and exponential horizontally-directed (y -directed) electrical field (E_y) in the device channel (circle all that apply)? 2

- (i) Inclusion of both mobile and static charge in the VSR
- (ii) Inclusion of both the y -directed and x -directed electrical fields in the VSR
- (iii) Inclusion of only the x -directed electrical fields in the VSR
- (iv) Inclusion of only the mobile charge in the VSR

(g) Sketch the horizontally-directed (y -directed) electrical field (E_y) in the device channel for a device in deep saturation for both the **long-channel** and **short-channel** $i-v$ model. 3



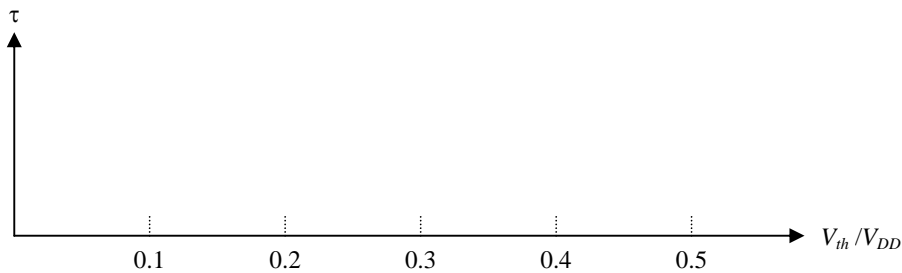
(h) What device breakdown mechanism is independent of scaling device channel length, L ? 1

(i) Would an n^- epitaxial layer over an n^+ substrate reduce latch-up as compared to a standard n -type wafer? Why or why not? 2

(j) Considering the parasitic BJTs that give rise to latch-up in CMOS, would a reduction in the minority carrier lifetime of these devices reduce the likelihood of latch-up? Why or why not? 2

(k) Fixed-voltage scaling in an uncommon scaling approach. Briefly and concisely explain why. 2

(l) Sketch the propagation delay, τ , vs. V_{th}/V_{DD} below. Clearly indicate the optimal operating region and indicate the reasons why other regions are sub-optimal. 3



(m) Why is dynamic threshold MOS (DTMOS) best suited to silicon-on-insulator (SOI) technology? 1

(n) What are the challenges associated with high-k gate dielectric materials (circle all the apply)? 1

- (i) Most are not stable on Si
- (ii) Most present a lower energy barrier height, thus gate current increases
- (iii) Most have lower thermal stability because they are metal-oxides
- (iv) Most are extremely rare as well as dangerous materials

(o) What is the primary purpose of strained-Si technology? 1

(p) After taking this course, which would be a more likely device technology that enters the main stream and why? (a) a new nanotechnology-based device that requires new processing techniques and CAD tools, but offers a 10x performance gain (b) a new and CMOS-compatible processing technique that offers a 1.5x performance gain 2

Problem 2 Total: 50 points

The simplified nMOS process flow with n+ poly-Si gate used in this problem is as follows. Assume all target thickness are actual and do NOT compute such thicknesses in the problem. *Note that you will be asked questions about a **scaled** version of this process.*

0. <100> p-type starting wafers, $N_A=10^{15}\text{cm}^{-3}$
1. LOCOS to define active region
2. Sacrificial pad oxide growth: Target=1000Å, 1200°C, 24min. dry O₂
3. Threshold implant: species=B, $E=30\text{keV}$, $Q=5\times 10^{12}\text{cm}^{-3}$
4. Strip sacrificial oxide
5. Gate oxidation: 950°C, 5min. dry O₂ + 2min. N₂ anneal. Target=45Å
6. *In-situ* Phosphorous doped polysilicon gate deposition: 650°C, 1hr. 35min. Target=2500Å, $N_{gate}=10^{20}\text{cm}^{-3}$ (assume $E_F = E_c$)
7. Gate definition
8. Re-oxidation: 1200°C, 3min. dry O₂ + 3min. N₂ anneal. Target=300Å total including gate oxide from 5
9. n+ S/D implant: species=Phosphorus, $E=10\text{keV}$, $Q=10^{12}\text{cm}^{-2}$ and anneal: 950°C, 30sec. in N₂
10. PSG deposition: 450°C. Target=3000Å
11. PSG densification: 950°C, 1min.
12. Contact hole mask
13. Metal deposition, masking, and patterning
14. Low temperature sintering

Device parameters for this process include the following:

$t_{ox} = 45\text{Å}$
 $x_j = 40\text{nm}$
 $V_a = 0.5\text{V}$ for pMOS (assume buried channel) and nMOS
 $V_{DD} = 1.2\text{V}$
 $L_{min} = 0.12\mu\text{m}$
 $W_{min} = 0.24\mu\text{m}$

Assume that dopants have no preference between moving into oxide and staying in silicon (i.e. no dopant redistribution). This implies that as an oxide grows, dopants in the path of the oxide end up in the oxide; those that are not reached by the edge of the oxide stay in the silicon. *Ignore the thermal budget of steps with temperatures below 800°C.*

- (a) Suppose that you are responsible for this process technology and you are developing a constant-field (full) **scaled** version of this process where $S=1.2$. Given this scaling factor, specify the **new** threshold voltage implant recipe (species, energy, dose). Be certain to consider all parameters that scale in including: t_{ox} and N_{sub} . Assume for both the current process and the scaled process that ΔV_{th} is proportional to the dose, D_I . **Do not** concern yourself with x_{dtest} . 15
- (b) List the **new** L , W , t_{ox} and V_{DD} for the **scaled** technology (assume x_j is also scaled by $1/S$). Given the V_{th} computed in (a) above, compute the drain current, I_D , for a fully-on ($V_{GS}=V_{DS}=V_{DD}$) minimum-sized nMOS device in this **newly scaled** technology where the nMOS device in deep saturation. **Do not iterate**. 12
- (c) Suppose your manager becomes concerned about device reliability for wide devices due to junction breakdown in the scaled technology. In particular, he is concerned about the newly scaled x_j . He asks you to consider extending the densification time in step 11. In particular, he asks you to consider a driver device with width $100\times W_{min}$ ($20\mu\text{m}$). Assume that junction breakdown occurs when $I_{sub}\times R_{sub}$ is equal to 1V. Assume $S\times N_{sub}$ for the background concentration, $R_{sub}=100\text{k}\Omega$, $V_D = V_{DD}$ and use I_D and V_{Dsat} from part (b) above. However scale I_D from (b) by $100\times$ to account for the width of concern ($20\mu\text{m}$). The diffusion coefficient for Phosphorus at 950°C is $6.5\times 10^{-15}\text{cm}^2/\text{s}$. Lastly, use the expression $I_{sub} = I_D(V_D - V_{Dsat})A_I/B_I e^{-B_I/E_m}$. To what time do you extend the densification step to avoid junction breakdown? 23

Problem 2 (work area)

Problem 2 (work area)

Problem 3 Total: 20 points

Suppose you work on a microprocessor that is being retargeted to a new technology node that is under development and about which you know nothing other than it is a constant field (or full) scaled version of the 90nm technology with parameters as listed below. The new scaled technology will use $S=1.2$.

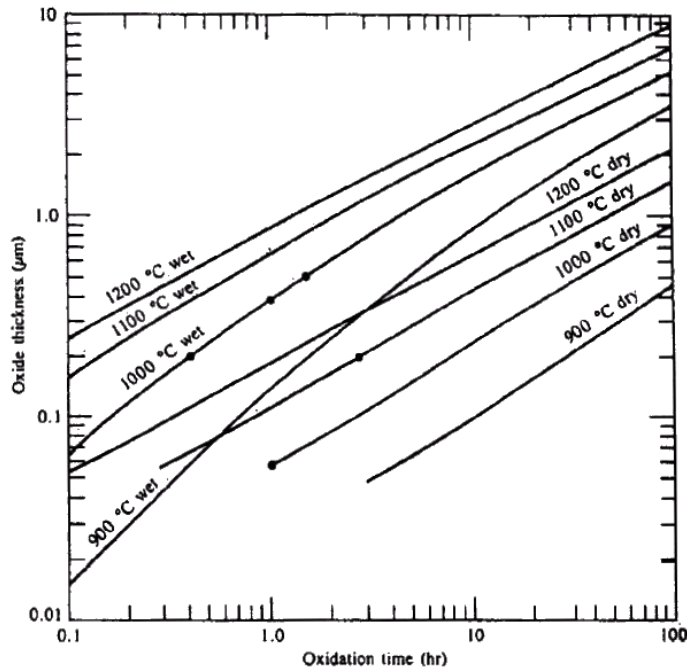
- $t_{ox} = 50\text{\AA}$
- $x_j = 10\text{nm}$
- $V_a = 0.5\text{V}$ for pMOS (assume buried channel) and nMOS
- $V_m = |V_{tp}| = 200\text{mV}$
- $V_{DD} = 1\text{V}$
- $L_{min} = 90\text{nm}$
- $W_{min} = 180\text{nm}$

- (a) For the current 90nm node, compute I_{Dsat} for a minimum-sized nMOS device where $V_{GS} = V_{DD}$. 5
- (b) List the relevant device parameters (L , W , V_{th} , V_{DD} , I_{Dsat} , t_{ox}) for the **scaled** technology node assuming $S=1.2$. 3
- (c) Consider the two expressions for propagation delay given below. Determine the percentage improvement in propagation delay for a minimum-sized inverter between the scaled and 90nm technology node using both expressions. Assume C_L is dominated by the gate capacitance for another minimum-sized inverter where the nMOS and pMOS devices are equally sized (i.e. ignore C_{SD} and $C_{interwire}$). Also assume $I_{av}=I_{Dsat}$ from part (a) above. Comment very briefly on the difference. 5

$$\tau \propto \frac{C_L V_{DD}}{I_{av}} \qquad \tau \propto \frac{C_L L^{0.5} t_{ox}^{0.5}}{V_{DD}^{0.3} (0.9 - V_{th}/V_{DD})^{1.3}}$$

- (d) In constant field (full) scaling, the doping concentration is increased. For simplicity, assume this causes the well-to-substrate capacitance to increase by S and the well and substrate resistance to decrease negligibly. Show, analytically (by expression and not computation) whether or not the scaled technology node is more or less susceptible to latch-up while only considering the generation current as the mechanism. Assume that the same power supply rise time is the same for the two technologies. Consider that all other parameters scale as would be expected for constant field (full) scaling. 7

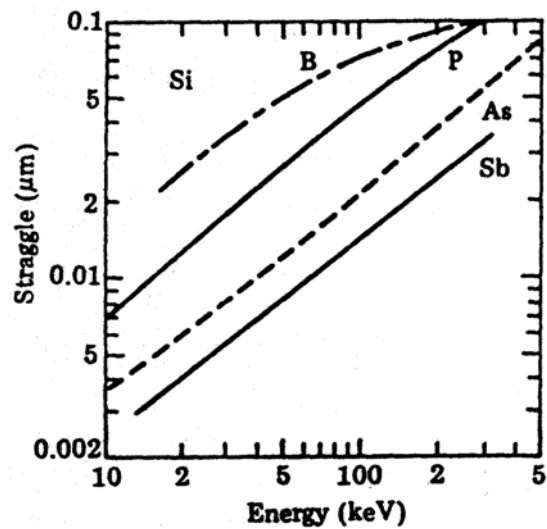
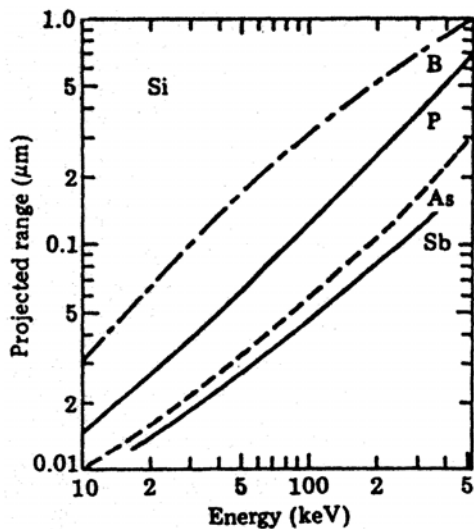
Useful Data



Wet and dry silicon dioxide growth for (100) silicon

Typical Diffusion Coefficient Values for a Number of Impurities

Element	D_0 (cm ² /sec)	E_A (eV)
B	10.5	3.69
Al	8.00	3.47
Ga	3.60	3.51
In	16.5	3.90
P	10.5	3.69
As	0.32	3.56
Sb	5.60	3.95



Standard Normal Cumulative Probability Table

Cumulative probabilities for negative z-values are shown in the following table:



z	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
-3.4	0.0003	0.0003	0.0003	0.0003	0.0003	0.0003	0.0003	0.0003	0.0003	0.0002
-3.3	0.0005	0.0005	0.0005	0.0004	0.0004	0.0004	0.0004	0.0004	0.0004	0.0003
-3.2	0.0007	0.0007	0.0006	0.0006	0.0006	0.0006	0.0006	0.0005	0.0005	0.0005
-3.1	0.0010	0.0009	0.0009	0.0009	0.0008	0.0008	0.0008	0.0008	0.0007	0.0007
-3.0	0.0013	0.0013	0.0013	0.0012	0.0012	0.0011	0.0011	0.0011	0.0010	0.0010
-2.9	0.0019	0.0018	0.0018	0.0017	0.0016	0.0016	0.0015	0.0015	0.0014	0.0014
-2.8	0.0026	0.0025	0.0024	0.0023	0.0023	0.0022	0.0021	0.0021	0.0020	0.0019
-2.7	0.0035	0.0034	0.0033	0.0032	0.0031	0.0030	0.0029	0.0028	0.0027	0.0026
-2.6	0.0047	0.0045	0.0044	0.0043	0.0041	0.0040	0.0039	0.0038	0.0037	0.0036
-2.5	0.0062	0.0060	0.0059	0.0057	0.0055	0.0054	0.0052	0.0051	0.0049	0.0048
-2.4	0.0082	0.0080	0.0078	0.0075	0.0073	0.0071	0.0069	0.0068	0.0066	0.0064
-2.3	0.0107	0.0104	0.0102	0.0099	0.0096	0.0094	0.0091	0.0089	0.0087	0.0084
-2.2	0.0139	0.0136	0.0132	0.0129	0.0125	0.0122	0.0119	0.0116	0.0113	0.0110
-2.1	0.0179	0.0174	0.0170	0.0166	0.0162	0.0158	0.0154	0.0150	0.0146	0.0143
-2.0	0.0228	0.0222	0.0217	0.0212	0.0207	0.0202	0.0197	0.0192	0.0188	0.0183
-1.9	0.0287	0.0281	0.0274	0.0268	0.0262	0.0256	0.0250	0.0244	0.0239	0.0233
-1.8	0.0359	0.0351	0.0344	0.0336	0.0329	0.0322	0.0314	0.0307	0.0301	0.0294
-1.7	0.0446	0.0436	0.0427	0.0418	0.0409	0.0401	0.0392	0.0384	0.0375	0.0367
-1.6	0.0548	0.0537	0.0526	0.0516	0.0505	0.0495	0.0485	0.0475	0.0465	0.0455
-1.5	0.0668	0.0655	0.0643	0.0630	0.0618	0.0606	0.0594	0.0582	0.0571	0.0559
-1.4	0.0808	0.0793	0.0778	0.0764	0.0749	0.0735	0.0721	0.0708	0.0694	0.0681
-1.3	0.0968	0.0951	0.0934	0.0918	0.0901	0.0885	0.0869	0.0853	0.0838	0.0823
-1.2	0.1151	0.1131	0.1112	0.1093	0.1075	0.1056	0.1038	0.1020	0.1003	0.0985
-1.1	0.1357	0.1335	0.1314	0.1292	0.1271	0.1251	0.1230	0.1210	0.1190	0.1170
-1.0	0.1587	0.1562	0.1539	0.1515	0.1492	0.1469	0.1446	0.1423	0.1401	0.1379
-0.9	0.1841	0.1814	0.1788	0.1762	0.1736	0.1711	0.1685	0.1660	0.1635	0.1611
-0.8	0.2119	0.2090	0.2061	0.2033	0.2005	0.1977	0.1949	0.1922	0.1894	0.1867
-0.7	0.2420	0.2389	0.2358	0.2327	0.2296	0.2266	0.2236	0.2206	0.2177	0.2148
-0.6	0.2743	0.2709	0.2676	0.2643	0.2611	0.2578	0.2546	0.2514	0.2483	0.2451
-0.5	0.3085	0.3050	0.3015	0.2981	0.2946	0.2912	0.2877	0.2843	0.2810	0.2776
-0.4	0.3446	0.3409	0.3372	0.3336	0.3300	0.3264	0.3228	0.3192	0.3156	0.3121
-0.3	0.3821	0.3783	0.3745	0.3707	0.3669	0.3632	0.3594	0.3557	0.3520	0.3483
-0.2	0.4207	0.4168	0.4129	0.4090	0.4052	0.4013	0.3974	0.3936	0.3897	0.3859
-0.1	0.4602	0.4562	0.4522	0.4483	0.4443	0.4404	0.4364	0.4325	0.4286	0.4247
0.0	0.5000	0.4960	0.4920	0.4880	0.4840	0.4801	0.4761	0.4721	0.4681	0.4641

Effective Mobility, μ_{eff} , Parameters

Device	μ_0 [$\text{cm}^2/\text{V}\cdot\text{s}$]	E_0 [MV/cm]	ν
nMOS	670	0.67	1.6
pMOS (buried)	290	0.35	1
pMOS (surface)	160	0.7	1

Empirical E_{eff} Parameters

$V_a = 0.5\text{V}$ for both nMOS and pMOS

Saturation Velocities

e^- in Si: $v_{sat} = 10^7 \text{cm/s}$

h^+ in Si: $v_{sat} = 8 \times 10^6 \text{cm/s}$

Impact Ionization Parameters

e^- in Si: $A_I = 2 \times 10^6 \text{cm}^{-1}$ and $B_I = 1.7 \times 10^6 \text{V/cm}$

h^+ in Si: $A_I = 8 \times 10^6 \text{cm}^{-1}$ and $B_I = 3.7 \times 10^6 \text{V/cm}$

Si-SiO₂ barrier height: $\phi_b = 3.2\text{eV}$

Impact ionization activation energy: $\phi_i = 1.5\text{eV}$

Constants

$q = 1.602 \times 10^{19} \text{C}$

$\epsilon_0 = 8.85 \times 10^{-14} \text{F/cm}$

Si : $\epsilon_r = 11.7$

SiO₂ : $\epsilon_r = 3.9$

$n_i = 1.45 \times 10^{10} \text{cm}^{-3}$

$kT/q = 26\text{mV}$