Information Regarding the Final Exam

Overview

This information sheet documents the details regarding the final exam.

Date, Time, and Location of Exam

Thursday April 19, 2007 at 1:30PM ET (sharp) – 3:30PM ET (hard stop) in 1670CSE (this is NOT our lecture room and is in the CSE building). You will have 2 full hours for this exam.

General Information

The exam will be open book and open notes. As before, any tables you require will be included on the exam including parameters for empirical expressions. Bring a calculator to the exam. You do not need a bluebook. You must include all of your work on your exam for full credit. The lecture notes are sufficient to perform well on the exam and other materials that have been distributed are merely supplemental. *This exam is cumulative and covers all topics in the course*. The depth of coverage will be up to as deep, but not deeper, than the coverage on previous exams.

The exam will be scored out of 100 points. It will follow a format similar to Midterm #2 and consist of some multiple-choice and short answers questions worth ~25 points total and 3 moderately-sized multi-part problems each worth ~25 points.

This course can be divided into 3 sections as listed below. The main topics from each section are listed below along with the percentage coverage.

Pre Midterm #1	Pre Midterm #2	Post Midterm #2
History of circuit technology Performance metrics and advantages and disadvantages of different device technologies Process modules including oxidations, film deposition, etching, ion implantation, diffusion and lithography CMOS process flow Threshold voltage implant Subthreshold swing	General MOS *i-v* modeling approaches including the 1-D (long channel) and quasi-2D (short channel) approaches Motivation for and details of short-channel *i-v* modeling including all regions of operation: linear, onset of saturation, deep saturation, and breakdown. In particular, an understanding of velocity saturation and the VSR along with mobility degradation are paramount. Hot carrier effects including: impact ionization, substrate current, gate current, etc. Device breakdown mechanisms and reliability Techniques for reducing hot carrier effects, particularly LDD Other short channel effects including: S/D resistance, GDE, geometric charge termination, narrow gate width effects, etc.	Latch-up mechanisms and reduction techniques including process and layout New isolation technologies and latch-up protection Scaling theory including scaling approaches for device parameters, interconnect and threshold voltage Current work in CMOS process technology including DTMOS, dual gate MOS, FinFET, strained Si, PD/FD-SOI, high-k gate dielectrics and metal gates
35–40%	35–40%	25%

The exam will focus most heavily on concepts and the application of concepts. Points will be awarded much more generously for properly applied concepts (even if final numeric solutions are incorrect) than for incorrectly applied mechanical approaches. Students are encouraged to understand the motivations for the approaches presented in lecture such that concepts can be leveraged and/or extrapolated to address unfamiliar problems.

I will be available for questions during the exam.