Midterm #1: February 19, 2007

Instructions

Read all of the instructions before beginning the exam.

You must sign the Honor Pledge below to receive credit for the exam.

There are 3 problems on this midterm exam (with numerous sub-problems), totaling 100 points. The credit for each problem is given to help you allocate your time accordingly. Points for sub-problems are shown in boxes to the right of the problem. You have a total of 90 minutes to finish this exam. Do not spend all of your time on one problem.

This is an open-book, open-notes exam.
Please place a circle or box around your answers (quantitative ones). Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the back of the pages) for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions. Note that there are extra pages at the end of this exam. Lastly, reasonable assumptions can be made as long as they are justified. For example, consider the peak concentration, N_o, of an impurity against a background concentration N_B. If $N_o >> N_B$, then N_B can be ignored when considering the net, or total, concentration.

Turn in the entire exam, including this cover sheet.

Put your name on any additional material that you submit.

Be sure to provide units where necessary.

Note that the last pages of this exam provide data that may be useful.

Honor Pledge: I have neither given nor received any aid on this exam.

Signed: ____

Problem 1 Total: 25 points

Short Answer and Multiple Choice

(a) Which technology was first in volume production, nMOS or pMOS, and why? 2

(b) What is the most significant disadvantage to logic gates based on bipolar technology as compared to CMOS technology? 2

(c) What percentage of the Si is consumed during oxidation via CVD (circle one)? 2

(i) 46%
(ii) 54%
(iii) 0%
(iv) 100%

(d) For very long thermal oxidation times and under fixed conditions, the oxide growth rate is limited by what (circle one)? 1

(i) surface reaction rate
(ii) mass transfer rate
(iii) the mass transfer and surface reaction rates equally
(iv) reactant concentration

(e) Why would a process engineer choose to deposit metal via sputtering as opposed to evaporation? 2

(f) In a CF_4 RIE chemistry, which plasma species is most reactive (circle one)? Note: superscripts indicate ion charge. 2

(i) CF^+
(ii) F^+
(iii) F^-
(iv) F^0

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(g) A process engineer wishes to etch a deep and narrow trench for a capacitor in a DRAM cell. Which etch technology is he or she most likely to select and why (circle one; then explain below)?

(i) Physical sputtering
(ii) Wet chemical etching
(v) RIE using a surface damage mechanism
(vi) RIE using a surface inhibitor chemistry

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Why would he or she select the etch technology you selected above?

1

(h) Ion implantation is a common technique for adjusting the threshold voltages of MOS devices. This approach adjusts the threshold voltage by an amount proportional to the dose. However, it has been shown that at large doses the change in threshold voltage is proportional to the root of the dose. Why does this latter case occur (circle one)?

(i) At large doses the Si does not absorb as much of the dose
(ii) At large doses the dose depth, x_s, exceeds the maximum depletion region, $x_{d,max}$
(iii) At large doses the implant looks like a sheet of charge
(iv) At large doses the maximum depletion region, $x_{d,max}$, is larger than the dose depth, x_s

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(i) Define subthreshold swing and propose device parameter modifications that minimize it.

3

(j) Why is drain-induced barrier lowering (DIBL) a bigger problem for buried channel devices as compared to surface channel devices?

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(k) In the table cells below, indicate qualitatively how you would modify (increase or decrease) the device parameters in each column to reduce punch-through and improve subthreshold swing (I_{Dst}) for a MOSFET. L is the device channel length, x_j is the source/drain junction depth, t_{ox} is the gate oxide thickness, and N_{ch} is the channel doping concentration. Use the following notation: (↑) indicates increase the parameter, (↓) indicates decrease the parameter, and (—) indicates no change in the parameter.

	L	x_j	t_{ox}	N_{ch}
Punch-through				
Subthreshold swing (I_{Dst})				

Problem 2 Total: 30 points

IC Fabrication Technology

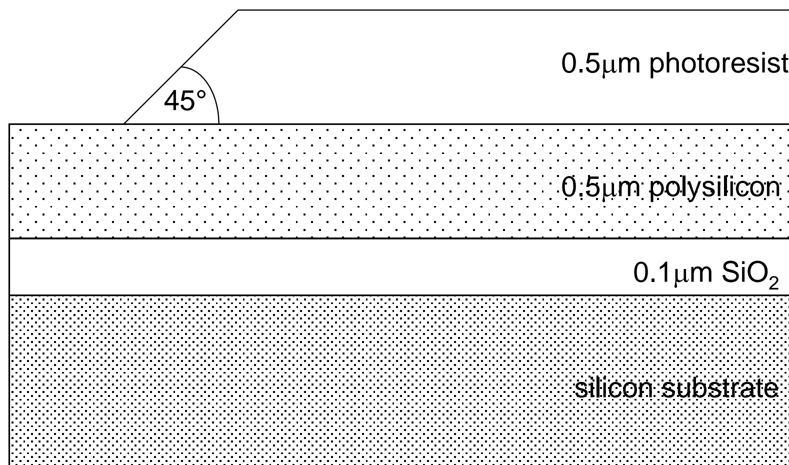
The cross-section of a polysilicon-oxide-silicon substrate sandwich structure with a photoresist pattern on top is shown. The pattern is etched in a plasma. Assume that the etch is 100% anisotropic; that the selectivity of silicon (and polysilicon):SiO_2:photoresist is 2:1:1; and that the etch rate of silicon (and polysilicon) is 0.1μm/min. Carefully draw cross-sections of the structure after:

(a) 2 minutes of etching — 5

(b) 5 minutes of etching — 10

(c) 11 minutes of etching — 15

Be certain to specify relevant angles and dimensions for each cross-section.



Problem 2 (work area)

Problem 3 Total: 45 points

MOS Fabrication Process

The simplified nMOS process flow with n+ poly-Si gate used in this problem is as follows:

0. <100> p-type starting wafers, $N_A=10^{15}$ cm^{-3}
1. LOCOS to define active region
2. Sacrificial oxide growth: Target=1000Å, 1200ºC, 24min. dry O_2
3. Threshold implant: species=unknown, E=unknown, Q =unknown
4. Strip sacrificial oxide
5. Gate oxidation: 950ºC, 5min. dry O_2 + 2min. N_2 anneal. Target=45Å
6. *In-situ* Phosphorous doped polysilicon gate deposition: 650ºC, 1hr. 35min. Target=2500Å, $N_{gate}=10^{20}$cm^{-3} (assume $E_F = E_c$)
7. Gate definition, drawn poly gate length, L=0.18μm
8. Re-oxidation: 1200ºC, 6min. dry O_2 + 3min. N_2 anneal. Target=500Å
9. n+ S/D implant: species=Phosphorus, E=80keV, $Q=10^{15}$cm^{-2} and anneal: 1200ºC, 1min. in N_2
10. PSG deposition: 450ºC. Target=3000Å
11. PSG densification: 950ºC, 10min.
12. Contact hole mask
13. Metal deposition, masking, and patterning
14. Low temperature sintering

Assume that dopants have no preference between moving into oxide and staying in silicon (i.e. no dopant redistribution). This implies that as an oxide grows, dopants in the path of the oxide end up in the oxide; those that are not reached by the edge of the oxide stay in the silicon. *Ignore the thermal budget of steps with temperatures below 800ºC.*

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(a) Suppose you work for *Not-So-Honest Semiconductor Corp.* (*NSHSC*) in a country where intellectual property rights are not well-enforced. Your colleague has just returned from a visit to *Very-Honest Semiconductor Corp.* (*VHSC*) in Taiwan where he has stolen the nMOS recipe above. However, he was unable to obtain the threshold voltage implant specification. Thus, your manager asks you to specify the threshold voltage for the device assuming V_t=500mV. He tells you to assume that ΔV_t will be proportional to the dose and he asks you to place the implant peak at the interface between the pad oxide and the Si. What threshold voltage implant do you specify for your manager (species, energy, dose)?

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(b) Another colleague of yours returns from a separate visit to *VHSC* where he has successfully stolen the threshold voltage implant specification. He tells you and your manager that it is Boron, 60keV and 1.5×10^{14}cm^{-2}. Now what is the V_t of the devices with this implant specification?

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(c) Your colleagues at *NSHSC* are not very clever. They have stolen this nMOS recipe for use in high voltage electronics for automobiles that their customer is knocking-off from the Germans. Your manager is concerned that at high drain voltages, the devices may fail. Assuming the simple model presented in lecture (i.e. where the gate field is ignored), at what minimum drain voltage, V_{DS}, will minimum length devices (L=0.18μm) fail from punch-through due to DIBL? Assume the source is grounded and use the threshold voltage implant specification in (b) such that $N_{ch}=N_s$.

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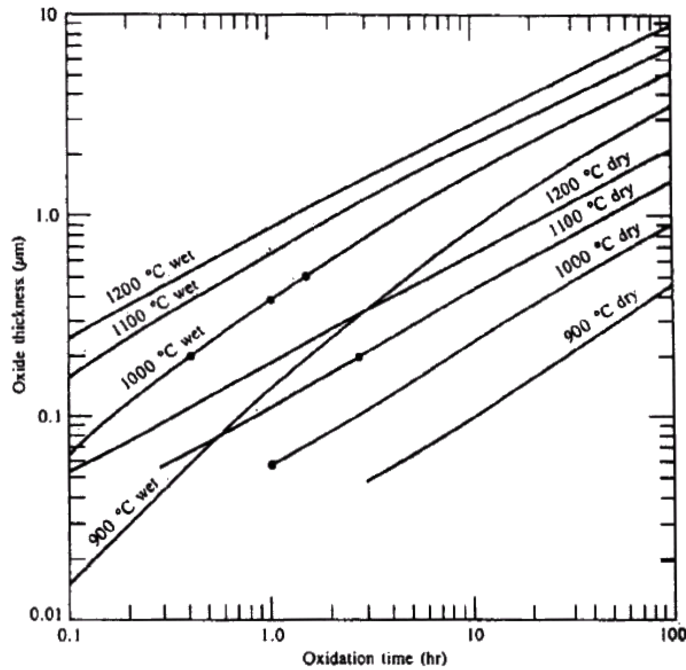
(d) Because you have integrity as a Michigan alumnus, you resign from *NSHSC* and move to Taiwan to work for *VHSC*. You tell the management at *VHSC* that *NSHSC* has stolen their nMOS recipe. *VHSC* sues *NSHSC*, but the judge's preliminary ruling is that all devices at this technology node behave more or less the same (V_{DD}, I_{DD}, V_t, etc.), thus there is insufficient proof that the process recipes are the same. The attorneys at *VHSC* ask you to somehow prove the egregious case that the threshold voltage implant recipes are exactly identical. You tell the attorneys that you can do this by measuring the threshold voltage, V_t, as a function of $(|\Psi_s| + |V_{SB}|)^{1/2}$. Qualitatively sketch a plot of what you would expect to measure. Label the slopes as variables (not numeric values) and indicate any breakpoints. You do not need to solve anything numeric in this problem.

Problem 3 (work area)

Problem 3 (work area)

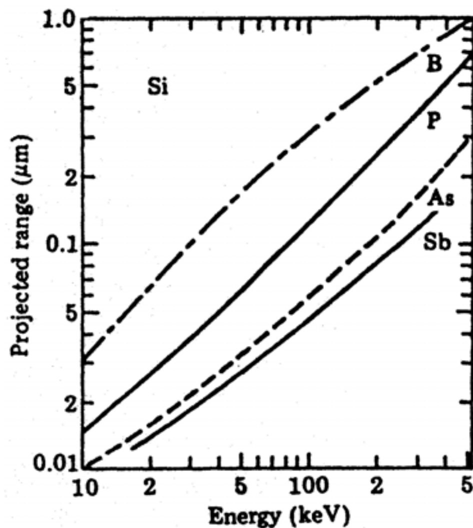
Useful Data

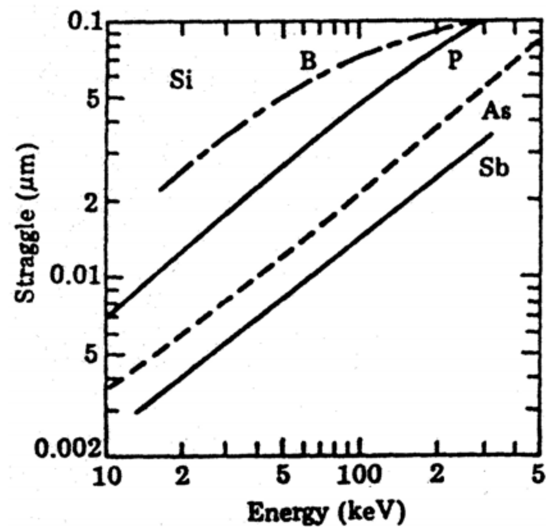


Wet and dry silicon dioxide growth for ⟨100⟩ silicon

Typical Diffusion Coefficient Values for a Number of Impurities

Element	D_o (cm^2/sec)	E_A (eV)
B	10.5	3.69
Al	8.00	3.47
Ga	3.60	3.51
In	16.5	3.90
P	10.5	3.69
As	0.32	3.56
Sb	5.60	3.95





Standard Normal Cumulative Probability Table

Cumulative probabilities for negative z-values are shown in the following table:

z	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
-3.4	0.0003	0.0003	0.0003	0.0003	0.0003	0.0003	0.0003	0.0003	0.0003	0.0002
-3.3	0.0005	0.0005	0.0005	0.0004	0.0004	0.0004	0.0004	0.0004	0.0004	0.0003
-3.2	0.0007	0.0007	0.0006	0.0006	0.0006	0.0006	0.0006	0.0005	0.0005	0.0005
-3.1	0.0010	0.0009	0.0009	0.0009	0.0008	0.0008	0.0008	0.0008	0.0007	0.0007
-3.0	0.0013	0.0013	0.0013	0.0012	0.0012	0.0011	0.0011	0.0011	0.0010	0.0010
-2.9	0.0019	0.0018	0.0018	0.0017	0.0016	0.0016	0.0015	0.0015	0.0014	0.0014
-2.8	0.0026	0.0025	0.0024	0.0023	0.0023	0.0022	0.0021	0.0021	0.0020	0.0019
-2.7	0.0035	0.0034	0.0033	0.0032	0.0031	0.0030	0.0029	0.0028	0.0027	0.0026
-2.6	0.0047	0.0045	0.0044	0.0043	0.0041	0.0040	0.0039	0.0038	0.0037	0.0036
-2.5	0.0062	0.0060	0.0059	0.0057	0.0055	0.0054	0.0052	0.0051	0.0049	0.0048
-2.4	0.0082	0.0080	0.0078	0.0075	0.0073	0.0071	0.0069	0.0068	0.0066	0.0064
-2.3	0.0107	0.0104	0.0102	0.0099	0.0096	0.0094	0.0091	0.0089	0.0087	0.0084
-2.2	0.0139	0.0136	0.0132	0.0129	0.0125	0.0122	0.0119	0.0116	0.0113	0.0110
-2.1	0.0179	0.0174	0.0170	0.0166	0.0162	0.0158	0.0154	0.0150	0.0146	0.0143
-2.0	0.0228	0.0222	0.0217	0.0212	0.0207	0.0202	0.0197	0.0192	0.0188	0.0183
-1.9	0.0287	0.0281	0.0274	0.0268	0.0262	0.0256	0.0250	0.0244	0.0239	0.0233
-1.8	0.0359	0.0351	0.0344	0.0336	0.0329	0.0322	0.0314	0.0307	0.0301	0.0294
-1.7	0.0446	0.0436	0.0427	0.0418	0.0409	0.0401	0.0392	0.0384	0.0375	0.0367
-1.6	0.0548	0.0537	0.0526	0.0516	0.0505	0.0495	0.0485	0.0475	0.0465	0.0455
-1.5	0.0668	0.0655	0.0643	0.0630	0.0618	0.0606	0.0594	0.0582	0.0571	0.0559
-1.4	0.0808	0.0793	0.0778	0.0764	0.0749	0.0735	0.0721	0.0708	0.0694	0.0681
-1.3	0.0968	0.0951	0.0934	0.0918	0.0901	0.0885	0.0869	0.0853	0.0838	0.0823
-1.2	0.1151	0.1131	0.1112	0.1093	0.1075	0.1056	0.1038	0.1020	0.1003	0.0985
-1.1	0.1357	0.1335	0.1314	0.1292	0.1271	0.1251	0.1230	0.1210	0.1190	0.1170
-1.0	0.1587	0.1562	0.1539	0.1515	0.1492	0.1469	0.1446	0.1423	0.1401	0.1379
-0.9	0.1841	0.1814	0.1788	0.1762	0.1736	0.1711	0.1685	0.1660	0.1635	0.1611
-0.8	0.2119	0.2090	0.2061	0.2033	0.2005	0.1977	0.1949	0.1922	0.1894	0.1867
-0.7	0.2420	0.2389	0.2358	0.2327	0.2296	0.2266	0.2236	0.2206	0.2177	0.2148
-0.6	0.2743	0.2709	0.2676	0.2643	0.2611	0.2578	0.2546	0.2514	0.2483	0.2451
-0.5	0.3085	0.3050	0.3015	0.2981	0.2946	0.2912	0.2877	0.2843	0.2810	0.2776
-0.4	0.3446	0.3409	0.3372	0.3336	0.3300	0.3264	0.3228	0.3192	0.3156	0.3121
-0.3	0.3821	0.3783	0.3745	0.3707	0.3669	0.3632	0.3594	0.3557	0.3520	0.3483
-0.2	0.4207	0.4168	0.4129	0.4090	0.4052	0.4013	0.3974	0.3936	0.3897	0.3859
-0.1	0.4602	0.4562	0.4522	0.4483	0.4443	0.4404	0.4364	0.4325	0.4286	0.4247
0.0	0.5000	0.4960	0.4920	0.4880	0.4840	0.4801	0.4761	0.4721	0.4681	0.4641