Midterm #2: March 27, 2007

Instructions

Read all of the instructions before beginning the exam.

You must sign the Honor Pledge below to receive credit for the exam.

There are 4 problems on this midterm exam (with numerous sub-problems), totaling 100 points. The credit for each problem is given to help you allocate your time accordingly. Points for sub-problems are shown in boxes to the right of the problem. You have a total of 120 minutes to finish this exam. Do not spend all of your time on one problem. Note that Problem #2 requires the most computation, Problem #3 requires less, and Problem #4 requires the least. This information may help you allocate your time more appropriately. Despite computational effort, and as always, focus on concepts and the framework for the solution to the problem. Significantly more partial credit will be awarded for properly framed solutions while little, if any, partial credit will be awarded for arbitrary computational effort.

This is an open-book, open-notes exam.
Please place a circle or box around your answers (quantitative ones). Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the back of the pages) for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions. Note that there are extra pages at the end of this exam. Lastly, reasonable assumptions can be made as long as they are justified.

Turn in the entire exam, including this cover sheet.

Put your name on any additional material that you submit.

Be sure to provide units where necessary.

Note that the last page of this exam provides data that may be useful.

Honor Pledge: I have neither given nor received any aid on this exam.

Signed: ____

Problem 1 Total: 20 points

Short Answer and Multiple Choice (be concise with short answers)

(a) What simplifying assumptions are made in the gradual channel approximation as used in the development of the *i*-*v* relationship for **long-channel** MOSFETs? [2]

(b) In the **long-channel** *i*-*v* model, what is the velocity of charge carriers in the pinch-off region of a saturated MOSFET? [1]

(i) 0
(ii) v_{sat}
(iii) ∞
(iv) $v_{sat}/2$

(c) In the **long-channel** *i*-*v* model, toward what value does the horizontally-directed (*y*-directed) electrical field approach as *y* approaches the pinch-off region (i.e. $y \rightarrow L - \Delta L$)? [1]

(i) E_{sat}
(ii) ∞
(iii) 0
(iv) E_{sat}^2

(d) In the development of the **short-channel** *i*-*v* model, what are the 2 most significant physical phenomena that were modeled and which were not modeled in the **long-channel** *i*-*v* derivation? [2]

(e) How would one scale the device length, *L*, and gate oxide thickness, t_{ox}, to make a **short-channel** device perform more like a **long-channel** device? Specify whether to increase or decrease the parameter. You may use the following notation: ↑ for increase and ↓ for decrease. [2]

(f) As device length, *L*, approaches 0, what is the velocity of the charge carriers at the source? [1]

(g) What signal can be measured to determine the magnitude of impact ionization in a device? [1]

(h) Where in the channel of an nMOS device (that is in deep saturation) is the gate current, I_g, highest? **1**

(i) At the edge of the source
(ii) At the edge of the drain
(iii) Where the channel potential, $V(y)$, equals the gate potential, V_{GS}
(iv) None of the above; it is uniform across the channel

(i) Where in the channel of an nMOS device (that is in deep saturation) is impact ionization the highest assuming that $V_{GS}=V_{DS}= V_{DD}$? **1**

(i) At the edge of the source
(ii) At the edge of the drain
(iii) Where the channel potential, $V(y)$, equals the gate potential, V_{GS}
(iv) None of the above; it is uniform across the channel

(j) Hot carrier induced breakdown is less significant for pMOS devices as compared to nMOS devices because (circle all that apply): **2**

(i) The energy barrier for the hot carrier in pMOS devices is higher than in nMOS devices
(ii) Holes don't give rise to impact ionization
(iii) Electron temperature, T_e, approaches ∞ for holes
(iv) The majority carrier mobility, μ_{eff}, is less for pMOS devices than for nMOS devices

(k) Does hot-carrier induced degradation improve or degrade the drain current performance of pMOS devices? Why (be brief and concise)? **2**

(l) What is the primary purpose of the lightly doped drain (LDD) structure (be brief and concise)? **2**

(m) In a device with an LDD that has no gate overlap of the LDD region, it has been shown that the device lifetime, τ (as measured by $\Delta I_D/I_D$) is worse than for a non-LDD (conventional) device. Why (be brief and concise)? **2**

Problem 2 Total: 30 points

Short-Channel i-v Modeling

Suppose you are promoted to VP of Engineering at a major semiconductor company. One of the new revenue paths you propose is to cost-reduce old and successful product lines which are at an old technology node (i.e. **long-channel** node) to a new submicron technology node (i.e. **short-channel** node), thus substantially improving the gross margin of these existing products by decreasing device area and ultimately reducing cost. Your management team is concerned about redesign effort costs but you claim that the design can be directly scaled, thus effort and cost are minimal. A subsequent concern of your management team is in regard to performance degradation at the proposed submicron node since it is known that the saturated current drive cannot decrease by more than 70% for the product to function properly. Considering the parameters for the target submicron process below, prove your point by calculating the following: [Note: These parameters below are **identical** to Problem #4, thus you may reuse calculated parameters from that problem if you solved it first or you may use parameters from this problem in Problem #4.]

t_{ox} = 8nm
x_j = 20nm
V_a = 0.5V for pMOS (assume buried channel) and nMOS
$V_{tn} = |V_{tp}|$ = 450mV
V_{DD} = 1.8V
L_{min} = 0.18μm
W_{min} = 0.36μm

(a) What is the percentage performance degradation, in terms of I_D, for fully-on (i.e. $|V_{GS}|=|V_{DS}|=V_{DD}$) logic gates with minimum-sized (W_{min}/L_{min}) devices? [i.e. Calculate K_1 for a minimum-sized nMOS **and** pMOS device.] Will the product work at the new submicron node? **9**

(b) Calculate the drain current, I_D, for minimum-sized nMOS and pMOS devices. Assume $|V_{GS}|=|V_{DS}|=V_{DD}$ as in (a). Iteration is **NOT** required. **8**

(c) Suppose the maximum allowable propagation delay for the product to function properly is set by considering the slowest edge or equivalently the low-to-high output transition, τ_{pLH}, of an inverter with minimum-sized devices and this maximum is 1ns. Assume the total lumped load at the output of the inverter is 25fF. Will the new technology node meet this requirement? [The answer is "yes" or "no" but it must be supported quantitatively.] Use your result from (b) above for I_{av} in τ_{pLH}. **5**

(d) Now your management team is convinced and wishes to get more "bang for the buck" by scaling the operating frequency by a factor of 4. To do so, you determine that τ_{pLH} will need to be decreased by a factor of 2. Will the proposed submicron technology node meet the requirements? If not, what technology node (i.e. what minimum gate length, L) would? [Hint: Find gate length, L, such that the new τ_{pLH} requirement can be met.] Iteration is **NOT** required. **8**

Problem 2 (work area)

Problem 3 Total: 25 points

Hot Carrier and Short Channel Effects

Suppose you are a process engineer and you wish to introduce a new gate insulator material for an existing CMOS process technology such that hot carrier induced gate current, I_g, can be reduced. Suppose that this new material presents an energy barrier of 4eV to electrons (as compared to 3.1eV for SiO_2). Also, the relative dielectric constant of the new material is $\varepsilon_r = 4.5$ (as compared to 3.9 for SiO_2).

(a) By what factor is the gate current reduced assuming the mean free path, λ, for electrons is 10nm and the electric field is 5×10^5V/cm? [Hint: It may be useful to recall the probability that a carrier will travel a distance $d = \phi_b/qE$ is given by $P = e^{-\phi_b/\lambda qE}$ where ϕ_b is the barrier height.] — 10

(b) What is the effective gate oxide thickness with this new gate material and while accounting for gate depletion effect (GDE)? Consider an nMOS device with n+ poly gate where: $N_{gate} = 10^{19}\text{cm}^{-3}$, t_{ox} = 10nm (note this is the new material thickness where $\varepsilon_r = 4.5$), V_{GS} = 1.8V, $N_{sub} = 10^{17}\text{cm}^{-3}$, and V_{th} = 450mV. [Hints: This question is requesting the effective t_{ox}, as if the gate insulator was SiO_2, but accounting for the new gate insulator and GDE. Consider V_{poly} as the potential lost between the applied gate-source voltage, V_{GS}, and the effective gate-source voltage, V_{GS_eff}, as presented in lecture. For an n+ gate over an nMOS device, assume $\phi_{ms} = -E_g/2 - |\phi_f|$.] — 15

Problem 3 (work area)

Problem 4 Total: 25 points

LDD MOS Devices

Suppose you are responsible for a semiconductor product that is having field failures due to MOS device reliability. Your team determines that the device failure is due to hot carrier effects in nMOS devices and the failure occurs after 1 year (i.e. τ = 1yr.). Your current process technology does **NOT** use an LDD structure. Dogged by this field failure, your management team wishes to consider dramatic changes to improve product reliability to at least 20 years. Thus, you propose to migrate the design to a process technology of the same gate length, L, but with an LDD structure. Relevant process parameters for the proposed **LDD** technology are listed below: [Note: These parameters are **identical** to Problem #2, thus you may reuse calculated parameters from that problem.]

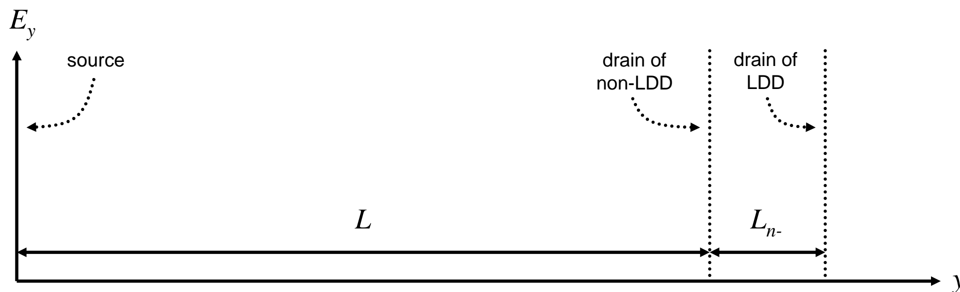
t_{ox} = 8nm
x_j = 20nm
V_a = 0.5V for pMOS (assume buried channel) and nMOS
V_{tn} = |Vtp| = 450mV
V_{DD} = 1.8V
L_{min} = 0.18µm
W_{min} = 0.36µm

(a) Assume for the current **non-LDD** technology that $(V_D - V_{Dsat})/l >> E_{sat}$, thus $E_m \approx (V_D - V_{Dsat})/l$. Also assume that the maximum horizontal (y-directed) electrical field, E_m, in the channel is 10^6V/cm and V_{Dsat} = 700mV for a fully-on minimum size device. Considering device lifetime, τ, in the form of $K(I_{sub}/I_D)^{-m}$ where m = -3 and K is unknown, compute K based on the fact that the device fails at 1 year. [5]

(b) Using your results for K above and for E_m and V_{Dsat} from Problem #2 (or recompute these variables with the **LDD** parameters shown), compute the device lifetime, τ, for the **LDD** process. Will the migration achieve the goal of reliability for at least 20 years? [5]

(c) Assume that the LDD doping is 2×10^{18}cm^{-3} and that the voltage is dropped **linearly** across the **entire** LDD region such that the field is 0 at the drain. Compute the LDD region length, L_{n-}. [Hint: The slope across the LDD region can be determined, from which L_{n-} can be found using E_m.] [6]

(d) Qualitatively sketch the horizontal (y-directed) electrical field for both the **non-LDD** and **LDD** device. Assume the gate length is the same for both and that the LDD device simply has the additional L_{n-} region. Label the maximum fields for each as E_m and E_m' respectively. [3]



(e) To justify the cost of design migration to the new **LDD** process, your management team also wishes to be able to scale the design from 500MHz (currently) to 2GHz while at the same process technology node. Can that be accomplished given the same desired device lifetime of 20 years? [The answer is "yes" or "no" but it must be supported quantitatively.] [3]

(f) Suppose it is identified that several inverters are causing the failure. A minor design change is introduced to decrease the input rise time from 100ps (currently) to 50ps, but the input fall time increases from 100ps (currently) to 400ps with the change. Does this design change enable the design to be scaled in the **LDD** process technology to 2GHz while maintaining 20 years of device lifetime? [The answer is "yes" or "no" but it must be supported quantitatively.] [3]

Problem 4 (work area)

Useful Data

Effective Mobility, μ_{eff}, Parameters

Device	μ_o [cm^2/V-s]	E_o [MV/cm]	ν
nMOS	670	0.67	1.6
pMOS (buried)	290	0.35	1
pMOS (surface)	160	0.7	1

Empirical E_{eff} Parameters
V_a = 0.5V for both nMOS and pMOS

Saturation Velocities
e^- in Si: $v_{sat} = 10^7$cm/s
h^+ in Si: $v_{sat} = 8\times10^6$cm/s

Impact Ionization Parameters
e^- in Si: $A_I = 2\times10^6$cm^{-1} and $B_I = 1.7\times10^6$V/cm
h^+ in Si: $A_I = 8\times10^6$cm^{-1} and $B_I = 3.7\times10^6$V/cm

Constants
$q = 1.602\times10^{19}$C
$\varepsilon_o = 8.85\times10^{-14}$F/m
Si : $\varepsilon_r = 11.7$
SiO_2 : $\varepsilon_r = 3.9$
kT/q = 26mV