

Information Regarding Midterm #2

Overview

This information sheet documents the details regarding Midterm #2.

Date, Time, and Location of Exam

Tuesday March 27, 2007 at 6PM ET (sharp) – 8PM ET (hard stop) in EECS Room 1303 (our standard lecture room). You will have 2 full hours for this exam.

General Information

The exam will be open book and open notes. As before, any tables you require will be included on the exam including parameters for empirical expressions. Bring a calculator to the exam. You do not need a bluebook. You must include all of your work on your exam for full credit. The lecture notes are sufficient to perform well on the exam and other materials that have been distributed are merely supplemental. This exam will cover lectures 14 – 26 (everything from MOS i - v modeling up to, but not including, latch-up). This exam is *not* cumulative and topics from the first Midterm will not be covered.

The exam will be scored out of 100 points. It will follow a format similar to Midterm #1 and consist of some multiple-choice and short answers questions worth ~20 points total and 2 large multi-part problems each worth ~40 points. However, this exam may include 3 moderate size multi-part problems. The average is likely to be low again, though more time will be provided for this exam thus it is less likely that students cannot complete the exam in the time allotted.

General topics to review include:

- a. General MOS i - v modeling approaches including the 1-D (long channel) and quasi-2D (short channel) approaches presented in lecture
- b. Motivation for and details of short-channel i - v modeling including all regions of operation: linear, onset of saturation, deep saturation, and breakdown. In particular, an understanding of velocity saturation and the VSR along with mobility degradation are paramount.
- c. Hot carrier effects including: impact ionization, substrate current, gate current, etc.
- d. Device breakdown mechanisms and reliability
- e. Techniques for reducing hot carrier effects, particularly LDD, along with techniques for increasing device reliability
- f. Other short channel effects including: S/D resistance, GDE, geometric charge termination, narrow gate width effects, etc.

The exam will focus most heavily on concepts and the application of concepts. Points will be awarded much more generously for properly applied concepts (even if final numeric solutions are incorrect) than for incorrectly applied mechanical approaches. Students are encouraged to understand the motivations for the approaches presented in lecture such that concepts can be leveraged and/or extrapolated to address unfamiliar problems.

A sample midterm, from a previous year, will be distributed in class.

I will be available for questions during the exam.