

PROBLEM SET 2

Issued: Tuesday, February 6, 2007

Due (at the beginning of class): Monday, February 19, 2007

The following pages comprise an actual 2 μ m p-well CMOS process flow with poly-to-poly capacitors (useful for non-digital applications, so we won't concern ourselves with it). No details are spared in this flow; even furnace program names are given, as are diagnostic steps used to verify each step. These details are included to present a more realistic situation. In doing this problem, you must sift through the extraneous information and concentrate on the recipe information (i.e. temperatures, times, implant doses, etc.).

Answer the following questions based upon this process.

- (a) Draw a qualitative cross-section corresponding to line A-A' in the layout (Figure 1). Identify layers and try to draw thicknesses to scale. You should distinguish between CVD oxides and thermally grown oxides (i.e. label them). Note that although capacitors are not used in this layout, you may need to account for the process steps involved with poly-to-poly capacitor formation to get a sufficiently accurate cross-section. Note that mask layers are identified in the drawing. (df) = dark field (i.e. geometry shows where an opening in the PR will be) and (cf) = clear field (i.e. geometry shows the portion to be covered by PR).
- (b) What is the gate oxide thickness t_{ox} ?
- (c) What is the depth x_{jn} of the nMOS n⁺ S/D junctions at the end of the process?
- (d) What is the depth x_{jp} of the pMOS p⁺ S/D junctions at the end of the process?
- (e) What is the gate-overlap capacitance:
 - (i) for nMOS devices?
 - (ii) for pMOS devices?
- (f) What is the threshold voltage V_{thn} for the nMOS devices of this process for zero source-to-bulk voltage, $V_{sb}=0$? Assume that the fixed charge in the gate oxide is negligible. (Note that this may or may not be a good assumption. Don't be surprised if you get a strange value for V_{thn} .)
- (g) What is the threshold voltage V_{thp} for the pMOS devices of this process for zero source-to-bulk voltage, $V_{sb}=0$? Assume that the fixed charge in the gate oxide is negligible. (Note that this may or may not be a good assumption. Don't be surprised if you get a strange value for V_{thp} .)
- (h) Calculate $k_n' = \mu_n C_{ox}$ and $k_p' = \mu_p C_{ox}$ for this process.
- (i) Assuming the p-well is tied to ground, what is the minimum value of voltage on a metal line over the field region in the p-well that would invert the p-well surface?
- (j) Assuming the n-substrate is tied to $V_{DD} = 5V$, what is the maximum value of voltage on a metal line over the field region in the n-substrate that would invert the n-substrate surface?

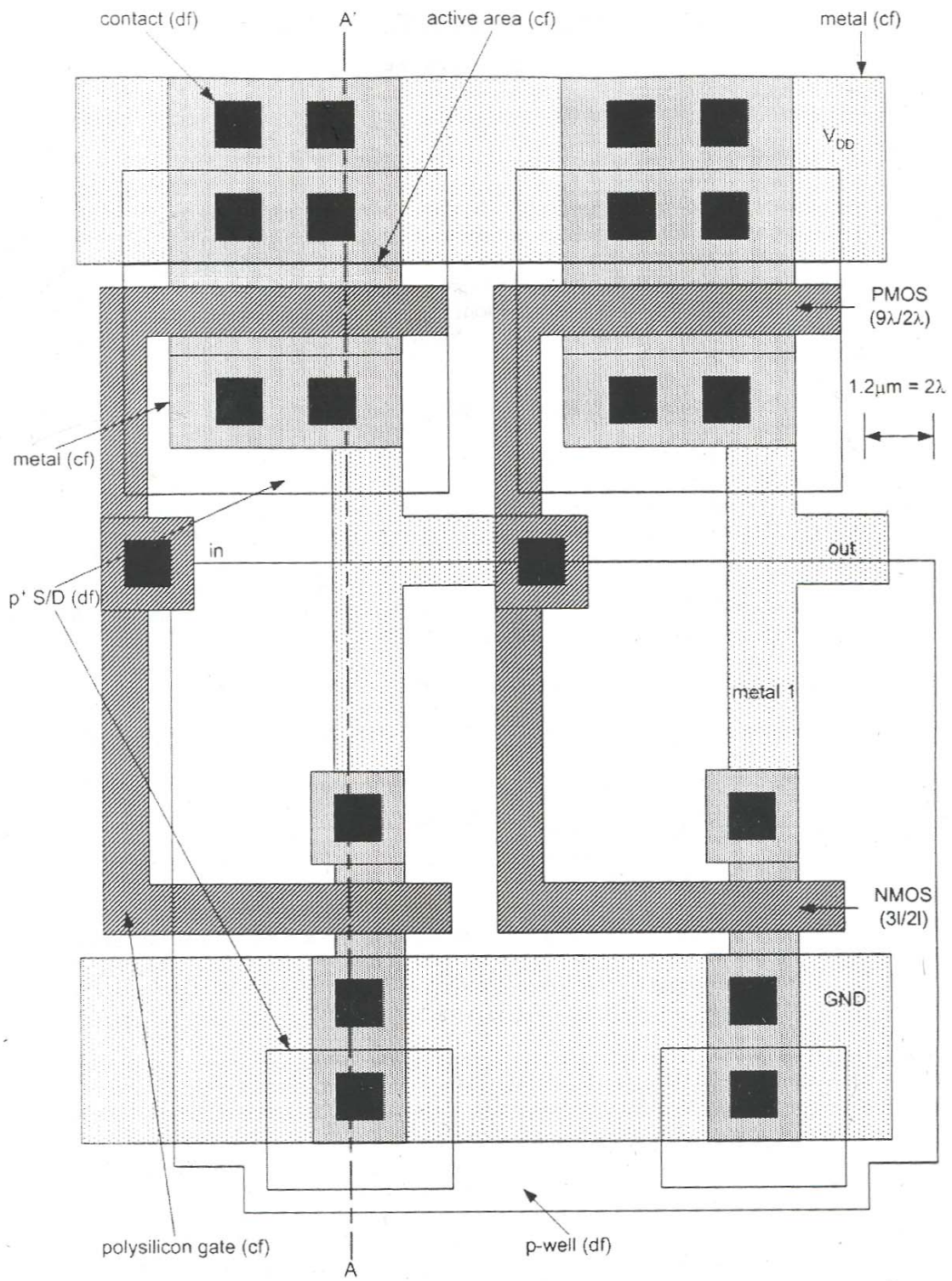


Figure 1

CMOS Process 2 μ m, P-well, double poly-Si, single metal (2P1M)	
0.0	Starting wafers: 8-12ohm-cm, n-type, <100> Control wafers: PWELL (n-type), PCH (n-type) Scribe lot and wafer number on each wafer, including controls. Measure bulk resistivity (ohm-cm) of PWELL.
1.0	Initial Oxidation: target = 1000(+/-5%)A
1.1	TCA clean furnace tube.
1.2	Std. clean wafers, include PWELL and PCH. Std. clean: piranha clean, DI rinse, BHF dip, spin-dry.
1.3	Wet oxidation at 1000C (SWETOXB): 5min. dry O2 9.5min. wet O2 5min. dry O2 20min. dry N2 Measure tox = ***
2.0	Punch-Through Implant Blanket implant: Phosphorus, 145keV, 1.2E12cm-2 Include PWELL and PCH.
3.0	Well Photo Mask: Control wafers are not included in any photoresist step. (PWELL proceeds to Step 4.0, PCH to Step 5.4)
3.1	Std. clean wafers. Dehydrate wafers in oven for >30min. at 120C.
3.2	Std. I-Line process: Spin, expose, develop, inspect, descum, hard bake. No etch. Resist is left on wafers.
4.0	Well Implant: Boron (B11), 3E12cm-2, 80keV. Include PWELL.
5.0	Well Drive-In: target $x_j = ***$, tox = 3500A
5.1	TCA clean furnace tube.
5.2	Etch pattern into oxide in 5/1 BHF. Strip oxide off of PWELL.
5.3	Remove PR in O2 plasma. Piranha clean wfrs.
5.4	Std. clean wfrs in include PWELL and PCH.
5.5	(a) Well drive-in at 1150C (WELLDLDR): 4 hrs dry O2 5 hrs dry N2 (b) Measure oxide thickness on work wafer. Measure two points on three wafers from different locations on the boat: front, middle and rear. tox(well) = *** tox(outside of well) = *** (c) Strip oxide and measure Rs on PWELL and PCH. RsPWELL = *** RsPCH = ***
5.6	TCA clean the furnace tube after well drive-in is done.
6.0	Pad Oxidation/Nitride Deposition: target = 300A SiO2 + 1000A Si3N4
6.1	TCA clean furnace tube.
6.2	Etch oxide in 5/1 BHF until wafers dewet.
6.3	Std. clean wafers. Include a tox monitoring wafer, PWELL and PCH.
6.4	Dry oxidation at 950C (SGATEOX): 1hr. dry O2 20min. dry N2 anneal. Measure tox on monitoring wafer. tox = ***
6.5	Deposit 1000A of Si3N4 immediately (SNITC): Include PWELL and PCH. Approx time = 23min., temp. = 800C. Measure nitride thickness on 3 work wafers, using tox obtained in 6.4. PWELL and PCH proceed to Step 13.3.
7.0	Active Area Photo Mask: Std. KTI process. Offset: x = 3.2420, y = 0.6155.
8.0	Nitride Etch: Plasma etch. Measure tox on each work wafer. Do not remove PR. Inspect. Measure PR thickness covering active area. tpr = *** PR must be >8kA. Hard bake again for >2hrs. at 120C.
9.0	P-Field Photo Mask: (basically, the pwell mask)
9.1	Std. KTI process. (Second photo) Inspect! Inside well, field is open and active areas are covered with Si3N4 and PR.
9.2	Measure PR thickness on active area. Wafers cannot be passed unless PR is >8kA. tpr = ***
10.0	P-Field (Channel Stop) Ion implant: B11, 100keV, 1E13cm-2
11.0	N-Field Photo Mask: (inverse of the pwell mask)
11.1	Remove PR in O2 plasma. Piranha clean wfrs. Dehydrate wfrs in oven for >30min. at 120C.
11.2	Std. I-Line process. Well area is covered with PR, active area with Si3N4.
12.0	N-Field (Channel Stop) Ion Implant: Phosphorus, 40keV, 5E12cm-2.
13.0	Locos Oxidation: target = ***
13.1	TCA clean furnace tube.

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- 13.2 Remove PR in O₂ plasma. Piranha clean wfrs.
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- 13.3 Std. clean wfrs include PWELL and PCH.
Dip in 10/1 BHF until field area dewets.
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- 13.4 Wet oxidation at 950C (SWETOXB):
5min. dry O₂
4hrs. 40 min wet O₂
5min. dry O₂
20min. N₂ anneal
Measure tox on 3 work wfrs. tox.= ***
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- 14.0 Nitride Removal
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- 14.1 Dip in 5/1 BHF for 30sec., include PWELL and PCH. (To remove thin oxide on top of the nitride)
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- 14.2 Etch nitride off in phosphoric acid at 145C.
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- 15.0 Sacrificial Oxide: target = 200(+/-20)A
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- 15.1 TCA clean furnace tube.
-
- 15.2 Std. clean wfrs, include PWELL and PCH.
Dip in 10:1 BHF until PWELL and PCH dewet.
-
- 15.3 Dry oxidation at 950C (SGATEOX):
30min. dry O₂
20min. N₂ anneal
Measure tox on 3 wfrs. tox = ***
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- 16.0 Threshold Implant:
Blanket implant: B11, 30keV, 9E11cm⁻².
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- 17.0 Gate Oxidation/Poly-Si Deposition:
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- 17.1 TCA clean furnace tube.
-
- 17.2 Std. clean wfrs, include PWELL, PCH and, 3 tox and 1 tpoly1 monitoring wafers.
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- 17.3 Dip off sacrificial oxide in 10/1 H₂O/HF until PWELL and PCH dewet (approx. 1min.).
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- 17.4 Dry oxidation at 950C (SGATEOX):
2hr. dry O₂
20min. N₂ anneal
Measure 5 pts. on each of the 3 tox monitoring wafers. tox = ***
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- 17.5 Immediately after oxidation deposit 4500A phosphorous doped poly-Si (SDOPOLYH).
approx.time = 2hr. 40min., temp. = 610C
Include tpoly1, PWELL and PCH.
tpoly1 = *** Measure 5 pts..
PWELL and PCH proceed to Step 20.2.
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- 18.0 Gate Definition Mask:
Std. I-Line process.
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- 19.0 Plasma etch poly-Si
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- 19.1 Etch poly. (CCl₄/He/O₂ at 300W, 280mT)
-
- 19.2 Measure tox. in S/D area of each work wafer.
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- 19.3 Remove PR in plasma O₂. Piranha clean wfrs.
Measure line width of 2 μ m gates on each work wafer.
One pt. measurement in 19.2 and 19.3.
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- 20.0 Capacitor formation:
Target = *** SiO₂ on 1st poly + 4500A 2nd poly
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- 20.1 TCA clean furnace tube.
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- 20.2 Std. clean wafers, include PWELL, PCH, tpoly1 and one of gate oxidation monitoring wafers as a 2nd poly monitoring wafer, tpoly2.
tpoly2 proceeds to Step 20.4.
From here on: only 10sec. dip in 25/1 H₂O/HF after piranha.
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- 20.3 Dry Oxidation at 950C (SDRYOXB):
55min. dry O₂
20min. N₂ anneal.
Measure oxide thickness on poly
tox(PWELL) = *** tox(PCH) = ***
PWELL proceeds to Step 24. PCH proceeds to Step 25.
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- 20.4 Second poly-Si deposition: immediately after oxidation deposit 4500A of phosphorus doped poly-Si (SDOPOLYH):
approx time = 2hr. 30min., temp.= 610C.
tpoly2 = ***
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- 21.0 Capacitor Photo Mask:
Std. I-Line process.
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- 22.0 Plasma etch poly-Si:
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- 22.1 Etch 2nd poly. Inspect.
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- 22.2 Measure tox. in S/D area on each work wafer.
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- 22.3 Remove PR in O₂ plasma. Piranha clean wfrs.
Dehydrate wfrs in oven for >30min. at 120C.
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- 22.4 Measure channel length. This measurement can be done at any step before Step 28.
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- 23.0 N+ S/D Photo Mask: (inverse of p+ S/D)
Std. I-line process. Do not hard bake.
Inspect. PMOS areas are PR covered. Capacitor areas are not.
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- 24.0 N+ S/D Implant: Arsenic, 160keV, 5E15cm⁻², incl. PWELL.
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- 25.0 N+ S/D Anneal
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- 25.1 TCA clean furnace tube.
-
- 25.2 Remove PR in O₂ plasma and piranha clean wafers (no dip here).
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- 25.3 Std. clean wafers, incl. PWELL and PCH.
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- 25.4 Anneal in N₂ at 925C for 1hr. 15min. (N₂ANNEAL).
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 26.0 P+ S/D Photo Mask:
 Std. I-Line process.
 All areas are covered with PR except PMOS areas.

 27.0 P+ S/D Implant: B11 at 30keV, 5E15cm-2, include
 PCH.

 28.0 PSG Deposition and Densification:
 target = 7000(+/-200)A

 28.1 Remove PR in O2 plasma and piranha clean wafers
 (no dip).

 28.2 Std. clean wfrs (10sec. dip).
 Include PWELL. PCH and one PSG monitoring
 wafer.

 28.3 Deposit 7000A PSG, PH3 flow at 10.3sccm
 (SDOLTOD).
 approx.time = 35min. (check current dep. rate)
 temp. = 450C

 28.4 Densify glass at 950C, immediately after PSG
 deposition (PSGDENS). Include PSG control.
 5min. dry O2
 20min. wet O2
 5min. dry O2.
 Measure tPSG = ***
 Etch oxide on PWELL and PCH and measure poly
 sheet resistivity on PWELL and PCH.

 28.5 Do wet oxidation dummy run afterwards to clean
 tube:
 1hr. wet oxidation at 950C (SWETOXB).

 29.0 Contact Photo Mask:
 Std. I-Line process.

 30.0 Contact Etch:
 Plasma etch. CHF3/CF4/He, 800 watts.

 31.0 Back side etch:

 31.1 Remove PR in O2 plasma, piranha clean wfrs (no
 dip).
 Dehydrate wafers in oven at 120C for >30min.

 31.2 Etch backside:
 (PWELL and PCH front side etch can be included in
 c), d) and e), and then proceed to 36.0).
 a) Spin PR on front side, do not expose; hard bake.
 b) Do a) again.
 c) Dip off oxide in 5:1 BHF until backside dewets.
 d) Etch poly-Si (poly2 thickness).
 e) Etch oxide off in 5:1 BHF until backside dewets.
 f) Etch poly-Si (poly1 thickness).
 g) Final dip in 5: 1 BHF until back dewets.
 h) Remove PR in O2 plasma, piranha clean wfrs (no
 dip).

 32.0 Metallization: target = 6000A
 Std. clean wfrs and do a >=30sec. 25/1 H2O/HF dip just
 before metallization.
 Sputter Al/2% Si on all wafers.

 33.0 Metal Photo Mask:
 Std. KTIprocess.
 Hard bake for >2hrs.

 34.0 Plasma etch Al.
 Remove PR in O2 plasma (no piranha).
 tAl = ***
 Probe test devices.

 35.0 Sintering: 400C for 20min. in forming gas.
 No ramping, (SINT400).

 36.0 Testing:
 2μm NMOS, PMOS devices, capacitors and inverter
 Measure the sheet resistivities of PWELL and PCH.

 End of Process
