PROBLEM SET 3

Issued: Tuesday, March 6, 2007

Due (at the beginning of class): Monday, March 19, 2007

1. For a long-channel MOSFET with channel length L:

   a. Derive expressions for the channel voltage $V(y)$ and the y-directed electric field $E_y(y)$ based upon the long-channel theory presented in lecture. To do so, equate the derived drain current expression for the linear region (as a function of terminal voltages and device parameters) to the general channel drift current expression based upon the mobile charge and according to the gradual channel approximation. Express both as functions of the threshold voltage V_{th}, geometric dimensions and applied voltages (i.e. V_{GS}, etc.). For your derivation, note that I_D is constant along y and take $V_S = V_B = 0$V.

   b. From the expressions derived, obtain equations for $V(y)$ and $E_y(y)$ that are valid when the MOSFET is at the edge of saturation.

   c. Using the results above, sketch $-E_y(y)L/(V_{GS}-V_{th})$ as a function of y over the range y=0 to y=L for V_{GS}>V_{th} and V_{DS}=(0.25, 0.50, 0.75, 1)×V_{DSAT}.

   d. Explain why $E_y(y)$ approaches a constant when V_{DS} is small.

   e. Find an expression for the total inversion charge in the channel (in Coulombs), in a transistor with width W, as a function of V_{GS}. You will need to use your result for $V(y)$ from part (a).

2. A submicron CMOS technology has the following specifications: t_{ox}=3nm and V_{th}=0.4V for the nMOSFET with n+ poly-Si gate and V_{th}=-0.4V for the pMOSFET with p+ poly-Si gate. For this problem, use $v_{sat}=10^7$cm/s for electrons and $v_{sat}=7\times10^6$cm/s for holes and assume α=0 (in the E_{eff} calculation) for both the nMOS and pMOS devices.

   a. Estimate I_{Dsat} and K_I of the fully on nMOSFET and fully on pMOSFET for two supply voltages: 1.8V and 1.2V. Assume L_{eff}=0.1μm and W=1μm. For this part, calculate the values for the parameters corresponding to the maximum drive capability of the device in question when used in a CMOS inverter application. For example, for a 1.8V supply, an nMOS transistor is driving the hardest at the start of the high-to-low transition when V_{GS}=1.8V.

   b. What are the percent improvements in I_{Dsat} if the nMOS and pMOS devices can be made with L_{eff}=0.02μm.

3. You are given a MOSFET for which:

$$Q_n = C_{ox}\left[V_G - V_{th} - V(y)\right]$$

   (i.e. ignore the increase in the bulk charge term along the channel) and

$$\mu_n = \mu_o\left[1+\frac{-E_y(y)}{E_{yc}}+\frac{E_{ox}}{3E_{xc}}\right]^{-1}$$

where E_{yc}, E_{ox} and E_{xc} are constants that are greater than zero. Also for this problem, assume that electron velocity is given by $\mu_n E_y$.

a. Derive $I_D(V_D,V_G)$ and as a function of device parameters and given constants.

b. What is g_m in the limit of small L?

c. Find an expression for I_D if E_{ox} is not constant, but is given by:

$$E_{ox} = \frac{1}{x_{ox}}\left[V_G - V(y) - V_{FB} - 2\left|\phi_f\right|\right]$$

4. Derive an approximate expression for I_D in the triode region that includes the effect of the drain and source series resistance (assume both are equal to R_{SD}) based on the short channel model presented in class.

5. a. Consider the bulk and inversion charge and show that the effective vertical electric field, E_{eff}, can be expressed by:

$$E_{eff} = \frac{V_{GS} + V_{th} + \alpha}{6t_{ox}}$$

b. Let N_A=5×10^{17}cm^{-3} and t_{ox}=4nm in an nMOSFET. Calculate α from part (a) above.

c. Consider a pMOS device with N_D=5×10^{17}cm^{-3} and t_{ox}=4nm. Calculate α (assume p+ poly-Si gate).

6. An nMOSFET with L_{eff}=0.8μm, t_{ox}=15nm and V_{th}=0.7V is biased with V_{GS}-V_{th}=3V and V_{DS}=2V.

a. Using the long channel theory, determine the velocity of the carriers in the channel at both the source and drain. Use μ_o=670cm^{2}V^{-1}s^{-1}.

b. Repeat part (a) above using the short channel model developed in class. Use v_{sat}=8×10^{6}cm/s.

c. Briefly comment on the differences between the results from (a) and (b) above.