PROBLEM SET 5

Issued: Monday, April 9, 2007

Due (at the beginning of class): Monday, April 16, 2007

1. Derive an expression for the current, I_{DD}, drawn from the power supply, V_{DD}, when a CMOS circuit is in a latched condition. Your expression should be in terms of the well and substrate resistors (R_w and R_{sub} respectively) and the parasitic npn and pnp BJT parameters: β_n, V_{BEn}, β_p, and V_{BEp}.

2. Consider the minimum holding voltage to induce latch-up. Suppose that a very low voltage technology (V_{DD}=700mV) is employed to reduce the likelihood of latch-up. Nevertheless suppose latch-up is occurring at an output driver that drives a bond wire inductance of 10nH.

   a. What current must the driver source to achieve the minimum holding voltage if the rise time is 10ps?

   b. The bond wire inductance and voltage rail are fixed. Propose two design changes that will prevent the minimum holding voltage from being achieved, thus eliminating latch-up. Provide quantitative answers for the proposed changes.

3. Assume that an inverter is driving another inverter routed by a wiring length L_w. Let W_p=2μm and W_n=1μm. Use the simple, CV/I model for propagation delay, τ_p. Consider a bulk CMOS technology with C_{JBULK}=1fF/μm (per unit width) and an SOI technology with C_{JSOI}=0.5C_{JBULK} (per unit width). For both technologies, C_{GBODY}=2fF/μm (per unit width) and C_w=0.2fF/μm (per unit length).

   a. Plot, or sketch, the propagation delay, τ_p, of an SOI device normalized to the propagation delay of the bulk device and against wiring length, L_w, from 1μm to 100μm.

   b. In terms of propagation delay, is there a significant advantage to the SOI technology if L_w is large? Briefly and concisely explain your answer.

4. Define t_{po} as the propagation delay for a minimum size inverter driving a minimum size load (i.e. minimum sized load with fan-out of 1). Consider the input load to the 1st inverter to be C_{in}. Now consider N-1 inverters, connected in series after the first minimum size inverter, the last of which drives a load of C_L=$u^N C_{in}$ and all of which are sized by u times the previous stage (i.e. 1, u, u^2, … , u^{N-1}). Derive the fact that the minimum delay for this inverter cascade is achieved by u = e.