

COURSE SYLLABUS

The following comprises a tentative syllabus describing the material to be covered in the course EECS 523, Digital Integrated Circuit Technology, for Winter 2007. Material to be covered for each dated lecture is indicated along with the corresponding reading material. Text material is indicated by the following: W: Wolf, J: Jaeger.

Wk.	Mo.	Day	Material to be Covered	Reading Assignment
1	Jan.	5	Course overview, history of digital integrated circuits	
2		8	Metrics for digital integrated circuits, bipolar digital technology	Handout
		9	MOS digital technology and device structure	Handout
		10	CMOS digital technology and device structure	Handout
3		15	<i>Martin Luther King, Jr. Day: No lecture</i>	
		16	IC fabrication: oxidation, film deposition	J: Ch. 3, 6
		17	IC fabrication: wet etching	J: Ch. 2.2
4		22	IC fabrication: dry etching, ion implantation	J: Ch. 2.2, 5
		23	IC fabrication: diffusion, lithography	J: Ch. 4, 2
		24	Litho. (cont.), performance-setting tech. metrics (CMOS inverters)	
5		29	Typical CMOS process	Handout
		30	Typical CMOS process (cont.)	Handout
		31	Threshold voltage; threshold implant (NMOS)	W: 4.6
6	Feb.	5	Threshold implant (cont.)	W: 5.8
		6	Problems with long-channel MOSFET IV models	W: 5.1, 5.2, Ko Handout
		7	Short-channel MOSFETs: A unified IV model; field-dep. mobility	W: 5.4, Ko Handout
7		12	Velocity saturation modeling (up to onset of saturation)	Ko Handout, W: 5.4
		13	Short-channel model up to onset of saturation	W: 5.4, Ko Handout
		14	MOS device scaling strategies	Ko Handout, W: 5.6, 5.7
8		19	<i>Exam 1: MOS devices and technology</i>	
		20	CMOS inverter using short-channel devices	
		21	Short-channel modeling beyond saturation	Ko Handout, W: 5.4
9			<i>Spring Break: No lectures all week</i>	
10	Mar.	5	Short-channel modeling beyond saturation (cont.)	Ko Handout, W: 5.4
		6	Complete short-channel I-V modeling	
		7	Hot electron effects	Hu Handout, W: 7.3.1, 9.1
11		12	Hot carrier-induced device degradation	Hu Handout, W: 9.3-9.4
		13	Techniques for reducing hot carrier degradation: LDD	Hu Handout, W: 9.6
		14	Other short-channel effects: gate depletion effect	Handout
12		19	Other short-channel effects: series resistance	Handout
		20	Charge-sharing, latch-up introduction	W: 5.2.1.2, Handout
		21	Latch-up continued, methods for alleviating latch-up	Handout
13		26	Basic junction isolation; LOCOS, trench isolation	W: 6.2, 6.5
		27	<i>Exam 2: Short-channel modeling & analysis</i>	
		28	SIMOX and other SOI techniques	Handout
14	Apr.	2	Interconnect processing, damascene, materials, CMP	Handout, J: Chpt. 7
		3	Interconnect parasitics	Handout
		4	CMOS scaling principles	Handout
15		9	Double gated MOSFETs (FinFETs, tri-gate, etc.)	
		10	BIG issues in CMOS scaling; leakage current, oxide	W: 7.5, Handout
		11	BIG issues in CMOS scaling; oxide, 3D integration	Handout
16		16	Review (or make-up lecture)	
		20	<i>Final Examination, Thursday, April 19, 1:30-3:30</i>	