

SEMICONDUCTOR



Radar Scope

Ascenium

Ascenium, first profiled in August 2002, is a seed stage startup founded in August 2000 to develop "a fundamentally new processor architecture that achieves dramatically better performance per mW than conventional DSP architectures." The company has raised \$500k to date and is currently seeking roughly \$1.6M in additional funding. Ascenium has 4 employees.

The Ascenium solution consists of a reconfigurable chip architecture and a compiler that allows standard microprocessor programming languages (C/C++, Java, etc.) to be used without special code modifications common in other reconfigurable and DSP approaches. Large portions of C-code or the equivalent of hundreds of conventional assembly instructions can be replaced by a single Mega-Instruction consisting of several thousand bits compressed into a few hundred bits in memory.

Ascenium's architecture is unlike existing architectures, yet can be programmed optimally in existing high level languages like C.

Hundreds of statically routed fine-grained reconfigurable logic elements build successive "giant" custom instructions logically equivalent to hundreds of RISC instructions. New instructions can be loaded every ten nanoseconds or so, but in many looping cases these instructions are reused because they comprise one or more copies of a loop.

Furthermore, these looping instructions are often split into pipelined stages that deliver computational performance equivalent to hundreds of RISC instructions per clock cycle worth of results. Ascenium is developing a C compiler prototype that will feed this array.

Ascenium plans to initially introduce a processor aimed at the 500mW range of the DSP market that will achieve a 40x improvement over mainstream DSP competitors running the BDTI benchmark suite and 185x improvement over general purpose embedded processors running the SPEC benchmark.

The company plans to offer ICs and given sufficient funding, anticipates that it is two years away from full production of a its first chip and fully optimized tool chain.

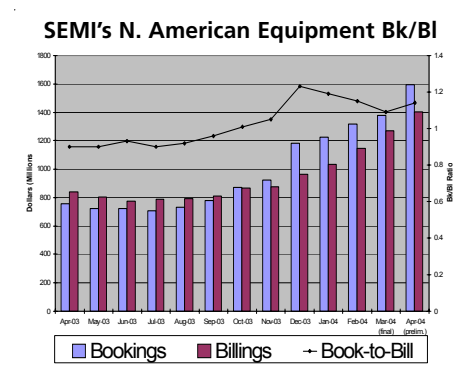
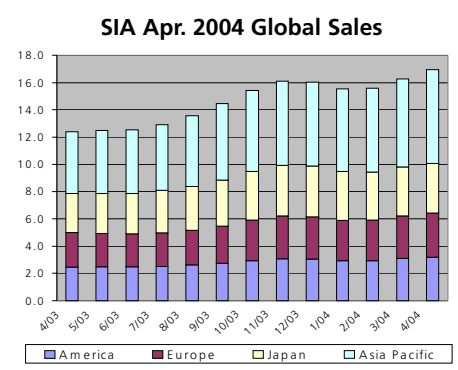
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Blue Pearl Software

Blue Pearl Software was founded in 2004 "to automate the process of RTL Closure for IC and electronic system design." Blue Pearl's initial products are based, in part, on technology developed by Veritable. Blue Pearl owns all rights to the technology. The company has received funding from private investors in the U.S. and Asia, and plans to seek additional capital before the end of 2004. Breakeven is anticipated in Q3'05. The company has 16 employees.

Blue Pearl's RTL Closure software will enable functional design, timing and de-



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sign-for-test (DFT) closure at the register transfer level (RTL). "RTL Closure" involves checking that the design meets its functional, timing and testability requirements so that the RTL can be handed off to the synthesis stage of the design process, eliminating or reducing the need for design iterations from the netlist or physical design stages back to RTL.

Blue Pearl provides ASIC, structured ASIC and FPGA designers with functional design closure by checking complex RTL design and verification issues such as synchronization of data crossing clock domains, initialization, and FSM behavior verification. The technology accelerates timing closure by identifying false paths and automatically generating timing constraints, and provides early DFT closure by identifying testability problems before synthesis.

The current industry solution to design structure and methodology checking is to synthesize RTL down to the logic level and use structural rules. Blue Pearl's technology uses functional rather than structural approaches, operating directly at the RTL level using symbolic simulation, which removes the pessimism of pure structural analysis, resulting in increased performance and accuracy. Blue Pearl also uses predictive analysis techniques without synthesizing to gates, allowing larger designs to be handled.

Implicit design behavior checks include automatic checks that allow users to identify unreachable or "dead code," as well as check for set-reset conflicts, bus conflicts, bus floats, initialization, full case, and parallel case compliance. Blue Pearl also automatically extracts and analyzes finite state machines and identifies unreachable and dead-end states. Blue Pearl's functional design closure

product can also check explicit user specified design behavior.

Blue Pearl's path analysis speeds up timing closure by identifying false and multi-cycle paths without requiring the user to provide stimulus vectors. Blue Pearl also allows users to check that RTL code complies with DFT rules before synthesis.

Blue Pearl argues that while there are companies that offer partial solutions to the problems its addressing, it doesn't have any direct competitors. Blue Pearl operates directly at RTL without synthesizing to logic/gates, and uses a functional rather than structural approach, which improves performance and accuracy and results in higher design capacity. Its functional approach is based on symbolic simulation and relevant state-space exploration, which allows the tool to check both design structure and both implicit and explicit design behavior.

Blue Pearl's DFT closure approach is test-procedure based rather than purely structural, which allows it to check test controller and test mode operation as well as identify DFT and ATPG issues. Lastly, Blue Pearl's timing closure approach uses functional activation rather than static sensitization and thus provides more accurate false timing path reporting than competing approaches.

Blue Pearl's first products are currently in evaluation and will be available in Q3.

Ellis Smith, Founder, President and CEO (previously president and CEO of Orora Design Technologies, TransEDA, Exemplar Logic, and CrossCheck Technology)

Prab Varma, Ph.D., Founder, CTO and VP of Engineering (previously President of Veritable, VP of Product Engineering for Duet Technologies and VP of Engineering at CrossCheck Technology)

Rick Dissly, CFO (previously held CFO positions at Semaphore Communica-

tions, a Xerox company, and Cross-check Technology, among others)

Carol Hallett, VP of WW Sales (previously held sales and marketing positions at Mentor, Icinergy, Tera Systems, TransEDA, and RoyoCAD)

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g2 Microsystems

g2 Microsystems was founded in February 2004 to develop active RFID devices. The company has secured US\$1.3 million in a seed investment round including DB Capital Partners (US\$500,000). The balance of the round was made by the founders of g2 and individual individuals. Series A round of roughly \$8M will be sought in Q4.

A number of the founders and engineers of g2 were previously from Radiata, an Australian startup that was acquired by Cisco in late 2000. The company has 8 employees. G2's chips will be fabricated by either TSMC or ST Micro.

John Gloekler, CEO and President.
Geoff Smith, VP of R&D

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Nannor Technologies

Nannor was founded to provide "Design For Manufacturability (DFM) solutions for IC designs at 130nm and below." The company offers a physical optimization tool for yield improvement, including redundant vias, wire spreading and wire sizing.

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Nascentric

Nascentric was formed to develop "software to electrically analyze CMOS IC designs." Nascentric's products are designed to accurately model the electrical behavior of ICs, with emphasis on the emerging nanometer effects present in 180 μm designs and below. Nascentric recently secured \$5.2 million in first-round funding from Austin Ventures, Silverton Partners and Needham Capital Partners.

Dr. John Croix, Founder and CTO (previously CTO and co-founder of Silicon Metrics)

Dr. Ramon Acosta, VP of Engineering (previously CTO of Fabric Networks, an InfiniBand network solutions company)

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Silicon Construction

Silicon Construction Sweden AB (SiCon), an ASIC design house, has completed a 5 million first round financing to commercialize Irondale III, its analog front-end signal decoder for the flat panel display and projector markets. A syndicate with Swedish investors InnovationsKapital, Creandum, Industriefonden and Scope completed the round.

SiCon was founded in 1982 as an ASIC design house and was acquired in 1998 by Canadian professional video technology supplier Leitch Technology. As an independent subsidiary SiCon started to develop a signal decoder to be combined with Leitch's video controller. In 2002, two of SiCon's original co-founders, Rolf Sundblad, Ph.D., CTO, and Staffan Gustafsson, Ph.D., COO & CFO, acquired SiCon through an MBO.

Irondale III, a 10-bit decoder, is the first application of SiCon's patented Irondale

technology for analog-to-digital conversion and features extremely low power consumption and small die size. Irondale III is initially targeting the high-end market for LCD-TV, plasma screens and projectors. Leading Asian consumer electronics manufacturers have verified the chip on evaluation boards with satisfactory results.

The decoder will initially be sold as a stand-alone chip, but will also be available for IP licensing for SoC integration. Irondale III will be followed by other ADC solutions for other application areas such as 802.11x and UWB.

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Stelar Tools

Stelar Tools was founded in 2003 to develop "EDA products that optimize design and simulation resources for ASIC, SoC and FPGA designers who are creating complex electronic products containing new and existing IP and testbenches." In March 2004, the company secured a seed round of \$1M from SmartForest Ventures, Northwest Technology Ventures, Capybara Ventures, and the founders. The company plans to seek roughly \$3-5M in additional funding in Q4. Stelar Tools has 7 employees.

Design teams currently use simulation and design capture tools to analyze and understand large designs. However, using simulation tools to uncover design, syntax, and connectivity errors is expensive because simulation resources are limited. Schematic/block generation tools are also of limited value in that they only provide a low-level graphical view of the design, preventing designers from seeing the overall design architecture effectively.

Stelar has developed a solution that addresses these issues for the re-design, analysis, re-engineering and management of large, complex designs. Stelar is developing a graphical and textual design analysis environment for large, complex HDL designs, enabling designers to explore, navigate, analyze, document and modify a design within their current design methodology and tools. Stelar's tools provide designers with a dynamic environment for navigating through increasingly complex designs at varying levels of detail and quickly finding and fixing errors.

Stelar's solution will not intrude on the customer's preferred methods and provides the best of navigation, exploration of a complex design, interactive analysis, and engineer friendly documentation. The company expects to introduce its first product, currently in beta, in 6 to 9 months.

Joe Tanous, CEO (Previously the founder of Contour Design, which was acquired by Mentor, and co-founder of OrCAD, which later went public and then was acquired by Cadence. After OrCAD, he became a principal in two venture funds.)

Jack Winter, CFO (previously a managing partner with Arthur Andersen & Co.)

Larry Carner, Co-founder & CTO (previously a software designer and hardware designer at Tektronix, Mentor and Eagle Design Automation, which was acquired by Synopsys, where he stayed for four years)

Steve Sapiro, Co-founder & VP of Marketing (previously held marketing, business development and engineering positions at Intel, CAE Systems, and AMI and has consulted to various EDA companies)

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Startup Profiles

Ashvattha

Ashvattha was founded in November 1999 by the father-son technical team of Guruswami and Kartik Sridharan both to develop highly-integrated, multi-mode RFICs for the wireless and handheld markets. After receiving initial seed funding, Ashvattha began ramping operations in January 2000. In August 2000, Ashvattha secured Series A funding from Comstellar Technologies and Redwood Ventures. In June 2002, Ashvattha raised \$3.25 million in its extended Series A funding led by Crossbow Ventures and including previous Series A investors Comstellar and Redwood. Series B funding was secured in March 2004 from the same investors. The company has raised \$11.5 million to date and is currently seeking roughly \$10 million in addition financing. Breakeven is anticipated in 1H'07. The company has 15 employees.

Multiple independently operating RF systems create headaches for RF system designers such as self-jamming, inter-modulation products, shielding requirements, tighter filtering requirements, etc. Ashvattha's technology eliminates noise and cross-talk problems between separate RF circuits, allowing the integration of multiple systems on a single chip. Its technology is designed to enable the integration of multiple disparate RF front ends on a single chip, with no compromise in the performance of the individual systems implemented.

Ashvattha's Multi Mode Engine (MME) product line is a set of RFICs designed to address the market for multi-mode portable cellular terminals. The Ashvattha MME architecture is claimed to be the only RFIC solution capable of supporting simultaneous operation of multiple modes of radio operation on the same physical chip. Ashvattha's technology is ideally suited for, and is first being applied to, RFICs that support

Cellular, GPS and Bluetooth modes of operation.

Initial silicon, manufactured by IBM using its 0.25u SiGe BiCMOS process, demonstrated all the performance characteristics required to support the company's high-integration product strategy. The test chip included all the key subsystems that will be integrated into the initial product including wireless, GPS, and Bluetooth transmitters and receivers, as well as the unique Ashvattha multi-mode synthesizer and the critical isolation mechanisms that prevent the several on-chip radios from interfering with each other even when operating simultaneously.

Ashvattha recently introduced its first product, the MME2800 multi-mode RFIC that incorporates a Quad-band GSM/GPRS transceiver, Bluetooth transceiver and GPS receiver in a single CMOS device. Ashvattha's isolation technology enables Bluetooth and GPS radio modes to operate simultaneously with the GSM/GPRS cellular radio mode.

The GSM/GPRS, Bluetooth and GPS receive section of the MME2800 includes all required LNA, down conversion, frequency synthesis, baseband filtering, and gain functions. The GSM/GPRS and Bluetooth transmit section includes all required modulation, frequency synthesis and PA driver functions. In addition, the MME2800 incorporates an integrated Bluetooth demodulator, power amplifier and transmit/receive switch. A single external 13 or 26 MHz crystal provides the frequency reference for the device.

The MME2800 is targeted at global markets for GSM and UMTS cellular handsets. In both applications, the MME2800 (with 3rd party WCDMA RFIC for UMTS terminals), provides handset manufacturers with IC solutions that are best in class in terms of size, cost and power consumption, according to the company.

The competition is comprised of collective solutions based on single mode GSM, GPS and Bluetooth RFICs. Ashvattha argues that its solution is less expensive, smaller, consumes less power, and is easier to integrate than solutions that use multiple single mode chips. The chip is also very competitive against multi-mode chips from other startups because Ashvattha claims to offer the only device that is capable of simultaneous multi-mode operation (2 or more RF modes at same time).

Samples of the GSM/GPS/Bluetooth RFIC are scheduled for Q3'04 with production starting in Q2/Q3 2005. The device is fabricated by TSMC on a low voltage 0.18u RF CMOS process. Follow-on products will include EDGE, WCDMA, WLAN and TV Tuner modes.

James Kamke, CEO (previously VP of Business Development at Sequoia Communications and VP of Product Marketing at PrairieComm)

Guruswami Sridharan, CTO and Chairman (previously held senior positions in both the circuits and systems areas at Rockwell/Conexant)

Kartik Sridharan, VP of Engineering (previously worked on next generation WLAN systems at Philips)

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Chelsio

Chelsio Communications was formed in 2001 "to provide high-speed protocol-offload products to manufacturers of server, storage, and data-communications equipment." In 2001, Chelsio received \$11M in Series A funding, led by Sequoia. In 2002, NEA led a \$19M Series B round. Other investors include Global Catalyst Partners, Horizon Ventures, and Pacesetter Capital. The company will seek additional capital later this year. Chelsio has 40 employees.

Chelsio is developing protocol acceleration technology. Featuring a highly scalable architecture, Chelsio has begun sampling its 10-Gigabit Ethernet adapter card with TCP offload engine in hardware, which delivers the low latency and superior throughput required for high-performance computing applications.

Chelsio's 10-Gigabit Ethernet host-bus adapter technology recently broke through the 10~s latency barrier for 10-Gigabit Ethernet. Chelsio claims to be the first 10G Ethernet adapter vendor delivering a TCP offload engine (TOE) in silicon and the first to deliver 10G iSCSI in silicon.

In a recent demo, Chelsio's solution was shown transmitting standard 1500-Byte Ethernet frames in a peer-to-peer configuration at 7.8Gb throughput with less than 10~s latency from user to user and 50% CPU utilization with a 2.2GHz Opteron. The line-rate performance of the adapter stays consistent with equal and stable bandwidth per connection, whether there is one or 10,000 connections.

According to Chelsio, the best performance other 10GE adapters on the market can claim in transferring standard Ethernet frames is only 3 to 4Gbps, with higher latency and more than 100% CPU utilization in multi-Itanium-II processor systems. Chelsio's 10G Ethernet adapter card simultaneously achieves high throughput, low latency and low CPU utilization – all while using the TCP/IP protocol suite with standard 1500-byte packets.

The T110 host bus adapter card is built with Chelsio's Terminator ASIC, a deeply-pipelined VLIW architecture that delivers high-bandwidth and low-latency advantages over RISC-based multi-processor implementations. It is claimed to be the first chip on the market to include a 10G TOE. The chip is fabricated by TSMC on a 0.13u CMOS process.

The Terminator ASIC has a capacity of one million sessions, while the T110 card can support up to 64,000 connections.

The T110 & Terminator include pre-standard RDMA RDMA functionality and the product roadmap will include RDMA on chip. For low numbers of connections, Chelsio believes RDMA is not required to achieve low latency. For a lot of connections, RDMA will be required.

The T110 board is sampling now and is priced at \$4,900 each in small quantities. Chelsio is an HBA company; however, if the opportunity for technology licensing of the Terminator chip makes sense, the company will do that as well.

Gartner estimates the total available market for 10G NICs in 2007 to be somewhere between \$1.5B and \$2B. The company will formerly introduce its products, roadmap and customers in September. Chelsio already has unnamed tier one OEM customers.

Competitors include Alacritech, NetEffect, Ammasso, Intel, and S2io. Competitive advantages include its ASIC development capability and the first claimed 10G TOE and iSCSI in silicon.

Kianoosh Naghshineh, Founder, CEO and President (previously CEO and president of IP firm ASIC Designers)

Dr. Ásgeir Eiriksson, CTO (previously responsible for protocol design, ASIC chip design and implementation, and formal design methodology at Silicon Graphics)

Robert Miller, VP of Operations (previously VP of Operations for the Storage Solutions Group at Quantum)

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Enpirion

A group of technologists from Bell Labs formed Enpirion in November 2001 to develop power systems on a chip. Enpirion has secured \$8 million in Series A funding led by Canaan Partners (\$7M) and including Silicon Alley Seed Investors (\$1M). A Series B funding round is expected to close by the end of Q2. The company currently has 24 employees.

Enpirion's mission is "to be the premier provider of Power Systems on a Chip for point of load and dynamic power management applications." Its PSOC technology provides the performance of a high efficiency switching DC-to-DC converter with the size and simplicity normally associated with a linear regulator. The fully integrated power management system reduces footprint and component count by 60% - 70%, simplifies power system design, and provides higher power efficiency than existing solutions – all at competitive pricing to existing BOMs.

The company has an extensive IP portfolio including 19 patents and 8 more pending. The patents cover a proprietary power FET allowing 10X increase in DC-DC switching speed & full control integration, integrated magnetics & process technology, and digital control and algorithms. Enpirion's Dynamic Power Management technology can more than double battery life in mobile applications.

Enpirion's Power FETs feature superior transient response and are 5x to 10x faster than existing devices, according to the company. The devices also have much smaller L&C requirements and can be packaged in the same die as the controller. Integrated power inductors replace costly and bulky discrete components.

The patented DPM digital control algorithm provides an order of magnitude faster response time and power saving

Startup Profiles

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due to the rapid handling of voltage and frequency scaling. The algorithm is also optimized for maximum slew rate control. The company's modules are built in DSM CMOS providing low cost and multiple foundry sources.

The company plans to offer two product families: iPOWER PSOCs are designed for point of load (POL) applications such as servers, desktop PCs, and printers. Samples with an integrated inductor were delivered in Q1. miPOWER PSOCs are designed for mobile applications such as PDAs, notebook PCs, and cellphones. First samples are anticipated in Q3 with production in Q1'05.

Enpirion recently introduced the EN5330, which is claimed to be the smallest Power System on a Chip (PSoC) and fastest synchronous buck converter. The EN5330 is the first of the iPOWER line of integrated DC-to-DC converters for use in Point of Load (POL) applications including servers, PCs, laser printers, set-top boxes, and telecom and datacom equipment.

Enpirion's patented approach capitalizes on semiconductor geometry advances that enable a 10x switching-frequency improvement, integrating a PWM controller, output FETs and magnetic components into a single IC package with a standard TSSOP footprint. The EN5330 features an integrated inductor and reduces real-estate requirements and part count by more than half, while slashing development costs and time-to-market. Very high switching frequencies reduce the amount of input and output capacitance required while at the same time offering an order of magnitude improvement in transient response.

In some applications, the power section can take up a third or in some cases up to half of the board space. With

iPOWER, OEMs can potentially reduce that fraction by 50% to 60%. Including the minimum of three external components, the entire DC-to-DC converter can be placed in as little as 135 mm² of single-sided or 102 mm² of double-sided board space.

Operation from common voltage rails of 2.5V, 3.3V and 5V is achieved with a wide input voltage range from 2.375V to 6.5V. With up to 3A or 10W of output power, and 90% efficiency, the output voltage is pin selectable with options for seven standard voltages (0.8V to 3.3V) and a resistor divider setting enabling a continuous set-point range from 0.8V to V_{IN} .

The EN5330 can be used in a sequenced start-up with a programmable soft-start time and a separate enable function. Full protection functionality is offered with over-current, short-circuit, over-voltage, under-voltage and thermal shutdown features. Other features include 5MHz operation, V_{out} accuracy of 3% (1% trimmed), and superior noise immunity between controller and power circuits.

The EN5330 is available now. Future plans include a 20W/6A version and a 1.8V and 12V platform development

miPOWER plans include DC/DC converters with input range from 2V to 6V, output range from 3.3V to 0.8V, high efficiency, dynamic power management, multiple LDOs, integrated inductors and several other features.

EN5330 competitors include Linear Tech, Maxim, Intersil, and Power-One, among others. Enpirion has the only device with an integrated inductor. Its device requires the fewest number of external components and has the highest frequency of operation. Lastly, its solution has the lowest profile and smallest area.

Mark Downing, CEO (previously VP of Mktg. for Micrel and Pericom)

Ashraf Lotfi, Ph.D., Founder, President & CTO (previously led the power management R&D effort at Bell Labs as Director of Power Management Research)

William Troutman, Ph.D., Founder and Chief Strategy Officer (previously Strategy Dir., Power Mgmt Products at Bell Labs)

Kevin Chynoweth, VP of Operations (most recently Director of Strategy for Global Operations at Agere)

Jian Tan, Ph.D., Founder and Technology Director (previously a principle investigator and expert in power semis at Bell Labs)

Trifon Liakopolous, Ph.D., Founder and Technology Director (previously a researcher in MEMS tech development at Bell Labs)

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FishTail D.A.

FishTail Design Automation was founded in 2002 to "tackle the difficult problem of precise constraints on chip timing – the area where the success or failure of a design is ultimately determined." FishTail has received funding from private investors and Magma Design Automation. FishTail is currently working with Magma and other EDA vendors to tightly integrate Focus into their design flows.

False paths and multi-cycle paths are large problems when trying to reach timing closure. Chip design teams today rarely specify such timing exceptions at the start of the chip implementation flow. Instead, these constraints are added piecemeal, late in the design cycle, adding time, uncertainty and risk.

FishTail solves this problem with its Focus product, which takes synthesizable RTL and clock definitions and auto-generates false and multi-cycle

paths for a chip. With “golden” timing constraints in place at the start of the chip implementation flow, design teams can implement higher quality chips with greater confidence in less time. Focus identifies false and multi-cycle paths early in the design cycle – before virtual prototyping and logic synthesis. By using Focus to freeze golden timing requirements early in the design cycle, users eliminate costly iterations to add timing exceptions when synthesis or place and route results do not meet requirements.

Focus is based on extensions to the Ph.D. dissertation work originally done at The University of Michigan by founder and CEO Ajay Daga. The unique technical innovation is the ability to analyze the intended functionality of the chip based on its high-level, synthesizable description and then determine the false and multi-cycle paths without user-specified stimulus.

Focus starts with the fundamental performance requirement for a chip, i.e. its clock specifications and the synthesizable description of the design. Focus then analyzes the intended functionality of the chip in the context of how it will be clocked, and determines the golden timing constraints that must be obeyed for a chip to run at its intended clock speed.

These automatically identified false and multi-cycle paths are written out in standard Synopsys Design Constraint (SDC) format, along with the clock specifications for the design. Focus generated constraint files can then be used to drive virtual prototyping, logic synthesis, and place & route tools. With golden timing constraints in place early in the design flow, chip implementation tools are empowered to generate low cost, low power chips without extra design iterations.

Focus is applicable to any digital ASIC or FPGA design and can be used to both generate full-chip constraints and

block-level implementation constraints. Focus can analyze multi-million gate designs in a matter of hours and is applicable for both flat and hierarchical design flows.

FishTail also offers the Golden Timing Constraints Service for designers who would like to obtain the benefits of automatically generated timing constraints without licensing the Focus software.

Toshiba’s System LSI Division in Kawasaki, Japan has purchased FishTail Focus for use in its System LSI chip-implementation projects. Toshiba continually run into problems with incomplete timing constraints during chip-implementation. Prior to Focus, the company had to manually sift through timing reports and establish whether timing problems were real – a tedious, error-prone and time consuming task, taking several weeks.

By deploying Focus, Toshiba expects to be able to significantly reduce the time spent during timing closure. In addition to the productivity improvements, on a 300K gate design, Toshiba also saw a 7% reduction in random-logic area through the use of Focus.

Ajay Daga, Ph.D., Founder & CEO (previously Senior R&D Manager for hierarchical static timing analysis in the PrimeTime team at Synopsys)

Barry Lazow, Sales Director (previously held Western Area Sales Director positions at Provis and Denali Software)

Larry Willeman, CFO (previously held a variety of financial positions including Business Unit Controller at Mentor and held CFO and Controller roles with several early stage companies such as Isite Design and Fluence Technology)

Lukas van Ginneken, Ph.D., Technical Advisor (a co-founder and Chief Scientist at Magma Design Automation)

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IPextreme

IPextreme was founded in January 2004 to develop semiconductor IP based on a new methodology for developing and packaging IP products.

Conventional wisdom says that IP quality is a verification problem, with improved verification technology solving the problem. Yet, IPextreme believes that IP quality is a design problem, with the goal being fewer bugs in the code. Better engineering, not better technology, is the solution to the quality problem. To address this paradigm, IPextreme claims to be the first vendor to apply Extreme Programming (XP) to IP development for quality and reliability.

Extreme Programming is a deliberate and disciplined approach to design with a relentless focus on creating the best quality source code, emphasizing simplicity and customer involvement in the design process and employing techniques such as pair programming and continuous integration to eliminate bugs as early as possible in development. XP is based on twelve practices: the planning process, frequent small releases, system metaphor, simple design, test driven development, refactoring, pair programming, collective code ownership, continuous integration, 40 hours week, on-site customer, and coding standard.

Developers work together along with a lead customer who provides ongoing feedback and is an integral member of the team. The team starts with the simplest design that could possibly work and builds the final product from that stable base through small, frequent releases, code refactoring (restructuring and rewriting), and continuous integrations that often occur several times a day.

Startup Profiles

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All new code is written in pairs – two engineers, one keyboard. IPextreme has also “instrumented” its design groups such that the company can measure the teams’ performance in a quantitative and unbiased way so as to improve its methodology and efficiency.

Often, IP packaging is a confusing mixture of code, scripts, and tools, and may be biased towards supporting a specific vendor’s EDA tools. IPextreme has developed a new lightweight technology for packaging IP that is based on the familiar metaphor of a datasheet, which contains all the descriptions and diagrams one would expect from a datasheet, but in reality, is the cockpit by which users interact with the IP.

The interactive datasheet contains all of the information and scripts necessary for customers to integrate the IP. Customers change configuration parameters or modify timing information by updating fields on the interactive datasheet. When printed, it appears as a normal datasheet, and is used as a record of the modifications. IPextreme’s packaging technology is EDA vendor neutral and supports the new industry standards from the SPIRIT Consortium.

The company’s core focus is IP and IP-related services in wireless communication and embedded systems design, including wireless (802.11, 802.16, Bluetooth, GPS, UWB), microprocessors and DSP.

Nexus Partner Products are silicon-proven products developed by IPextreme partners and packaged with its lightweight IP packaging technology. The Nexus program provides a channel by which semiconductor companies can exploit their IP for maximum commercial value. IPextreme “refurbishes” their IP to bring it up to usability standards and packages it for sale. IPex-

treme sells, maintains and provides first line technical support to end customers.

Infineon is the first Nexus partner, and will offer its C166 16-bit microcontroller and TriCore 32-bit MCU-DSP cores for licensing through IPextreme. Infineon expects the cores to be available from IPextreme by Q3’04.

IPextreme is also developing proprietary “IP titles” for embedded systems applications using Extreme Programming practices to virtually eliminate bugs before the product reaches customers. Lastly, IPextreme provides design services, IP services, and methodology services.

Warren Savage, Founder, President & CEO (previously created and ran the Star IP Program at Synopsys and head of the Synopsys DesignWare engineering organization)

Michael Chapman, CTO (Most recently Director of Engineering at Synopsys heading development activities associated with its wireless IP products. Before that, he was VP of Engineering at a network processor startup in Paris)

Paul Giordano, VP of Sales (previously held VP of sales and marketing positions at ArsDigita, RealCommunities, AppNet and Angeles Design Systems, and has 16 years of EDA sales and marketing experience at Valid Logic/Cadence, Mentor and Quickturn)

Michael Cizl, Director, Munich Design Center (most recently R&D manager, heading the development of a Bluetooth baseband controller IP core at Synopsys)

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Lighthouse D.A.

Lighthouse Design Automation was formed in 2004 “with the intent to automate the verification process for customers by commercializing robust production-worthy software products and verification IP that have resulted from initial research at Silicon Forest Research.” Lighthouse DA has raised roughly \$1M from angel investors, including some veterans in the EDA industry, and is currently seeking additional investment. Breakeven is anticipated in toward the end of 2005. The company currently has seven employees.

Lighthouse DA has developed inFact, an intelligent dynamic verification series of tools that automate testbench sequence generation for the simulation of RTL designs. Lighthouse DA believes its inFact series of tools finds design bugs faster than existing verification tools can, and finds bugs that existing verification tools cannot find at all. The result is a higher degree of confidence in higher quality designs, in much less time. inFact also enables verification engineers to achieve higher coverage.

inFact is based on patent-pending technology that combines the best attributes of formal verification and functional simulation. inFact compiles a design’s specifications into executable generators that adaptively construct sequences of transactions during simulation. The result is a high-coverage testbench that requires less time to develop, detects design bugs in less simulation cycles, and covers more of a design’s functionality.

Lighthouse DA argues that inFact software products improve verification productivity by a factor of 10X or more. And, inFact’s verification IP and model libraries reduce verification time and cost even further.

inFact intelligent Compiler (iComp) compiles a user's specification that describes a design's behavior, and then synthesizes intelligent Sequence Generators in the form of native-compiled code executables. Using basic constructs in standard C++, a verification engineer can create iSpec, the input to iComp from a design's specification and its interface protocols.

Unlike other testbench tools, iComp does not require the verification engineer to write each of the sequences to be tested. Instead, using implication technology, inFact automatically generates more unique sequences, faster than any other alternative tool or methodology.

inFact's standard C++ input descriptions are easy to write and do not require learning a new custom language. inFact requires far less input from the verification engineer, the format is simpler, and the language is an industry standard.

inFact intelligent Sequence Generators (iGen) are compact native-compiled code executables that automatically generate unique sequences of transactions during simulation runtime. iGen's only generate legal sequences, eliminating the time-consuming task of wading through reams of testbench data to find and remove illegal transactions. Multiple iGen's can run in parallel, automatically generating complex verification scenarios that detect design bugs only elicited by subtle interactions between multiple subsystems in a design.

For specifications and interfaces unique to their designs, verification engineers can create iGen's by using the inFact Compiler. For many common industry standard interfaces and protocols, verification engineers can purchase pre-synthesized iGen's from Lighthouse.

inFact intelligent Synchronizer (iSync) manages the execution and interaction between a Verilog simulator and one or

more inFact intelligent Sequence Generators during simulation. Unlike other testbench tools, iSync utilizes only the fastest and most widely supported PLI routines, which enables inFact testbench sequences to be created with negligible impact on simulation performance.

When multiple inFact iSG's are generating verification sequences in parallel, iSync keeps track of all of the design's resources, making sure they are allocated and shared properly between interfaces. If the design hardware is programmable, inFact interweaves firmware instructions to configure the hardware prior to generating hardware verification sequences.

Lighthouse DA is initially targeting several segments that fall within the IC design verification market, including testbench generation for software-based simulators, hardware-based emulators, and hardware-software co-simulation. Industry analysts estimate these markets to exceed \$300M in potential annual revenue. Lighthouse DA is also initially targeting companies that have problems bridging the gap between module level verification and system level verification.

By combining attributes of formal verification and functional simulation, inFact provides between 10X to 100X improvement in verification productivity compared to existing products on the market, according to the company. Describing a design's specification with inFact requires less than one-fifth the amount of code required by existing products. inFact requires less than one-fourth as many simulation cycles to cover the same amount of design functionality as competing solutions. Since inFact tracks constructed sequences, inFact is the only toolset that can provide a functional coverage report of transactions covered during simulation.

inFact production releases were first shipped to customers in Q1'03. Current customers include SanDisk, Fujitsu, Hitachi, and Mentor. Several other companies are currently evaluating inFact.

Clifton Lyons, President, CEO & Co-Founder (previously Director of Engineering at Mentor Graphics and a founder of Performance CAD, which was acquired by Mentor)

Sudhir Kulkarni, CTO and Co-Founder (previously led the engineering team that produced Verilog-XL at Cadence and led Monet and QuickFaultII engineering teams at Mentor)

Mark Olen, VP of Worldwide Sales and Marketing (most recently VP and GM of Cascade Microtech's Pyramid Probe Division)

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Microbridge

Microbridge Technologies was formed in 1999 as a spin-out from Concordia University as "a product and technology licensing company specializing in micro-systems technology for electronics, micro-devices and sensor-based systems." Initially the company was working on MEMS-based mass flow meters; however, the focus shifted to electrical trimming in late 2003.

In December 2003, Microbridge closed the second tranche of its seed equity financing, raising a total of \$2.65 million CDN in venture capital. The Fonds de solidarité FTQ and Innovatech Montréal were the major investors. The company is currently seeking \$5M US in additional capital. Breakeven is anticipated in 2005/6. The company has 8 employees.

Microbridge uses micro-thermal devices based on conventional silicon IC technology to create electronically adjustable resistive micro-devices. The

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Rejutor, Microbridge's flagship product, is an electronically precision-adjustable passive micro-resistor device for in-circuit automation of resistive 'trimming.' The Rejutor is non-volatile and re-adjustable many times, bi-directionally, to very high precision, using only electrical signals.

Rejutor devices are based on standard semiconductor (e.g. CMOS, BiCMOS) and MEMS processing capabilities and stem from the common technology platform of micro-thermal devices using suspended microstructures. In general, these devices consist of a micro membrane (or membranes) suspended over a cavity etched in the silicon substrate. An electrical micro-heater is fabricated on the membrane using a conductive, heat-dissipating layer, typically polysilicon.

By suspending the micro-heater over an air cavity, the microstructure attains high thermal isolation, allowing the device to reach very high temperatures, such as 800°C - 1000°C, at very low power while leaving the surrounding circuitry undisturbed. The cavity provides thermal isolation, eliminating the risk of thermal damage, allowing many adjustable resistors on a single chip, facilitating low voltage and power to trim (3-10V and ~2mA), and providing fast cycling.

Because the devices are so small, they have very low thermal inertia. In combination with the high thermal isolation, this enables very rapid heating without significantly heating the integrated circuitry residing around the outside of the cavity. This heating changes the resistive property of the poly resistive element. Rejutors can feature a resistance range of 500 ohms to several Mohms, bi-directional adjustment over a 30% range, and 0.01% to 0.001% resistance matching and adjustment resolution.

The devices can achieve over 5,000 adjustment cycles.

Microbridge has developed a hardware-and-software technique for high-precision adjustability (to within 5-20 parts per million or better) of the electrically resistive elements in the suspended microstructure. The trimming algorithms and techniques can be performed by typical production test equipment at wafer probe, final packaged test, and/or during in-circuit board level testing, or with custom designed calibration circuitry during system level calibration or production system test.

The ability to perform high precision trimming raises the issue of Temperature Coefficient of Resistance (TCR) problems, which may not be important at lower precision levels. According to Microbridge, at present the TCR of a material is widely viewed as a given, and never trimmed at the level of an individual device. There has been no practical, cost-effective means to even measure the TCR of an individual component, let alone trim it. Microbridge's eTCR technology not only electronically adjusts resistance to high precision, but can also measure the RTCR of pairs of resistors and electronically adjust the TCR to high precision.

Rejutor and eTCR innovations include techniques for designing adjustable resistors to reside on thermally-isolated membranes suspended over micro-machined cavities, applying electrical trimming signals to accomplish high-precision trimming, designing pairs of adjustable resistors such that their RTCR can be measured, and simultaneously manipulating both the resistance and TCR to independent settings. The combined techniques enable these resistors to be adjusted using very low power (a few mA at 3-12V), without affecting surrounding circuitry, while maintaining stability during operation.

The resistance adjustment and TCR matching is accomplished at IC compatible low voltages and currents. Trimming of Rejutor is presently performed with the use of conventional multi-channel ADC/DAC acquisition equipment and an adaptive algorithm run from a PC-based software package. Specialized software allows flexibility and adapting the trimming technology to a variety of practical applications and manufacturing technologies.

Rejutors can also be temperature coefficient matched with other Rejutors using only electrical signals. Pairs of Rejutors can be resistance matched to typically better than 0.005% and their Temperature Coefficient of Resistance can be adjusted to match another Rejutor to better than 2 ppm/oK, or intentionally adjusted to a precise mismatch in TCR to help temperature compensate electronic circuitry.

The company offers Dual and Quad Rejutors, Application Specific Rejutor Networks, and a Rejutor Trim evaluation kit, designed to assist the user in becoming familiar with Microbridge's Rejutor technology and to permit the user to perform repeated, precision electrical trimming of Rejutors. The Rejutors in the kit come in DIP packages. Each package has one or more Rejutor pairs, which may be used for single resistor trimming, bridge-balance trimming and TCR matching. X-FAB is the foundry partner for the initial manufacturing of the Rejutor.

The company is broadening the range of values available and is working on various schemes to push up the power dissipation to 30mW or even 50mW. The company is also moving towards a chip-scale package (e.g. micro BGA). Lastly, Microbridge is developing discrete components in hermetic packages for the electro-optic field and is investigating opportunities in the sensor market.

The company's long term strategy is to license the technology to semiconductor companies. Rejutors are CMOS and BiCMOS process compatible, thus they can be incorporated into analog, mixed-signal and SoC designs. Rejutors are particularly interesting for RF applications as passive adjustable resistors with low capacitance and excellent high-frequency performance.

Other trimming techniques, such as manual trim pots, laser trimming, electrically-fuseable arrays, and digital pots have many limitations such as high cost, unidirectional trim, drift, and lack of precision. According to Microbridge, a large percentage of laser trimming, both at wafer and thick-film, can be replaced with the Rejutor. The company is focusing on areas where digital trimming is not optimum because of high precision, high frequency, or low power requirements. The Rejutor can also improve device performance, for example a precision voltage reference's temperature performance can be improved significantly by hanging a couple of Rejutors on it.

A large corporation in Japan has purchased the eval. kit. Microbridge has also engaged in high level discussions with several large semiconductor companies and has at least one project materializing.

Michael Foster, President and CEO (previously president and CEO of Symagery Microsystems and COO of Chrysalis-ITS)

Dr. Les Landsberger, CTO, Founder (Concordia Research Chair, heading the Microelectronics Fabrication activities in the Department of Electrical and Computer Engineering, Concordia University)

Dr. J. David Cheeke, VP of Operations, Founder (Chairperson Physics Department, Concordia University, 1992 to 2000)

Dr. Oleg Grudin, VP of R&D, Founder (15+ years experience in advanced

technological R&D in Ukraine and 10+ years R&D and experience in micro-thermal devices)

Nick Tasker, VP of Business Development (previously formerly Strategic Marketing Manager of Dalsa Semiconductor, President and EVP of Marketing and Sales of Goal Semiconductor, and Founder and President of Task Microelectronics)

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NetEffect

Banderacom, a 10Gb InfiniBand chip startup, has been restructured as NetEffect "to develop silicon to enable the next generation of high-performance, multi-gigabit Ethernet." NetEffect has secured \$22 million in Series A financing led by TL Ventures and joined by new investors Granite Ventures, TI Ventures and Duchossois Technology Partners, along with existing investors Austin Ventures, JatoTech Ventures and Infinity Capital. NetEffect has 25 employees, including eighteen former Banderacom employees.

Senior members of the technical staff at Jato Technologies, a networking chip startup that was acquired by Intel, founded Banderacom was in November 1999 to develop InfiniBand chips. Banderacom had raised \$9M in Series A funding from Austin Ventures, JatoTech and Intel, and Series B funding of \$35M in June 2001 from Infinity, Trinity, and Qlogic. In late 2002, the decision was made to suspend InfiniBand chip development efforts to focus on the emerging TOE/RDMA Ethernet NIC market. NetEffect retained Banderacom's VP of Engineering, as well as the architects and designers who brought Banderacom's 10G chips to production. NetEffect has a proven silicon team and will re-use Banderacom's IP and architectures.

According to NetEffect, data center servers will require 10Gb connectivity by 2006. However, realizing 10Gb and even multiple Gb performance requires the elimination of overhead caused by TCP/IP processing, intermediate buffer copying and application context switches. The migration from 100Mb to 1Gb increased server overhead 10x, resulting in unacceptable levels of server CPU processing and memory bandwidth consumption. And the migrating to 10Gb will increase server overhead 10x yet again.

NetEffect lab test data indicates that 40% of CPU overhead results from transport processing, 20% from intermediate buffer copying, and 40% from application context switches. Transport Offload Engines (TOE) move transport processor cycles to the NIC, and move TCP/IP protocol stack buffer copies from system memory to the NIC memory. RDMA/DDP eliminates intermediate and application buffer copies, reducing memory bandwidth consumption. And Kernel bypass (direct user-level access to hardware) reduces application context switches. A TOE-enabled, iWARP-enabled networking stack would eliminate transport overhead, buffer copies, and context switches.

NetEffect ICs "allow Ethernet to easily scale to meet data center demands, using next-generation iWARP RDMA Ethernet that is fully compatible with the Ethernet infrastructure found in today's data centers." Today's servers require multiple adapters to connect to Storage, Network, and Cluster Fabrics. iWARP, which is compatible with today's Ethernet infrastructure, virtually eliminates networking overhead, enabling the delivery of multi-gigabit Ethernet and convergence of data center traffic for networking, storage, and clustering over a single network technology.

Servers with the NetEffect iNIC deliver optimized file and block storage, net-

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working, and clustering from a single adapter. IT managers can support all data center fabrics with just Ethernet. For blade servers, the iNIC reduces I/O real estate, power, cost, and SKU options while delivering increased flexibility.

Competitors include Alacritech, Chelsio, Ammasso, Intel and S2io. Neteffect believes that its patented virtual pipeline architecture, which reduces latency, provides it with a distinct competitive advantage. The company plans to have first silicon later this year and is currently choosing a foundry partner.

Rick Maule, CEO, President & Chairman (previously VP and GM of the Mobile Communications Division of 3Com)

Terry Hulett, VP of Engineering (previously VP of engineering at Banderacom)

Rob Senders, CFO (previously CFO for Banderacom and VP of finance for Compaq's Industry Standard Servers Group)

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www.rdmaconsortium.org

Sierra D.A.

Sierra Design Automation was founded in January 2003 to "provide the highest productivity IC implementation system solutions to the semiconductor industry."

According to Sierra Design, IC implementation tool capacity for overnight closure has stagnated, resulting in delayed schedules and higher design resource costs. In current generation implementation tools, physical synthe-

sis is the biggest capacity bottleneck. Existing physical synthesis approaches rely on computationally expensive techniques, such as iterative improvement and brute-force trial-based optimization.

In addition, traditional physical prototyping approaches are inaccurate because their product architectures are decoupled from the final implementation systems. This results in misrelated timing analysis, congestion analysis and an inability to predict the final performance after implementation.

Pinnacle, Sierra's flagship product, is claimed to be the first IC implementation solution developed specifically to meet the high capacity, short turnaround time and quality of results (QoR) demands of large designs targeted at manufacturing processes of 90 nanometer and below.

Pinnacle's physical synthesis technology and architecture speeds design closure by 5x to 10x over last-generation tools, according to the company, slashing turnaround time from days to hours. Pinnacle's open architecture and ultra-compact database can optimize 10 million gates flat (chips or blocks) on a 32-bit machine in an overnight runtime and scales to 50+ million gate hierarchical designs on a 64-bit machine.

Pinnacle claims that its ultra-compact database has the industry's highest capacity and the smallest memory footprint, which enables both prototyping and implementation to be performed in the same unified environment. Implementation engines are directly used during prototyping, resulting in very high correlation between the two steps.

Pinnacle's shorter turnaround time is due to new technological advances in the area of performance bottleneck detection and analytical optimization.

Pinnacle also addresses the challenge of constraint validation for "dirty" de-

sign data using its physical synthesis technology, which works in the presence of ill-formed constraints. In addition, for nanometer design variability, Pinnacle enables designers to simultaneously analyze and optimize multiple design corners and modes, eliminating weeks or months of iteration around different variability scenarios.

Pinnacle seamlessly integrates in customer's existing flows. It has built-in global and trial routing technology and has demonstrated excellent correlation with routing tools at multiple customers. The built-in static timing analysis engine has demonstrated very good correlation with sign-off timing analysis tools and its delay calculation technology has also been correlated closely with SPICE.

Prices begin at \$395K for a one year license.

Fujitsu is incorporating Pinnacle's physical design system into its IC implementation flow and is analyzing Pinnacle's architecture for use with AccelArray, Fujitsu's new ASIC design platform.

Toshiba is interested in integrating Sierra's Pinnacle into its existing flows for its SoC design productivity improvement. The run time of Sierra's Pinnacle system was under 12 hours for placement and optimization on Toshiba's 6 million gate design, utilizing a flat physical design flow on a 32-bit Linux machine.

Pravin Madhani, Founder, President and CEO (previously co-founder, president & CEO of Everest Design Automation, which was acquired by Synopsys)

Shankar Krishnamoorthy, Founder, CTO and VP of Engineering (previously at the helm of the Physical Synthesis R&D organization at Synopsys)

Rusty Ingram, VP of Sales (previously VP of Sales at Plato Design Systems,

which was acquired by Cadence in 2002)

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SiVerta

SiVerta was formed in November 2002 "to be the premier supplier of high performance, competitively priced, RF MEMS components to the wireless industry." The company is self-funded and is currently seeking roughly \$5 million. The company has 4 employees.

Companies like Teravicta, Magfusion, XCOM Wireless and WiSpry are developing RF MEMS switches, which promise to offer substantial improvements over semiconductor solutions in the areas of signal loss, isolation, signal purity, and design simplicity. Unfortunately, these hopes have often been frustrated by the challenges associated with MEMS technology, which has limited the company's ability to secure funding.

SiVerta claims to have broken this impasse by delivering all the benefits expected of a RF MEMS switch in a package that is manufacturable in high volumes, can be handled by standard assembly equipment, and brings a highly competitive cost structure with the current solid-state industry. SiVerta technology also provides superior reliability and performance.

SiVerta has developed a patent-pending manufacturing process that substantially decreases the cost structure of RF MEMS, bringing component costs in line with or below the costs of building products with current semiconductor components. SiVerta devices do not require the cost and size constraints of an external hermetic package. The company has successfully proven that their

wafer level sealing process works with an RF MEMS device.

The SiVerta RF MEMS wafer was placed through a standard dicing/sawing process proving that finished wafers can be handled like normal semiconductor wafers. SiVerta believes these are the only RF MEMS switches that have ever been put through standard dicing/swing processes.

SiVerta's RF MEMS switch design increases battery life due to low power requirements and very low insertion loss. The company plans to offer single and multi throw devices with the same very low insertion loss and high isolation properties (<0.2dB insertion loss & >50dB isolation). The devices cover a very wide bandwidth, extend base station coverage, reduce dropped calls, and reduce design criteria for board space and number of components

Current samples are showing excellent performance for "proof of concept devices" and potential customer reaction has been very good. The company's initial target market is a multi-throw antenna switch for multiband or multimode cellular handsets and multi-band WLANs systems.

Gary Pashby, Founder, President & CEO (17 Years of MEMS experience; delivered high volume automotive MEMS products)

Tim Slater, Founder, VP of Engineering & CTO (Co-founder and Principal Scientist at Xros, which was acquired by Nortel)

Glenn Gottlieb, Business Development

Greg Reznick, Director & Executive Consultant (most Recently president and CEO Of Xros)

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People

AMCC has appointed **Brian Wilkie**, former VP and GM of the PowerPC business unit at Motorola, as VP and GM, Embedded Products group. AMCC has also created its Austin Design Center, which will play a key role in the company's overall PowerPC development and design. The Embedded Products group will further develop AMCC's PowerPC 400 portfolio of products, acquired from IBM earlier this year.

PowerPC veterans **Mark McDermott**, **Sam Fuller** and **Victor Menasce** have joined AMCC's Embedded Products team as VP of engineering, VP of marketing and CTO, respectively. McDermott previously served as GM and director of the Texas Development Center at Intel, director of the joint IBM-Motorola Design Center and director of the Austin Design Center for Cyrix. At Motorola, Fuller held PowerPC management positions. Menasce previously held key positions at Tundra, Nortel and BNR. Dave Rickey, president, chairman and CEO. www.amcc.com

AMI has appointed **John Kent** as VP of technology R&D. Kent previously was the manager of ASIC and Array development for IBM's microelectronics division. Chris King, president and CEO. www.amis.com

Aptix, a supplier of pre-silicon prototyping tools and platforms for embedded SoC design, has named **Dr. Hamdi El-Sissi** as CEO, succeeding Dr. Amr Mohsen, who resigned in April. Dr. El-Sissi was most recently an investment manager focused on IT and communications companies. www.apitix.com

Aspex Semiconductor, has appointed **Jeremy Hendy** as VP of Marketing. Hendy previously held several positions in TI's UK wireless marketing group, followed by 10 years at Symbionics, the wireless & digital TV design house (acquired by Cadence in 1998) serving as

People

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Business Director. Paul Greenfield, CEO. www.aspex-semi.com

AuthenTec, a provider of fingerprint sensors, has appointed **Chris Lister** as director of sales, Americas. Lister previously served as director of sales at Analog Devices and western-area sales director at Harris Semi. AuthenTec has more than two million sensors deployed worldwide. Bill Dennehy, VP of worldwide sales. www.authentec.com

Bandspeed has appointed **Bill Eversole, Ph.D.** as president and CEO replacing interim CEO Walt Thirion, who remains chairman. Eversole worked at TI from 1973 to 2002, where he rose from a defense systems IC design engineer to become GM of the Worldwide DSL Business in the Broadband Communications Group. Since 2002, Eversole served as president and COO of Quellan. Bandspeed's Gypsy SDMA architecture and Listen+Learn software are the basis of the company's AP SOC products. www.bandspeed.com

Bay Microsystems has hired its first CFO, **Michael McDonald**, formerly with ISSI. McDonald was recently VP of finance, CFO and secretary at ISSI. Chuck Gershman, president and CEO. www.baymicrosystems.com

Broadcom has appointed **Dianne Dyer-Bruggeman** as VP of Human Resources. Dyer-Bruggeman previously served as VP of Human Resources at Titan. www.broadcom.com

Cabot Microelectronics, a supplier of chemical mechanical planarization (CMP) slurries, has appointed **Adam Weisman** as VP of Operations reporting to William Noglows, Chairman and CEO. Weisman previously held senior operations management roles at General Electric, including GM of Manufacturing for GE Plastics - Superabrasives, and most recently, as EVP of Operations for GE Railcar Services. www.cabotcmp.com

Cadence has appointed **Michael Fister** as president and CEO, succeeding Ray Bingham, who has been elected chairman. Former chairman Donald Lucas will continue as a director. Fister most recently served as SVP at Intel and GM of the Enterprise Platforms Group. www.cadence.com

CSR has appointed **Richard Ord** as VP, Bluetooth Business Unit. Ord was previously a VP at VLSI Technology and Philips Semiconductor, and CEO of Vulcan Machines. www.csr.com

Engim has appointed **David Gagne** as VP of Sales. Gagne most recently served as VP of Sales at T-Networks. Nick Finamore, CEO. www.engim.com

Fujitsu Microelectronics Europe GmbH (FME) has appointed **Shimpei Hirata**, a Fujitsu career executive with 25 years experience, as president. He is based at FME's European headquarters in Dreieich-Buchschlag, near Frankfurt. Hirata succeeded Yutaka Suzuki who has returned to Japan as Group SVP of Fujitsu's Marketing & Sales Group, Electronic Devices. Hirata was previously Marketing Strategy Planning Director at Electronic Devices. www.fujitsu-fme.com

Infineon has appointed **Dr. Wolfgang Ziebart** as President and CEO. Ziebart most recently served as Deputy Chairman of the Executive Board at Continental AG. **Thomas Seifert** will assume global responsibility for the Memory Products Business Group succeeding the previous Group CEO, Dr. Harald Eggers, who is leaving the company after more than 25 years of service. Until the appointment of a successor, **Peter Gruber**, CFO of the Wireline Communications Business Group, will assume responsibility for the Group headed until now by Seifert, who has headed Infineon's Wireline Communications Business Group since 2002. www.infineon.com

Intellon has appointed **Andreas Melder** as SVP of Sales, Marketing and Business Development reporting to Charlie Harris, Chairman and CEO. Melder previ-

ously was COO of Clarisay, a developer of SAW filter modules for the cellular handset market. Melder was also a founding member of Microtune, where he served as VP of sales & marketing and later, VP of business development. www.intellon.com

ISSI announced that **Henry Pu**, who has over nine years with ISSI in Silicon Valley, has relocated to Shanghai and now serves as GM for ISSI China. Pu joined ISSI in 1994 as Senior Director of Quality Assurance and was promoted to VP of Q&R in 1996. ISSI currently has approximately 85 employees in China. Jimmy Lee, Chairman and CEO. www.issi.com

iVivity, a technology provider for storage networking systems, has created two new management positions that will be instrumental in the launch of its iDiSX technology later this year. **Jim O'Connor** was appointed to the new role of SVP of Engineering and **Ashu Joshi** to VP of Technology. O'Connor joined iVivity as a VP in 2003. Joshi joined iVivity in 2000 as Director of Product Development. David Coombs, president and CEO. www.iVivity.com

Layer N Networks has appointed **Keith McAuliffe** as COO reporting to CEO, Mike Salas. Most recently, McAuliffe held senior management positions at several startups including RLX, Surgient and ClearCube. www.LayerN.com

Motorola has appointed **Michel Mayer** as chairman and CEO of **Freescale Semiconductor**, a Motorola subsidiary that is expected to become a separate, publicly traded company later this year. Mayer most recently served as GM of IBM Microelectronics. Freescale's 2003 sales were \$4.9 billion. www.Freescale.com

Nazomi has promoted **Chamy Ryu** as regional sales manager to manage Nazomi's new Korean office. Jay Kamdar, President and CEO. www.nazomi.com

Nitronex, a manufacturer of gallium nitride (GaN) based RF power transistors,

has appointed **Chris Rauh** as VP of Sales and Marketing. Charles Shalvoy, Executive Chairman and CEO. www.nitronex.com

SMSC has appointed **Louis Lam** as VP and Managing Director of Asia Pacific Sales, reporting to Mitch Statham, VP of Worldwide Sales. SMSC has also opened a new office in Hong Kong, where Louis will be located. Lam previously was Area Sales Director for 3Com's Asia Pacific and Europe OEM Business and Asia Sales and Marketing Director for Telecom Semiconductor HK. www.smisc.com

Stretch has appointed **Reynette Au** as VP of marketing, reporting to CEO Gary Banta. Au previously served as president and CEO for Triscend, which was recently acquired by Xilinx. Prior to Triscend, she was president of ARM Inc., ARM's U.S. operations. www.stretchinc.com ■

Funding & IPOs

Beach Solutions has received \$3 million in second round funding from MTI Partners, Beach's lead investor. The company has raised \$7.2M to date. Beach is a supplier of system-level EDA solutions and design tools for hardware software co-design. Roger Howarth, Marketing Manager. www.beachsolutions.com

Berkana Wireless has closed an additional \$9 million in Series B financing from new investor Hotung Capital Management, along with all existing institutional investors and other new investors. As with Berkana's previous rounds, this new round was oversubscribed. Berkana is developing a single-chip Quad-Band GSM/GPRS CMOS transceiver. David Tahmassebi, president and CEO. www.berkanawireless.com

Cradle Technologies has completed a \$12 million round of funding in a valuation step-up. The round was led by a \$7 million investment from Investor Growth Capital. Previous investors, including Charter Venture Capital, East Gate Capital Management, Prodea, NeoCarta Ven-

tures and Smart Technology Ventures also participated. Cradle is currently shipping a real-time H.264/MPEG-4 AVC video codec solution implemented on a single DSP. Arthur Chang, CEO and president. www.cradle.com

eASIC has secured \$5M in a third round of equity financing from Kleiner Perkins Caufield & Byers. The previous funding rounds involved angel investors and semiconductor industry veterans. The new funds will be used to complete the Structured ASIC product family and tools set that are being jointly developed with Flextronics Semiconductor and Magma Design Automation. eASIC's Structured ASIC technology has been validated by ST Microelectronics and proven in silicon for its high performance and density. The first product member has been taped-out and the full family is scheduled for production release at 0.13 μ process in early 2005. Zvi Or-Bach, President and CEO. www.eASIC.com

Golden Gate Technology has closed its first-round venture capital funding with a \$9 million investment co-led by Lightspeed Venture Partners and Horizon Ventures. GGT develops physical design tools that address the design requirements of low-power ICs. Oki Semi has been using the GGT GoPower/PG Router in its standard design methodology for more than a year and has successfully taped out 20 designs. Dr. Michael Burstein, president and CEO. www.ggtcorp.com

KeyEye, a provider of transceivers for 10 Gbps copper-media communications, has closed an oversubscribed \$15 million Series B financing led by Menlo Ventures and including Series A investors American River and Blueprint Ventures. The company has raised more than \$21 million to date.

KeyEye has validated the successful operation of its multi-channel, multi-level, full-duplex 10 Gbps solution based on its patent-pending EchoWave technology. EchoWave enabled a single-chip solution for full-duplex 10 Gbps communications rates over 4-pair category 5e/6 copper

cable. The company expects to have samples of its first product by the end of 2004. Harvey Scull, president and CEO. www.keyeye.net

Lumera, a majority owned subsidiary of Microvision (Nasdaq: MVIS), has filed a registration statement with the SEC for a proposed IPO of 5 million shares of its common stock. The lead manager for the offering will be Paulson Investment Company, with I-Bankers Securities acting as co-manager. Lumera develops polymer materials and products based on those materials for applications, including wireless antennas and systems, biotechnology disposables, electro-optic devices and polymer-based products for government applications. www.lumera.com

MathStar has closed \$9.6 million in funding, bringing to \$52.3 million its total financing to date. Douglas Pihl, founder and CEO. www.mathstar.com

Miasole, formerly Raycom Technologies, a manufacturer of thin-film solar cells, has closed \$5.4 million in funding led by VantagePoint Venture Partners and including Firelake Strategic Technology Fund, Garage Technology Ventures and Nippon Kouatsu Electric Company. Venture Banking Group also participated. Miasole's technology is based on a proprietary vacuum deposition sputtering technology that is used to apply a thin-film of light absorbing semiconductor material composed of copper, indium, gallium and selenium, more commonly known as CIGS. The CIGS material and other thin-film layers are deposited in a continuous process in the vacuum system on stainless steel foil.

The new funding is earmarked to transition the company's demonstrated R&D process to an existing high volume production system rated for 5MW of annual solar cell output. Last year, Miasole demonstrated solar cells with 12% conversion efficiency, a level competitive with multicrystalline silicon solar cells. Miasole hopes to reduce the cost of photovoltaic modules from today's approximately \$3

Funding & IPOs

(Continued from page 15)

per Watt to less than \$1 per Watt. David Pearce, CEO. www.miasole.com

Mobius Microsystems, an Ann Arbor-based company launched in 2000 that sells patented analog and mixed-signal IP, has received \$50K from the University of Michigan's Wolverine Venture Fund. The investment comes as part of Mobius' near \$1M investment round. The Copernicus Clocking Solution is a completely integrated clock that enables IC designers to put the entire clock function on-chip. The solution requires no pins, external reference, capacitance, or components. It can achieve multiple frequencies from 1kHz to 2GHZ with accuracy of +/-0.75% without trimming. Michael McCorquodale, CEO and CTO. www.mobius-microsystems.com

NetCell has closed a \$13.7 million funding round, led by Allegis Capital with another new investor, Granite Ventures. Earlier investors August Capital and APV Technology Partners also participated. NetCell's storage controller technology solves the reliability risks associated with simple-striped RAID-0 systems in performance desktop PCs and workstations, while simplifying installation and usability as compared to other hardware- and software-based desktop RAID solutions. Andy Mills, president and CEO. www.netcell.com

Nomadics has received an equity investment from Digital Power Capital. Nomadics has developed a sensitive sensor based on molecular wire technology licensed from MIT. This technology sets a new standard for explosive vapor detection and has significant additional applications in Homeland Security and Defense. Related Nomadics technologies provide similar opportunities for the detection of chemical and biological warfare agents. Colin Cumming, CEO. www.digitalpower.com

Plextronics, a pioneer in the commercialization of inherently conductive polymers

(ICPs), has closed a \$3.4 million financing round led by Smithfield Trust Company and including Innovation Works as well as new and existing angel investors. This round also included financial support from the Pennsylvania Department of Community and Economic Development (DCED) and an equipment line of credit with Silicon Valley Bank. Plextronics has secured total financing of \$4.6 million since its July 2002 founding.

Plextronics, a Carnegie Mellon University spin-out, leverages over a decade of research from the laboratory of Dr. Richard McCullough, co-founder and Dean of the Mellon College of Science at Carnegie Mellon University.

Plextronics' products are a new generation of materials that combine the functional benefits of conductivity with the design, processing, weight and cost advantages of plastics. The company's core technology, Plexcore, enables highly conductive and stable systems with superior physical properties at a cost that facilitates broad market opportunities.

These characteristics coupled with multiple integration methods will make Plexcore the material of choice for the coatings, bulk plastics and advanced electronics industries. According to Business Communications Co, the North American market for conductive polymers will increase eight fold to \$1.6 billion over the next four years. Andy Hannah, President and CEO. www.plextronics.com

Qcept, a developer of Chemical Metrology solutions for semiconductor manufacturing, has closed \$4 million in Series B up-round funding led by previous investor Pittco Capital Partners and joined by additional previous investors Atlanta Technology Angels (ATA) and Bergman and Associates. Notable private investors included Steve Chaddick, SVP and Chief Strategy Officer of CIENA, and Meade Sutterfield, president and CEO of SPC-SS and Special Limited Partner of Antares Capital. New investors include O'Neill and O'Neill. Bret Bergman, President and CEO. www.qceptech.com

Quellan has closed \$5.5M in venture funding from Cordova Intellimedia Ventures, ITU Ventures, The University Financing Foundation, Steve Chaddick, and the Yamacraw Seed Capital. Tony Stelliga, CEO and Chairman. www.quellan.com

Sirific Wireless, a developer of single chip multi-standard multi-band RF transceivers, has closed its \$17 million Series B financing round led by TD Capital Ventures with Intel Communications Fund making a strategic investment. Current investors, including Agilent, Celtic House, BDC Venture Capital and GrowthWorks WV Funds, also increased their investment in this oversubscribed round. Sirific is currently demonstrating a single-chip CMOS quad-band EDGE RF transceiver. Production at the end of 2004. Mike Hogan, president & CEO. www.sirific.com

TransChip, a developer of integrated camera solutions for mobile phones and other multimedia-enabled devices, has received approval from the Office of the Chief Scientist (OCS), part of the Government of Israel's Ministry for Industry and Trade, to implement a NIS15.5 million (US\$3.38 million) R&D project.

The OCS will contribute US\$1.352 million for TransChip's R&D in the areas of performance and design of CMOS-based mobile imaging solutions. The 2004 award is the third grant made by the OCS to TransChip. TransChip recently completed a significant US\$19 million Series D funding round led by Redpoint Ventures and including all previous investors. Viktor Ariel, CEO. www.transchip.com

Xanoptix, a developer of 3D semiconductor integration and high-density parallel optics technology, has closed \$15.2 million in Series C Convertible Preferred securities led by primary investors William Blair Capital Partners, Euclid SR Partners, Envest Ventures and Optical Partners. Rob Baxter, Chairman and CEO. www.xanoptix.com ■

Mergers & Acquisitions

Intersil has acquired a substantial portion of the assets of **BitBlitz** for \$2.5 million in cash. In addition, Intersil has agreed to pay contingent consideration of up to \$5 million if certain performance milestones are met in 2004 and 2005. BitBlitz will become part of Intersil's Elantec Products Group. BitBlitz provides high-speed SerDes, retimers and transponders to the networking industry. Mohan Maheswaran, VP & GM, Elantec Products Group. www.intersil.com

Micronas has signed an agreement to acquire **LINX Electronics**, a fabless semiconductor company that develops digital television solutions for improved reception of HDTV signals, for approximately \$26 million in cash and Micronas' shares. LINX has developed an ATSC compliant receiver technology that delivers superior reception. Wayne Li, co-founder of LINX; Hans-Juergen Desor, Micronas VP of consumer products. www.micronas.com

Tegal, manufacturer of plasma etch and deposition systems, has signed a definitive agreement to purchase the assets of **First Derivative Systems**, developer of a mono-block physical vapor deposition (PVD) system for 300mm applications. FDSI has also developed a line of sputtering (PVD) sources for the MD(x) series that meet emerging requirements for 300 millimeter wafer metallization. FDSI was founded in 1999 as a spin-off of Sputtered Films, which itself was acquired by Tegal in August 2002. Michael Parodi, chairman, president and CEO. www.tegal.com ■

Business & Financials

Passave, a provider of semiconductors for fiber-to-the-home (FTTH) systems, has surpassed sales of 500,000 FTTH ports of its standards-compliant Ethernet passive optical networking (EPON) silicon. Demand for EPON ICs is surging, as Asian carriers are quick to adopt the new IEEE802.3ah EPON standard. Pas-

save claims that its' PAS5001-N OLT and PAS6001-N ONU devices are the only mature EPON solutions to provide high-efficiency and programmable dynamic bandwidth allocation (DBA), tailored to QoS requirements of specific applications and carriers. Ariel Maislos, President. www.passave.com ■

Market Research

Worldwide sales of semiconductors rose to \$16.94 billion in April, a sequential increase of 4.1% from the \$16.28 billion reported in March and a 36.6% increase from April 2003, according to the **SIA**. Worldwide semiconductor sales in April, traditionally a strong month for semiconductor sales, reached the highest monthly level since July 2000. Strong sales of cell phones were a major contributor to increased chip sales, especially for DSPs which were up by 6.8%, ASSPs for wireless which grew by 8.8%, and flash memory devices which rose by 3.2%. DRAM month-to-month growth was 10.3%. Sales of image-sensing devices grew 7.6% sequentially. www.sia-online.org

The **world semiconductor market** reached \$166B in 2003, according to the **World Semiconductor Trade Statistics (WSTS)**. Q4'03 indicated a stronger momentum of recovery than originally

anticipated, and Q1'04 has demonstrated consistency and stability in market growth across all regions and major product lines. The WSTS Committee now predicts that the year 2004 will grow 28.4% over 2003, which is a 9% point improvement over the growth projections made last autumn. A deceleration in growth is forecast to 8.5% growth in 2005, followed by virtually zero growth in 2006. In 2007, another recovery cycle is expected to begin, with market growth in the 10% range. www.wsts.org

North American-based manufacturers of semiconductor equipment posted \$1.59B in orders in April 2004 and a book-to-bill ratio of 1.14, according to **SEMI**. The three-month average of worldwide bookings in April 2004 was \$1.59B, 16% above the revised March 2004 level of \$1.38B and 111% above the \$757 million in orders posted in April 2003. The three-month average of worldwide billings in April 2004 was \$1.40B, 10% above the revised March 2004 level of \$1.27B and 67% above the April 2003 billings level of \$840 million. www.semi.org

Flash memory consecutive yearly demand bit growth rates for 2004, 2005 and 2006 over 2003 are forecast to be 209%, 191% and 150% respectively, according to **Web-Foot Research**. The highest contribution to production bit growth will be

WSTS World Semiconductor Market Forecast

	Amounts (US \$B)				Year on Year Growth in %			
	2003	2004	2005	2006	2003	2004	2005	2006
Americas	32.3	39.5	41.7	40.1	3.4	22.2	5.6	-3.9
Europe	32.3	40.5	43.7	43.1	16.3	25.5	7.8	-1.4
Japan	38.9	47.8	51.1	50.3	27.7	22.8	6.8	-1.5
Asia Pacific	62.8	85.8	95.3	96.5	22.8	36.5	11.1	1.4
Total World	166.4	213.6	231.7	230.0	18.3	28.4	8.5	-0.7
Discrete Semis	13.3	16.0	17.0	16.7	8.1	20.2	6.2	-2.0
Optoelectronics	9.5	13.1	14.9	15.3	40.6	37.3	13.4	2.9
Sensors & Actuators	3.6	4.8	5.7	6.3	2)	35.3	18.9	9.1
ICs	140.0	180.0	194.1	191.8	16.1	28.4	8.0	-1.2
Bipolar	.2	.2	.2	.2	-4.2	10.6	-16.3	-25.0
Analog	26.8	33.7	37.0	37.0	12.0	25.6	9.9	-0.1
Micro	43.5	52.4	57.2	57.6	14.3	20.4	9.2	0.6
Logic	36.9	46.4	50.6	49.6	18.1	25.7	9.1	-2.1
Memory	32.5	46.9	49.1	47.6	20.2	44.4	4.6	-3.1
Total Products	166.4	213.6	231.7	230.0	18.3	28.4	8.5	-0.7

Market Research

(Continued from page 17)

added production capacity, followed by the transition to 300mm wafers, the transition to the 90nm manufacturing node and the increase in multi-bit cell components. The demand/production capacity ratio shows an ongoing over demand situation for both NOR and NAND through Q4'04. This imbalance will be as high as 15.7% for NAND 1-bit/cell components in Q2'04 and as low as 0% for NAND low capacity components in Q4/2004. The imbalance situation is forecast to reverse for all five groups of Flash memory components as of Q1'05. www.webfeetresearch.com

The Electronic Product Code (EPC) based **RFID tag market** shows potential for a dramatic revamp over the late 2004/early 2005 period, according to **ABI Research**. Faced with looming mandates from both commerce and government, the Hardware Action Group established by EPCglobal is trying to iron out differences in several proposals for a standardized Gen 2 UHF (868-956 MHz) EPC air-interface protocol. The deadline for completing the standard is October 4, 2004.

Proposals from three groups are under consideration. Each group includes different sets of ICs and transponder manufacturers. The first, known as the Unified Group, consists of Philips, TI and start-up Impinj. A second group, called the Performance Team, has EM Microelectronic Marin, Matrics, Atmel & several smaller companies. The final contender, the Q Proposal, is championed by Alien Technology.

Although all the proposals, based around ISO 18000-6A, are broadly similar in technical terms, there are enough differences to redraw the map of the RFID supply chain depending upon which one prevails. This has less to do with technology than with timing.

Matrics, with its UHF Class 0 chips and Alien Technologies with Class 1 chips,

have been market leaders so far; all the tests being done to this point have used tags from one or the other. However, once the protocol is ratified, those chips will be phased out and replaced with Gen 2 chips. www.abiresearch.com ■

Emerging Trends

Universal Display, a developer of OLED technology for flat panel displays and other opto-electronic applications and **Vitex Systems**, a developer of thin-film packaging solutions for flexible flat panel displays, have unveiled a flexible OLED (FOLED) built on a metallic substrate. The Universal Display FOLED prototype was packaged by Vitex using their Barix encapsulation technology.

The 6" x 6" icon-format OLED prototype using Universal Display's high-efficiency phosphorescent OLED (PHOLED) technology and materials was built on a 4 mil metallic substrate, prepared by Palo Alto Research Center, a subsidiary of Xerox. Enabled by Universal Display's FOLED and transparent/top-emission OLED (TOLED) technologies, the novel use of metallic substrates for OLEDs is a complementary alternative to glass and plastics.

Flexible metallic substrates offer excellent barrier properties, thermal and dimensional stability over a broad temperature range, cost-effectiveness and potential near-term integration with backplane technology for active-matrix displays for applications such as rollable, retractable and rugged displays.

Vitex's Barix technology is a thin-film barrier encapsulation solution comprised of alternating layers of polymer and ceramic film applied in vacuum. The Barix coating has a total thickness of about three microns. Since Vitex's technology can be applied directly on top of an OLED display, it eliminates the bulky mechanical packaging components, while at the same time provides the moisture and oxygen protection required by an OLED display. Steven Abramson,

President & COO of Universal Display; Malcolm Thompson, Vitex CEO. www.universaldisplay.com, www.vitexsys.com ■

New Products

Analog Devices has introduced its EaglePLUS ADSL2/2plus customer premises equipment (CPE) chipset, capable of transmission rates of up to 24 Mbps. The EaglePLUS is claimed to be the first commercially available chipset compliant with the ITU ADSL2/2plus standards, and has established interoperability with the Alcatel 7300 Advanced Services Access Manager (ASAM) in ADSL2plus mode. The EaglePLUS chipset is based on Aware's StratiPHY2+ datapump technology. EaglePLUS also incorporates Reach-Extended ADSL2, which was approved by the ITU in October 2003 (ADSL2 Annex L). RE-ADSL2 uses new power spectral density (PSD) masks that significantly increase ADSL's reach by up to 40%. John Croteau, GM, Media Platforms and Services Group. www.analog.com, www.aware.com

CEVA has introduced Xpert-GPS, a DSP-based GPS solution that reduces power consumption and thus increases battery life by up to 4x that of existing solutions, according to the company. The total solution cost for Xpert-GPS, including the RF component, is estimated to be less than \$3 per unit. Xpert-GPS delivers accurate location information to within 5 meters, reduces the "time to first fix" to 2.5 seconds when a system is first powered up, and provides an instantaneous "location lock" in continuous tracking mode. Xpert-GPS runs on either a single-MAC CEVA-TeakLite DSP or a Dual-MAC CEVA-X DSP. Chet Silvestri, president and CEO. www.ceva-dsp.com

CopperGate has introduced the CopperStream CG3010 Chipset, which enables equipment manufacturers to develop home networking products that transform both existing phonelines and coax cables into a single whole-home network. Cop-

perGate claims that the chip is the first to comply with the HomePNA 3.0 specification, providing 128 Mbps data rate. Unlike other home networking products that provide only prioritized QoS, the CG3010 chipset features guaranteed QoS via a synchronous mode of operation to insure delivery of each data stream with predefined bandwidth, latency and jitter. The chipset provides up to 90% user throughput over both coax and phone-lines. The existing wires can be combined into one network with a \$3 passive device.

The CG3010 chipset is composed of two devices which, together with a low-cost hybrid, comprise a complete HomePNA 3.0 compatible modem. The CG3011 includes the complete PHY, MAC, Link Layer Control and a choice of host interfaces, including USB 2.0, MII/RMII and MSI. The protocol stack runs on an internal RISC processor from expandable on-chip memory capable of also buffering data flows. The CG3010 also provides an adaptation layer that enables transparent bridging to other networks, such as 802.11, 100BaseT Ethernet, IEEE1394 Firewire or UWB. The CG3012 Analog Front-End includes amplifiers, filters, ADC, and DAC and features an optional power boost amplifier for extended-reach applications. Samples now; production in Q3. Gabi Hilevitz, CEO. www.coppergate.com

DataPower has introduced the XG4 (XML Generation 4) product family of XML chips and modules, which deliver XML networking security and acceleration with gigabit performance. The XG4 architecture combines DataPower's XML ASIC, off-the-shelf components and proprietary driver software to perform XPath and XML Schema validation directly in hardware.

The XG4 product family allows OEMs to embed XML Web Services security in traditional firewalls or security switches, SOAP load balancing in server load balancers, or XML acceleration in routers. XG4 ASIC-based subsystems are currently available as PCI cards or PMC

modules, with PCI-X support available in Q3. XG4 chipsets can also be integrated into custom solutions. Steve Willis, VP of Advanced Technology. www.datapower.com

eASIC has taped out its first Structured ASIC array to be fabricated by a European IDM partner, presumably ST Microelectronics, at 0.13u process technology. The taped-out array called FA1, is the smallest member of the company's Structured eASIC product family. The initial parts will be used to characterize timing and power for the Structured ASIC fabric and cell libraries. The complete product family is scheduled to be released for production in early Q1'05. This product is being co-developed with Flextronics Semiconductor who will also be offering Structured ASIC products and services.

The patented Structured eASIC architecture consists of an array of logic cells (eCells) with SRAM-based LUTs (Look Up Table) and flip-flops. eCells are inter-connected by a segmented wiring grid utilizing upper metal layers, which are customized per customer design with a single Via-mask. Logic programming of the eCell is done similarly to an FPGA, by loading a bit-stream to program the LUTs and flip-flops after powering up the device.

Thus, a customer design is implemented on the Structured eASIC fabric by using a combination of bit-stream to program the LUTs and single custom Via-mask for customizing the routing. Single Via-customization is a perfect fit for an alternative lithography approach, namely the Direct-write eBeam, which eliminates the customization tooling cost, shortens time-to-market and adds manufacturing flexibility.

The FA1 features 600K usable ASIC gates, 384Kb bRAM (high density diffused single-port memory blocks), 12 bRAM blocks, 640Kb eRAM (configurable distributed dual-port memory, flexibly traded-off with logic gates, approximately one bit per gate), 160 eRAM

blocks, 4 PLLs, and 372 I/Os. The eASIC family will feature devices with 0.6M - 3M ASIC gates, 0.4M - 1.6M memory bits, and 372 - 820 User I/Os. eASIC was founded in 1999 by Zvi Or-Bach, president and CEO, the founder of Chip Express. www.eASIC.com

Galazar has introduced VersaNode, an OC-12/3 Multi-Service networking solution for Ethernet and PDH services over point-to-point networks, RPR and UPSR rings. VersaNode is ideal for multi-service line cards and customer premise equipment access platforms that are designed to support ring and hub-and-spoke network topologies with distributed layer 2 packet processing over mixed High Order (STS/VC paths) and Low Order (VT/VC paths) Virtual Concatenation (VCAT) groups with Link Capacity Adjustment Scheme (LCAS). Richard Deboer, CEO. www.galazar.com

Inapac Technology has introduced a new solution for integrating DRAM into SiP applications using its proprietary wafer stress methodology called voltage induced burn-in emulation (VIBE). VIBE eliminates the requirement for oven-based, burn-in stress testing, ensuring high quality and reliability at the die level. Inapac's stackable DRAM technology overcomes the primary barrier for space-efficient, economical SiP solutions.

Conventional DRAM often cannot be used for SiP integration, since it requires a post assembly burn-in process of 12-24 hours to reach a suitable quality level. By contrast, Inapac's DRAM die designed specifically for SiP utilize embedded logic circuitry to ensure testing and quality at the die level without costly burn-in through the use of Inapac's VIBE methodology. The company offers stackable, SiP-optimized DRAM in sizes ranging from 16Mb to 128Mb, in bus widths from 16bits to 128bits. **Atsana** has integrated its SoC media processor into a SiP with stacked Inapac DRAM to maintain a 10x10mm footprint. Inapac's technology has also been proven in other SiP applications with major semiconductor

New Products

(Continued from page 19)

manufacturers. Jean-Pierre Braun, President and CEO. www.inapac.com

MathStar announced availability of its Field Programmable Object Array (FPOA) for customer demonstration. The FPOA family offers a combination of a deterministic clock (up to 1 GHz), low recurring costs, off-the-shelf programmability, and no mask costs. The first FPOA devices have 400 1 GHz Silicon Objects, resulting in a device with 400 giga operations of performance. Silicon Objects are 16-bit medium grained devices like ALUs, Multiply-Accumulators, Pattern-matching CAMs, Register Files, CRCs and Truth Functions. The device is fabricated in 130nm technology. General availability in Q3. Dean Westman, VP of Sales & Marketing. www.mathstar.com

PowerDsine has introduced the PD64004 4-Channel Power over Ethernet (IEEE 802.3af) Manager developed jointly with Motorola and using Mot's SMART-MOS8 technology. The device will join the 12-port PD64012, broadening PowerDsine's offerings of PoE ICs. Samples in Q3; production in Q4. Igal Rotem, President and CEO. www.powerdsine.com

Pulse~LINK has developed an IC for a media-diverse UWB Software Defined Cognitive Radio (SDCR) solution. The test silicon unveils an architecture that supports Pulse~LINK's UWB wireless, UWB power line, and UWB cable communications technologies simultaneously on the same chipset. Combining these networking technologies on a single chipset allows consumer electronics and computing devices around the home to be seamlessly networked together.

Pulse~LINK's target data rates for its chipset, planned for commercial release in mid-2005, are up to 1 Gigabit for UWB wireless connectivity, up to 200 Mbps for UWB power line communications (elec-

trical wiring in homes and small offices), and up to 1 Gigabit of new downstream bandwidth across existing cable television networks in addition to hundreds of megabits of new bandwidth per node upstream. John Santhoff, CTO. www.pulselink.net

RFDomus has introduced its Q-MAX technology, which is based on a local oscillator (LO) architecture that enables an order-of-magnitude reduction in power consumption when compared to conventional LO implementations. Designed for simplifying the integration of the LO block with other radio blocks in CMOS and SiGe processes, Q-MAX provides the flexibility needed for inclusion in complete single-chip RF transceivers.

In RF transceivers, the LO block typically consumes the majority of the power due to causes that include the common methods used for generation of accurate in-phase and quadrature oscillator signals required for high performance wireless communications systems.

Leading-edge SiGe and RF-CMOS processes project a roadmap of increasingly high Q factor inductors, based on continuing advances in metallization, and eventually RF-MEMS. Although high Q inductors theoretically should equate to lower LO power consumption, conventional LO architectures are unable to leverage these process advances into substantial improvements in power consumption without decreasing performance.

Q-MAX technology is synergistic with high Q inductors resulting in an order-of-magnitude reduction in power consumption, while maintaining or improving performance, with equivalent or lower cost to implement.

Q-MAX technology is portable to multiple wireless communications applications such as GPS, Bluetooth, Wireless LAN and Ultra-Wideband. Using Q-MAX, RFDomus has designed a LO

block for GPS applications that consumes 10x less power than an LO in competitive products, according to the company. The company is designing a LO for Bluetooth applications and expects to achieve similar results. RFDomus plans to exploit Q-MAX technology in a family of ultra low power single chip RF transceivers. Kevin Strong, EVP of Business Development. www.rfdomus.com

StarCore has introduced its new V4 architecture for use in mobile electronic devices. Combining an average of 50% higher video processing capability, improved RTOS support and enhanced program control compared to previous StarCore processors, the new architecture advances video performance, while slashing power consumption in half.

The StarCore V4 architecture accelerates encoding and decoding of video algorithms, such as MPEG-4, H.264, Windows Media Video 9 (WMV9), and RealVideo, via application-specific instructions and the high level of parallelism of the StarCore variable-length execution set (VLES) architecture.

New SIMD instructions allow the V4 architecture to execute up to 54 elemental RISC operations per clock cycle when performing motion estimation. As a result, processors based on the StarCore V4 architecture can perform simultaneous software encoding and decoding of VGA-quality MPEG-4 video at 30 frames/second and beyond.

The new architecture features improved OS support and superior code density. The architecture introduces partial pipeline interlocking and new instructions that make the architecture a better compiler target and improve the density of compiled code.

Freescale recently collaborated with StarCore to adopt the architecture for future cellular handset products and communication infrastructure products. The StarCore architecture is currently used in

Motorola's MXC platform and 2.5G, 2.75G and 3G handsets as well as their existing communication infrastructure products. The StarCore SC2000 family of processor cores will be the first to implement the StarCore V4 architecture. The SC2000 family is based on a six-stage pipeline that is optimized for low power consumption, allowing the processors to operate at frequencies of up to 450 MHz in worst-case 90-nm silicon technology and up to 600 MHz in typical devices.

Lead customers have already started to design around the new cores. General availability of the SC2000-family cores and platforms is planned for late summer this year. Alex Bedarida, VP of marketing. www.starcore-dsp.com

Tarari has released its RAX Content Processor, which incorporates the industry's first in-silicon implementation of Random Access XML (RAX), according to the company. RAX fundamentally changes how XML is utilized, as it allows complex XML document analysis to be completed at up to 200x that achieved by software-only solutions. RAX enables network switch, server, blade, and appliance vendors to create a variety of new applications such as gigabit message classification and routing, high transaction rate publish and subscribe systems, advanced SOAP message processing, high performance XML security firewalls and real-time telecom billing solutions.

According to ZapThink, the amount of XML traffic on the Internet is already nearly equal to the amount of email traffic, and will grow to 4x the amount of email traffic by 2006. To ensure the integrity and security of these applications, all their XML messages must be thoroughly inspected and analyzed without significantly impacting network and system performance.

RAX utilizes W3C standards-based XPath queries, which are becoming the most popular way to decode and route

XML documents. Today's method of parsing using XPath involves sequentially processing each XPath query, which is too slow and compute-intensive to be practical in large-scale solutions. The Tarari RAX Content Processor enables gigabit-level XPath processing by simultaneously processing very large groups of XPath queries and offloading compute-intensive tasks from the main processor. Simultaneous XPath is vastly faster than any software-based XPath engines like Saxon, Xalan, and libxml.

The most efficient way, until now, to process XML has been to use one of two programming interfaces: DOM or SAX. However, these software-based approaches don't scale. Tarari's Simultaneous XPath engine produces results directly from the input XML document, whereas DOM or SAX-based systems need to create an in-memory representation of the document. Tarari is proposing that RAX be accepted as an industry-standard just as DOM and SAX have garnered many supporters within the W3C community. The Tarari RAX Content Processor, currently implemented in an FPGA, is available on Tarari's Nitro series of PCI-based Processing Platforms. Randy Smerik, president and CEO. www.tarari.com

Ultra Data has introduced its first product, the UD3000 fully programmable video processing IP core. The UD3000 is a complete video subsystem available for license to companies developing ICs for the home entertainment market. The UD3000 includes a complete Verilog design package as well as software for all three high-definition video decoders specified by the DVD Forum: ITU-T/ISO H.264/AVC, Microsoft's WMV9 HD and MPEG-2.

The UD3000 includes two enhanced RISC processors for initial processing of the encoded bit stream, three 64-bit VLIW processors for video operations and a "smart" DMA controller for moving two-dimensional arrays of video data.

The UD3000 achieves a worst-case clock speed of 400 MHz and sustains 4.8 billion multiply-accumulates per second in a 130nm ASIC process. David Yager, VP of Sales and Marketing. www.ultradatacorp.com

Xceive has introduced the XC2028, an ultra-small analog TV one-chip receiver. The XC2028 receives TV signals anywhere on the planet, regardless of the local standards environment. Xceive has also introduced the XC3028, which is claimed to be the smallest single-chip analog, digital terrestrial, and cable receiver that enables "TV Anywhere." Samples in July; production in Q4. Jordan Du Val, VP of sales and marketing. www.xceive.com ■

Licensing & Partnerships

Xelerated has developed a joint solution with **Broadcom** enabling the development of future proof switches for Enterprise and Metro Ethernet applications. The reference design is based on Broadcom's StrataXGS family of Ethernet Switch chips and Xelerated's family of fully programmable network processors. Together these chips enable networking OEMs to build cost effective, flexible, high-functionality switches ranging from stackable to chassis-based systems.

To complement the standard fixed Ethernet/IPV4 feature set provided by the StrataXGS chipset, Xelerated's network processor provides programmable feature set extensions including IPv6, MPLS and VPLS. These feature set extensions are provided as a "Virtual ASIC" application package covering IPv6 (unicast/multicast, access control lists), MPLS LER/LSR, VPN (VPLS PWE3/Martini) and IPv6 to IPv4 transition mechanisms. Like all applications implemented in the Xelerated network processors, wire-speed performance is guaranteed thanks to the NPUs' data-flow architecture.

Unlike hard coded solutions, customers can obtain a fast time to market with the

Licensing & Partnerships

(Continued from page 21)

“Virtual ASIC” application package and still has the option to offer additional proprietary value-add features by leveraging the programmability of the Xelerated NPU. Due to the programmability, Xelerated can support new features like IP-FIX, Netflow and sFlow without having to do costly re-spins.

An advanced services chipset and virtual ASIC software capable of supporting four full-duplex Hi-Gig™ links (up to 48 Gigabit Ethernet ports or four 10 Gigabit Ethernet ports) is priced at \$500 for high volumes. The solution is based on the Xelerated X10q NPU and SPI4.2-to-HiGig buffer manager, while Xelerated's next generation network processor, the X11, sampling in Q4 this year, will connect directly to the StrataXGS products. Martin Lund, Senior Director Broadcom's Enterprise Switching LoB; Tho-

mas Eklund, VP of Business Development. www.xelerated.com ■

Customer Wins & Trials

Zarlink announced that **Given Imaging**, maker of the only swallowable camera capsule for diagnosis of disease of the gastrointestinal tract, is now using an ultra low-power transmitter chip from Zarlink in its M2A capsule endoscope. The M2A capsule consists of a microchip camera, LED that act as a flash, Zarlink's RF transmitter chip, antenna and two silver-oxide batteries. Steve Swift, VP & GM, Ultra Low-Power Communications. ulp.zarlink.com ■

Late Breaking News

Ambarella, a fabless chip startup in Sunnyvale, is focusing on next-gen consumer digital media applications and is funded by a first tier global VC firm. Ambarella is incorporating @HDL products, including @Verifier and @Design-

er, for the development of its SOCs. Chan Lee, VP of VLSI Engineering. www.ambarella.com

Quorum Systems has introduced the QC 2530, a single-chip, multi-mode RF transceiver that is able to support both WLAN and Quad Band GSM cellular applications simultaneously. The QC2530 converges 802.11b/g WLAN and cellular GSM/GPRS/EDGE technologies in a single die using Quorum's Multi-Access Technology (QMAT) IP, which allows the radio resource to be shared. Samples now. Bernard Xavier, co-founder, president and CEO. www.quorumsystems.com

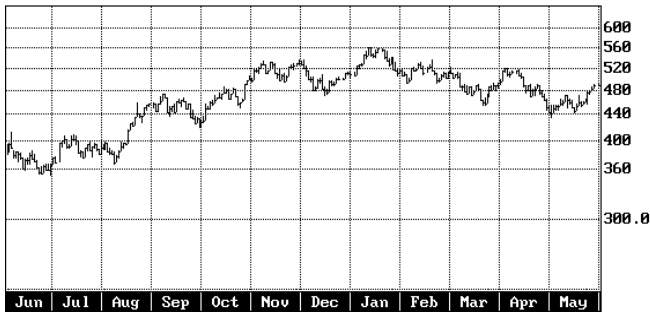
SEQUANS, a fabless chip startup created in 2003, has joined the WiMAX Forum. SEQUANS is develops SOCs addressing both Base Station and Subscriber Station products with the complete IEEE 802.16 PHY and MAC layers supported by the WiMAX Forum. Georges Karam, president and CEO. www.sequans.com ■

Company Financials

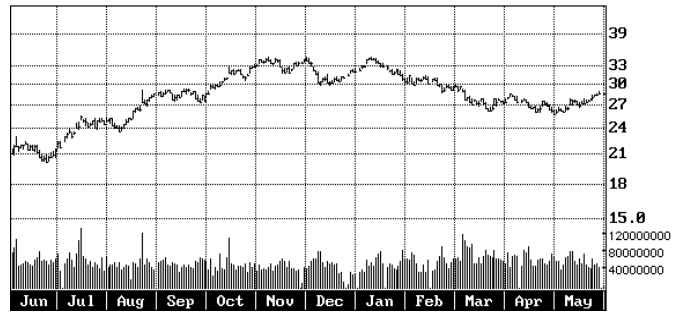
Company	Symbol	Current Qtr.				Last Qtr		Yr ago qtr			Sales Growth	Qtr	Ending
		Sales	Net	Margin	GM	Sales	Net	Sales	Net	GM			
Analog Devices	ADI	679	152.6	22%	59%	605	116.8	502	71.3	54%	35%	2Q04	1-May
Atheros	ATHR	43	2.4	6%	44%	38	-0.2	9	-5.4	0.4	359%	1Q04	31-Mar
Aware	AWRE	4	-1.1	-31%	n/a	3	-1.3	2	-3.0	n/a	89%	1Q04	31-Mar
C.M.D.	CAMD	16	1.8	11%	41%	17	0.0	11	-3.5	2%	46%	4Q04	31-Mar
Catalyst	CATS	17	5.6	33%	49%	17	2.4	13	4.0	42%	34%	4Q04	30-Apr
CSR	CSR	37	7.1	19%	48%	27	4.7	11	-2.4	0.4	244%	1Q04	2-Apr
Focus Enhancements	FCSE	4	-1.6	-39%	32%	7	-0.5	4	-1.0	41%	0%	1Q04	31-Mar
IXYS	SYXI	54	-5.2	-10%	15%	36	-1.8	38	-5.5	11%	42%	4Q04	31-Mar
Marvell	MRVL	270	14.5	5%	53%	243	19.8	168	4.4	55%	60%	1Q05	1-May
Microtune	TUNE	11	-8.7	-79%	46%	11	-10.3	13	-14.7	17%	-13%	3Q03	31-Mar
MoSys	MOSY	5	-0.5	-11%	89%	3	-0.4	8	2.7	87%	-43%	1Q04	31-Mar
Neomagic	NMGC	1	-7.0	-1000%	0%	1	-6.7	1	-6.6	0%	17%	1Q05	30-Apr
NVIDIA	NVDA	472	21.3	5%	32%	472	24.2	405	19.7	31%	17%	1Q05	25-Apr
O2Micro	OIIM	22	4.2	19%	58%	25	5.0	19	1.7	56%	15%	1Q05	31-Mar
Semtech	SMTC	62	14.8	24%	59%	55	12.5	44	8.3	56%	41%	1Q04	25-Apr
Sigma Designs	SIGM	8	0.2	3%	67%	7	0.3	8	0.4	59%	0%	1Q05	30-Apr
Siliconix	SILI	118	14.0	12%	30%	109	10.5	98	10.0	29%	21%	1Q04	3-Apr
Simtek	SRAM.OB	4	-1.0	-29%	31%	4	-0.3	4	-0.6	36%	-10%	1Q04	31-Mar
Sipex	SIPX	18	-3.7	-20%	25%	4	-17.1	15	-7.2	-1%	20%	1Q04	3-Apr
Supertex	SUPX	14	0.3	2%	38%	13	0.6	15	1.1	41%	-6%	4Q04	31-Mar
Synopsys	SNPS	295	28.7	10%	78%	285	32.2	292	22.3	0.8	1%	2Q04	30-Apr
Tvia	TVIA	0	-1.5	-312%	44%	1	-2.9	1	-2.1	40%	-4%	4Q04	31-Mar
Zarlink	ZL	51	-2.3	-4%	46%	47	-11.2	53	-23.6	50%	-3%	4Q04	26-Mar

Notes: All figures in millions, unless noted. GM = Gross margin.

Philadelphia SOX Index



Intel



Micron – DRAM Barometer



TSMC



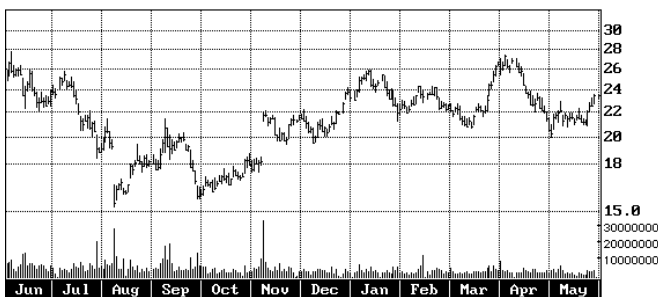
Analog Devices



Marvell



NVIDIA



Siliconix



Startups In This Issue

- ✓ **Ascenium** – Reconfigurable Processor Architecture
- ✓ **Ashvattha** – Quad-band GSM/GPRS, Bluetooth, GPS Receiver
- ✓ **Blue Pearl** – RTL Closure Software
- ✓ **Chelsio** – 10-Gigabit Ethernet Host-Bus Adapter
- ✓ **Enpirion** – Power Systems on a Chip
- ✓ **FishTail Design Automation** – Timing Constraints EDA Tools
- ✓ **g2 Microsystems** – Active RFID Devices
- ✓ **IPextreme** – Extreme Programming-based Semiconductor IP
- ✓ **Lighthouse Design Automation** – Verification Tools
- ✓ **Microbridge** – Electronically Adjustable Resistive Chips
- ✓ **Nannor** – Design for Manufacturability Solutions
- ✓ **Nascentric** – EDA Software for Nanometer Effects
- ✓ **NetEffect** – iWARP RDMA Ethernet iNIC Chips
- ✓ **Sierra Design Automation** – IC Implementation Tools
- ✓ **Silicon Construction** – Video Analog Front-End
- ✓ **SiVerta** – RF MEMS Switches
- ✓ **Stelar Tools** – EDA for Large, Complex HDL Designs

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