A CMOS Magnetic-Field-Controlled Duty-Cycle Oscillator Sensor

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ABSTRACT

A differential current generated by a MAGFET array is converted to a varying duty cycle waveform by a high speed twin capacitor oscillator. The output duty cycle varies linearly with magnetic field strength. The entire sensor circuit was fabricated on a 2μm CMOS process.

I. INTRODUCTION

Of late there has been a growing interest in integrated magnetic field sensing. Magnetic sensors have been used for current or power metering, contactless switching (for example in keyboards) and position detection (for example in brushless DC motors). Traditionally hall plate sensors have been used. However, because CMOS is the technology of choice for many integrated systems, the split-drain MOSFET magnetic field sensor (or MAGFET) [1] has been the subject of recent research.

Circuits have been presented which convert the differential output current of a single MAGFET to a voltage [2,3], and to a varying frequency [4]. However, in telemetry, a varying duty cycle is less affected by noise [5], and the duty cycle signal can be more useful in some applications, for example power electronics. Furthermore, digitization of such a signal is easy to implement.

Recently, a bipolar voltage-controlled duty-cycle oscillator implemented as a temperature transducer was described [5]. A CMOS magnetic-field-controlled oscillator is described here. Unlike the bipolar circuit, this circuit offers a linear relationship between true duty cycle $t_1/(t_1+t_2)$, not mark to space ratio t_1/t_2, and input stimulus.

II. MAGFET

The basic sensing element used in the transducer is a split-drain MOSFET, commonly referred to as a "MAGFET" (see Fig. 1). In the presence of a magnetic field perpendicular to the device surface (B), carriers travelling from source to drain are deflected resulting in a difference in drain currents. The differential drain current is linearly related to the magnetic field strength. Experimentation has shown the optimum MAGFET aspect ratio (W/L) to be close to unity [6], verifying theoretical and simulation work.

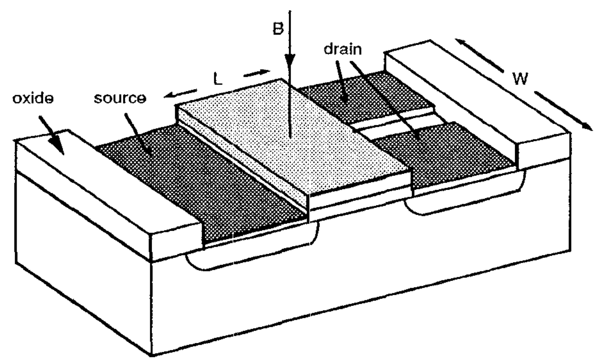

Fig. 1. MAGFET structure.

Sensitivity can be defined as the ratio of differential drain current per Tesla of magnetic field to the total drain current.

$$\text{Sensitivity} = 100\left(\frac{1}{B}\frac{I_{D1}-I_{D2}}{I_{D1}+I_{D2}}\right)\%/T,$$

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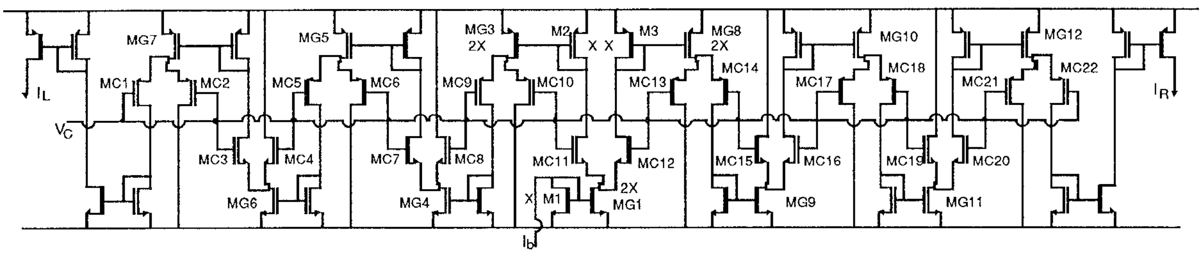

Fig. 2 MAGFET Array.

where I_{D1} and I_{D2} are the split-drain currents. N-type MAGFETs with a unity aspect ratio were found to display a sensitivity of approximately 4% per Tesla. Because of their lower carrier mobility, the sensitivity of equivalent p-type devices was found to be much less, approximately 0.9% /Tesla.

III. MAGFET ARRAY

In order to achieve higher sensitivity, MAGFET's have been combined in a genealogical tree structure, and in parallel [7]. A parallel array structure is shown in Fig. 2. This array differs from earlier implementations in that MAGFET's (p and n type) form part of the current mirrors. In the figure MG1, MG4, MG6, MG9 and MG11 are n-type MAGFETs, whereas MG3, MG5, MG7, MG8, MG10, and MG12 are p-type devices. Because the sources of the MAGFET's are always connected to the appropriate rail voltages, both n and p-types are unaffected by the body effect.

The array works as follows: A bias current I_b is fed into the diode-connected MOSFET M1, which generates a gate voltage for the MAGFET MG1. Because the aspect ratio of MG1 is twice that of M1, the total current through the MAGFET is equal to $2I_b$. In the absence of a magnetic field the drain currents of MG1 are identical and so must equal I_b. The drain currents are fed into two diode connected p channel transistors (M2 and M3) which generate gate voltages for the p-type MAGFETs MG3 and MG8. Again in the absence of a magnetic field the drain currents of these devices and similarly the drain currents of all other MAGFET's are equal to I_b. In the presence of a magnetic field the deflections of the individual MAGFET's accumulate to give a much larger overall deflection and sensitivity. The total sensitivity of the array S_{Array} is approximately

$$S_{Array} = 3S_p+3S_n,$$

where S_p is the p MAGFET sensitivity and S_n is the n-type sensitivity. Cascode devices (MC1 and MC2) are used to lessen the difference in MAGFET drain voltages, in an effort to minimize offset and improve linearity.

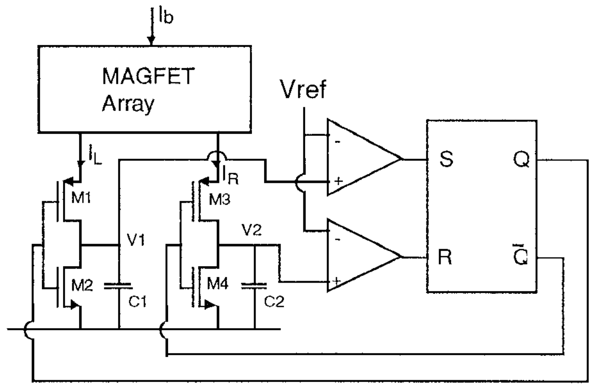

Fig. 3 Block diagram of oscillator.

IV. DUTY CYCLE OSCILLATOR

A current-controlled oscillator architecture which transforms the differential current output of the array to a varying duty cycle, is shown in figure 3. The oscillator is based on a recently presented double capacitor oscillator [8]. In order to understand how the circuit works, assume there is no magnetic field so that both current outputs of the array (I_L and I_R) are equal. If the latch output Q is low, capacitor C1 will be charged through M1 until V_1 exceeds V_{ref} at which point the latch changes state, C1 discharges through M2 and C2 begins to charge through M3. Because discharging proceeds rapidly the oscillation period is determined solely by the charging times. In this way the capacitors are responsible for alternate halves of the duty cycle, and because of symmetry a 50% duty cycle is achieved.

In the presence of a magnetic field the currents from the MAGFET array are no longer equal. The capacitor charging currents are no longer equal, and the duty cycle changes accordingly. If the switching and comparison time t_d at the end of each half cycle is ignored it can be shown that the duty cycle varies linearly with the differential array current and hence also linearly with magnetic field strength. In equation form, where B is the magnetic field strength, and K_{Array} is the sensitivity of the array

$$\text{Duty Cycle} = \frac{t_1}{t_1+t_2} = 100(0.5 - K_{Array}\,B)\%$$

It can be seen that the output is not dependent on capacitance or reference voltage value V_{ref}. This structure has the added advantage that it does not require linear floating capacitors. In fact simple MOS gate capacitors can be used without detrimental effects. Furthermore as the capacitors are charged from ground potential to V_{ref}, relatively large capacitor voltage amplitudes are achievable, thus helping to minimize jitter [9].

The delay time t_d contributes nonlinearity to the sensor characteristic. To minimize this effect the two comparators and latch were implemented as a fast double differential latching comparator (Fig. 4). MOSFET's M1, M2, M3 and M4 resemble the differential pair and active load of a classical CMOS gain stage. The extra components, M5 and the resistor RL help latching to occur. The state of the latch is stored on the parasitic capacitances of nodes S and R. To understand how the latching comparator works assume that initially node S is low, node R is high and V_1 the voltage across C1 is rising. Because S is low M5 is off, and so the gate voltage of M4 is set by the current flowing through the diode connected device M3. When V_1 exceeds V_{ref} the current flowing through M2 becomes greater than that through M1. The drain of M4, node S, rises turning on M5. The resulting voltage drop across R causes the gate voltage of M4 to fall, and because of the feedback action S is latched high. The high value of S activates the pull down MOSFET MP2 pulling node R low so that the entire latch has now changed state. In the same way the latch will again change state when V2 exceeds V_{ref}.

V. Experimental Results

The sensor circuit was implemented in a 2 micron 10V n-well process. The timing capacitors were implemented as double poly structures and n-wells were used to form the resistors. A photomicrograph of the circuit is given in Fig. 5. The entire sensor occupies an area of approximately 500,000 μm^2. A graph of the duty cycle output versus magnetic field for a 10μA bias current, over a +/- 500mT range, is given in figure 4. The duty cycle changes by 6.95% when the magnetic field strength is varied by 1 Tesla. This change represents 13.9% of the nominal 50% duty cycle value. The end point nonlinearity of the characteristic is less than 2%.

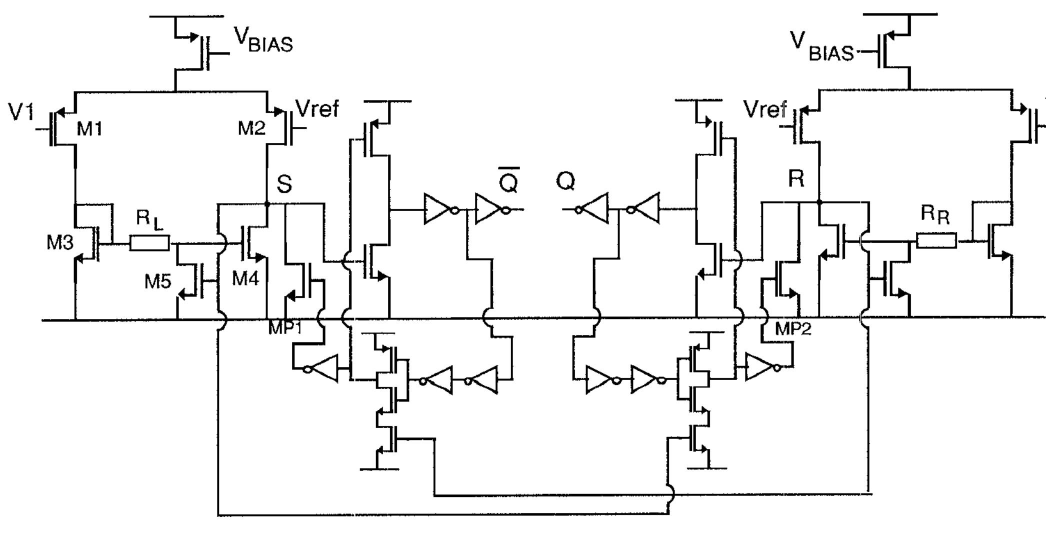

Fig. 4. Double differential latching comparator.

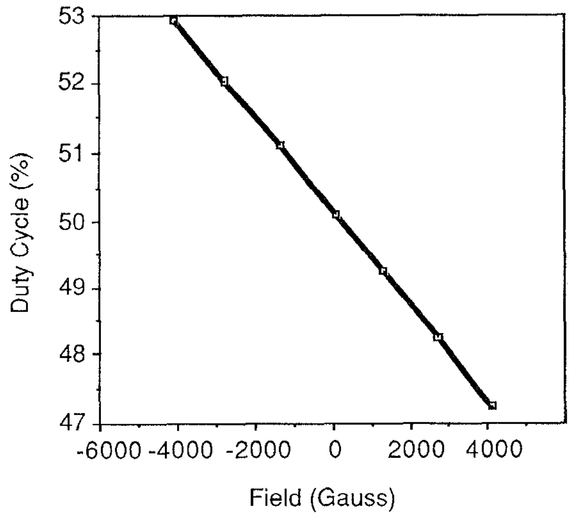

Fig. 5. Measured characteristic.

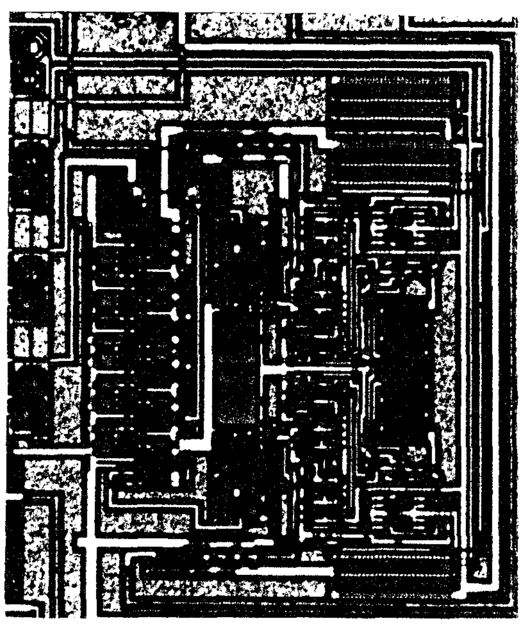

Fig. 6. Die photomicrograph.

VI. CONCLUSIONS

A magnetic field sensor circuit with a duty cycle output has been described. Greater sensitivities can be achieved by simply adding more MAGFETs to the array. Because MAGFET's are compatible with standard CMOS and because the circuit has no special capacitor or resistor requirements the entire circuit can be fabricated with a digital CMOS process.

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