

A ‘Digital’ 6-bit ADC in 0.25 μ m CMOS

Conor Donovan^{1,2} and Michael P. Flynn^{2,1}

¹National Microelectronics Research Centre, Dept. of Microelectronics, National University of Ireland at Cork, Ireland.

²Parthus Technologies plc., Cork, Ireland.

Abstract

Traditionally, circuit designers have adopted analog techniques to overcome comparator offset in flash converters. These schemes usually have an adverse effect on area and power consumption, and more seriously do not scale easily to low voltage processes. We describe a digital technique, which removes the accuracy constraints from the comparators. With no analog matching requirement, the comparators can be small, fast and power efficient. A 6-bit prototype converter built in a standard 0.25 μ m digital CMOS process occupies 1.2mm² and dissipates 110mW from a 2.2V supply at 300Ms/s.

Introduction

In a conventional flash converter, the comparators are either designed to be accurate or some form of analog offset cancellation is applied to control comparator error. In [1] the transistors are made sufficiently large to control mismatch and hence comparator error. For fine geometry processes, this scheme usually implies an increase in gate length, causing power and area to grow. In [2] the input to each comparator is pre-amplified and switched capacitor techniques are used to cancel the pre-amplifier offset. Switched capacitor techniques do not scale well and the preamplifiers consume power and area. More seriously the offset cancellation has to be repeated regularly, perhaps every millisecond. In another scheme [3] each comparator offset is trimmed with the help of a DAC current, increasing the analog complexity of the circuit.

Here, we describe a purely digital solution to the problem of comparator offset. The scheme removes any requirement for comparator accuracy, therefore the comparators can be small, fast, and power efficient. In practice, the comparators need be only be accurate to only 1 or 2 bits. In effect, analog accuracy is traded for complexity in the digital encoder. Because the scheme is dominated by digital circuitry, it will scale readily to finer geometry process. The converter functions from a supply voltage as low as 2V. Unlike recently reported devices, a 3.3V supply or a thick gate-oxide option are not required.

Architecture

A. The standard flash converter

Fig. 1 is a block diagram of a typical flash analog-to-digital

converter. There are 2^{n-1} comparators, one dedicated to each of the comparator codes. A resistor ladder sets the nominal trip-points or thresholds for the comparators. The comparator outputs form a thermometer code. The position of the meniscus (i.e. the 1-0 transition) represents the analog input and is determined by a transition detect circuit (usually a series of NAND gates). The ‘1 in n’ code generated by the transition detect block is converted to binary.

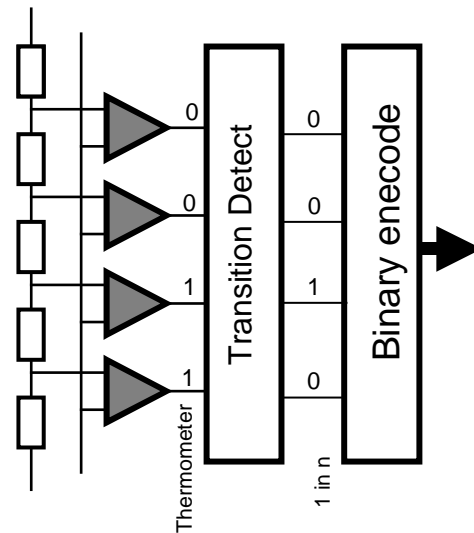


Fig 1. A conventional flash converter

B. The Pruning Calibration technique

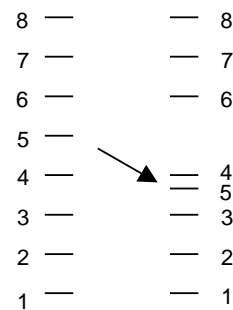


Fig 2(a) Ideal thresholds and (b) an example of a trip-point offset

In practice there may be random and systematic offsets in the comparator trip points. Fig 2(a) shows a series of ideal

thresholds in an ADC. In Fig 2(b) threshold 5 has an offset greater than one LSB, causing a missing code and a large DNL error.

Reassignment of comparator thresholds is an important part of the new technique. In Fig. 3, threshold 5 is re-assigned to represent code 4, and similarly threshold 4 is re-assigned to represent code 5. After this re-assignment the sequence of thresholds becomes monotonic. The missing code is eliminated but there is still a large DNL error.

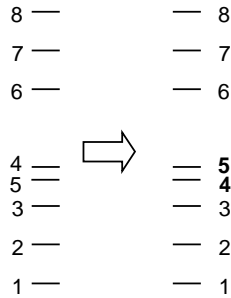


Fig 3 Comparators 4 and 5 are reassigned to eliminate a missing code

The second and key part of the technique is to initially allocate more than one comparator to each code. During a calibration sequence (at power on), for each code, the comparator with a threshold closest to the ideal value for that code is chosen. (In the prototype four comparators are initially allocated to each code)

Nominal Trip	Code	Actual Trip	Code
5a-----5b-----5c-----	5	5b-----	5
4a-----4b-----4c-----	4	5a -----4b----- 5c	4
3a-----3b-----3c-----	3	2a----- 5a ----- 5c	3
2a-----2b-----2c-----	2	3a----- 5a ----- 5c	2
1a-----1b-----1c-----	1	5a ----- 5c -----	1

Fig 4 (a) Ideal trip points (b) choosing the best comparator for each code.

It is important to note that a comparator nominally assigned the one code, can be assigned to represent another code. Depending on its actual trip point, a comparator can potentially be assigned to any one of the codes. This makes the use of extra comparators far more efficient. There is no requirement for the comparator thresholds to be accurate. However the comparator trip-points should be constant.

Because the unassigned comparators are powered down, only the 2^{n-1} selected comparators consume power. With no matching constraints the comparators are far smaller than in conventional design. The unused comparators occupy little area. In practice the comparator cell is only a slightly larger than a

standard digital library flip-flop. Furthermore because the devices can be small, the comparator is fast and power efficient.

The pruning calibration technique is illustrated with an example in Fig 4. In this example, three comparators are initially allocated to each code (Three rather than four comparators are shown for clarity). The nominal trip voltage for each set of three comparators is equal to the ideal trip voltage (the dashed line) for the corresponding code. In this example the actual trip voltages for the comparators differ considerably from the nominal values. (For example the the trip voltage of comparator 1c is 4LSBs from its nominal value.). During calibration the comparator with the most appropriate actual trip voltage is assigned to each code. In the example comparator 5c is assigned to code 1 and comparator 3a is assigned to code 2.

Circuit Blocks

A. Calibration

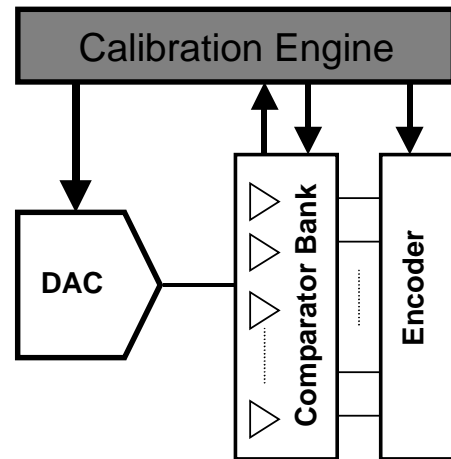


Fig 5. The ADC in calibration mode

At power on the ADC is calibrated. During this time 2^{n-1} comparators (i.e. 63 in this case) are selected from the bank of comparators, and one is assigned to each code. Fig. 5 shows a block diagram of the converter in calibration mode. The resistor ladder is reconfigured as a DAC. A state machine, the *calibration engine*, controls the calibration sequence. For each code, the engine adjusts the DAC output voltage to search for the comparator with a trip point closest to the ideal value. Once a comparator is chosen for a code, it is removed from the list of available comparators.

B. The Comparator

The converter uses a simple CMOS comparator [6]. Minimum length MOSFETs are used throughout, making the

device fast and power efficient. We estimate the 1σ input-referred offset of the comparator to be approximately 50mV (i.e. ~ 4 LSBs). There are no preamplifiers, and because the comparator is fast and has a short aperture time, no sample-and-hold is required.

At the end of the calibration sequence unused comparators are powered down so that only useful comparators (in this case 63) consume power. Care is taken to discharge gate channel charge of the input MOSFETs of the unused comparators. This minimizes the converter input-capacitance.

C. Encoder

In the design of the encoder the following must be considered:

- Comparators that are not assigned during calibration are ignored.
 - The encoder must also account for the re-assignment of comparators.
 - The comparator output does not form a thermometer code
- Clearly the encoder scheme of a conventional flash converter cannot be used.

Comp #	Decision	Comp#	Decision	Comp #	Decision
8	0	8	0	8	0
7	0	7	0	7	0
6	0	6	0	6	0
5	1	4	0	5	1
4	0	5	1	4	0
3	1	3	1	3	1
2	1	2	1	2	1
1	1	1	1	1	1
					sum = 4

(a)

(b)

(c)

Fig 6. Comparator outputs (a) with offset, (b) reassigned and (c) summed.

Instead of explicitly reassigned comparators, the same result can be achieved by summing the comparator outputs. This is shown in Fig 6. Fig 6(a) shows a sequence of comparator outputs where one of the comparators has a large error. If comparator outputs are reassigned then the thermometer code can be processed in the standard way (Fig 6(b)). Alternatively the comparator outputs can be summed, giving the same answer (see Fig 6(c))

This summing approach was judged to be too slow for this prototype. Instead a hybrid two-stage approach is used. The output of the comparator bank is fed to the two stage encoder (Fig. 7). The coarse encoder determines the 3MSBs and passes an 8-bit residue to fine stage. In a sense, the coarse encoder determines in which octant the output lies. (The coarse encoder is programmed during calibration). The 8-bit residue transferred to the fine stage is the output of the comparators in that octant. The fine encoder stage sums the 8-bit residue to form the 3

LSBs. A 3-bit register aligns the coarse and fine encoder output.

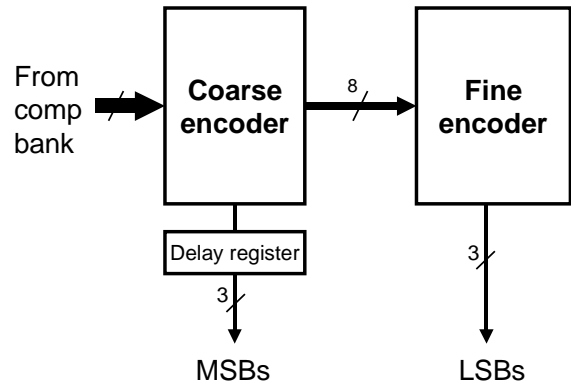


Fig 7 Two stage encoder

Experimental Results.

A 6 bit prototype converter was built in a 5 metal, single poly, 0.25 μ m digital CMOS process. The converter occupies 1.2mm². The device was packaged in a 28 pin ceramic LCC. A die photograph is given in Fig 8

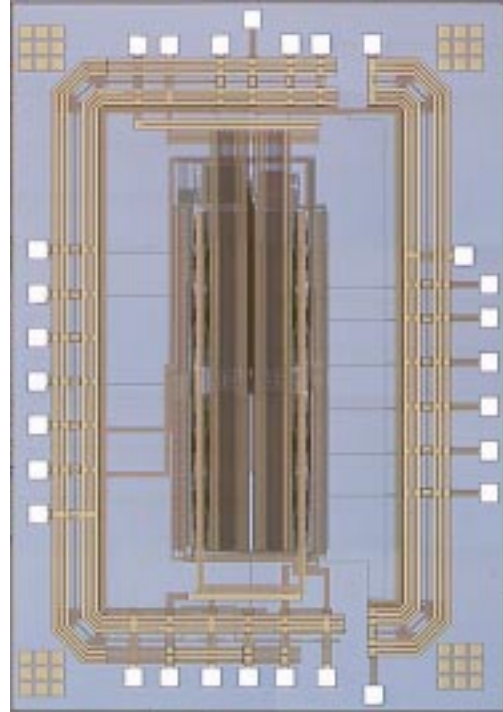


Fig 8 Die Photo

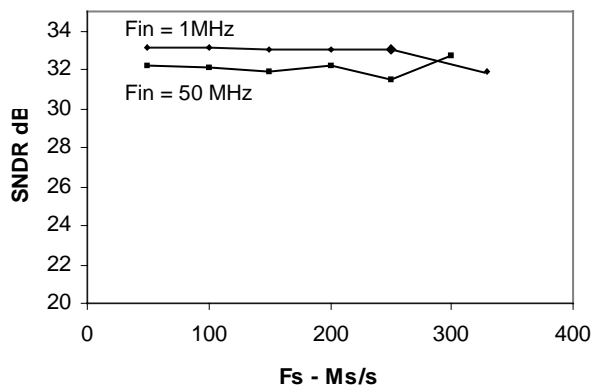


Fig. 9. SNDR versus sampling frequency for $F_{in} = 1\text{MHz}$ and 50MHz

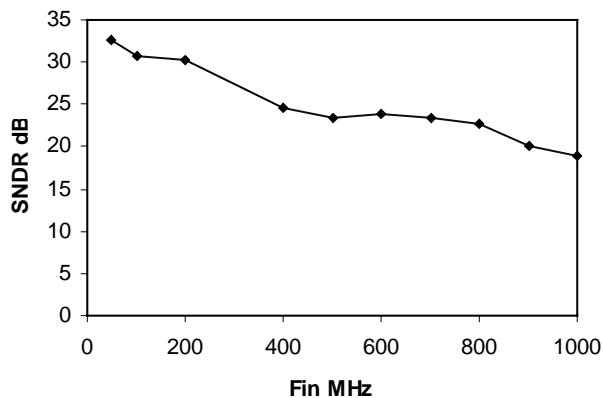


Fig. 10. SNDR versus input frequency for $F_s = 300\text{Ms/s}$

Fig. 9 shows the variation of measured SNDR with sampling rate for a full power input sinusoid at 1MHz and 50MHz. At 300Ms/s with a 50MHz input, the measured SNDR corresponds to 5.2 effective bits of resolution.¹ Fig. 10 shows the variation of measured SNDR versus input frequency with the sampling rate at 300Ms/s. With a 200MHz input the measured SNDR is in excess of 30dB. It can be seen that SNDR degrades gracefully with frequency.

The specifications are summarized in table 1. At 300Ms/s the device dissipates 110mW from a 2.2V supply. In terms of power per Ms/s, the prototype compares favorably with most recently-published devices (e.g. [2],[3] and [5]) Over a 12 hour period of continuous operation, without re-calibration, the SNDR varied by less than 0.1dB. All parts tested to date are completely functional.

¹ During evaluation, sampling speed was limited by the maximum speed of the clock source (330MHz) and not by the speed of the converter itself.

Conclusion

The calibration technique presented here effectively breaks the link between comparator offset and performance for flash converters. The comparators are designed for speed and power efficiency, without the constraint of analog matching. The architecture should scale easily to finer geometry processes. Because the converter is dominated by the digital circuitry, the performance and power consumption will improve. After an initial calibration the converter can operate continuously without re-calibration.

Acknowledgements

We thank TSMC for fabricating the prototype. The authors acknowledge the assistance of P. Walsh, F. Quinlan, D. Foley, and J. Ryan.

Table I
Measured ADC Characteristics

Resolution	6bits
LSB size	15mV
Input capacitance	1.2pF
Latency	2.5cycles
Package	28 pin Ceramic LCC
Supply	2V to 2.8V
Power at 300Ms/s	110mW
Area	1.2mm ²
Process	0.25 μm digital CMOS

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