

A Low-power 8-PAM Serial-Transceiver in 0.5 μ m digital CMOS

David J. Foley^{1,2} and Michael P. Flynn^{1,2}

¹Parthus Technologies plc., Cork, Ireland.

²National Microelectronics Research Centre, Dept. of Microelectronics, National University of Ireland at Cork, Ireland.

Abstract

A CMOS multi-level (8-PAM) transceiver is described. Pre-emphasis is implemented without an increase in DAC resolution or digital computation. The receiver oversamples with three fully differential 3-bit ADCs. The device transmits at up to 1.3Gb/s and has a measured BER of $<10^{-13}$ for an 810Mb/s PRBS transmission. The device, packaged in a 68 pin CLCC, is implemented in 0.5 μ m digital CMOS, occupies 2mm² and dissipates 400mW from a 3.3V supply.

Introduction

To reduce both pin and PCB track count, there is a growing demand for high speed serial transmission between ICs. The serial transceiver described in this paper employs multi-level signaling (8-PAM). For a given data rate, this 8-PAM scheme reduces the channel symbol rate to one third of that of a conventional 2-PAM approach [1]. The 2mm² transceiver was fabricated on a generic 0.5 μ m CMOS process and consumes 400mW at 1-Gb/s from a 3.3V supply. This circuit compares favorably in terms of reduced area to [1](1Gb/s, 0.5 μ m CMOS, 450mW, 4mm²) and [2](8Gb/s, 0.3 μ m CMOS, 1.1W, 4mm²).

Architecture and circuit design

A. Multi-level Transceiver

In Fig. 1 two ICs are communicating to each other using the 8-PAM transceiver circuitry. A 3-bit DAC in *chip-A* generates the 8-PAM output. Three interleaved ADCs and a data selection engine in *chip-B* decode the transmitted data. Clock phases for the transmitter and receiver are derived from a low-speed system or board clock. In the receiver a low-jitter DLL-based synthesizer generates clock phases $ck_{<3:1>}$, at 3 times the reference frequency, for the three receive ADCs. The DLL is self-correcting [3], it will not false lock to a multiple of clock periods. This allows the transceiver to be used for a range of data frequencies. A similar synthesizer generates a clock for the transmitter. The DLL filter capacitor is on chip. The data selection engine selects the ADC output that is closest to the center of the data eye.

Fig. 2 shows the transceiver in more detail. In addition to the transmit DAC, the transmitter incorporates a pre-emphasis

block, generating pre-emphasis for both step-up and step-down code changes. (Pre-emphasis compensates for the limited bandwidth of the package leads and link media). Baseline wander and gain compensation are performed in the receiver. The transceiver also contains a 3-bit fixed pattern generator and a $2^{10}-1$ PRBS generator and verifier for BIST.

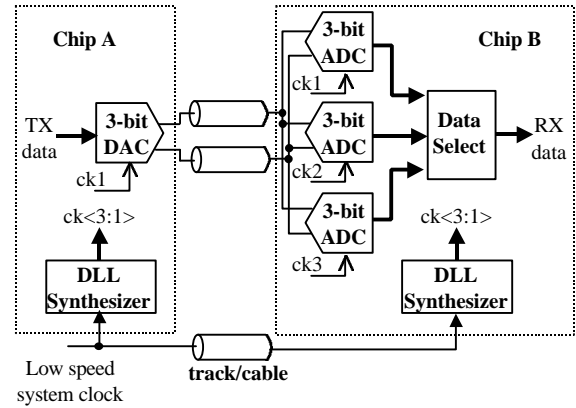


Fig. 1 Two ICs employing the 8-PAM interface.

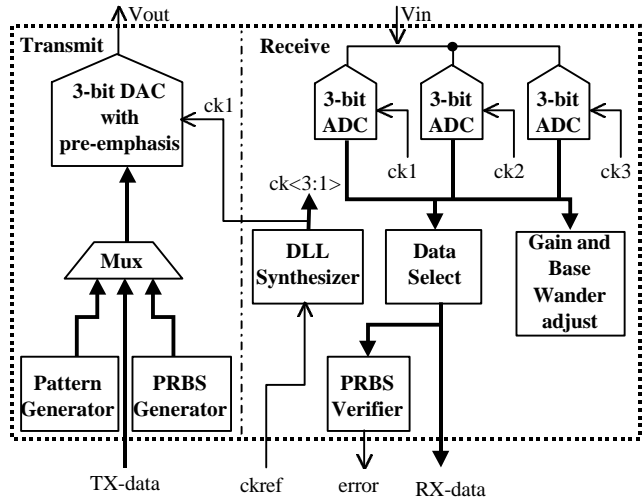


Fig. 2 Transceiver Block Diagram.

B. Transmitter

The transmitter is shown in more detail in Fig. 3(a). The output of the 3-bit current DAC is converted to an 8-PAM signal by the (off-chip) termination network. Pre-emphasis

might entail digital pre-processing and an increase in the resolution of the DAC – this approach was judged too slow and power hungry in this application, particularly in $0.5\mu\text{m}$ CMOS. Instead, pre-emphasis is implemented with two auxiliary DACs (NDAC and PDAC). While active, NDAC generates a current proportional to the present symbol value. Similarly, PDAC generates a current of opposite polarity, proportional to the previous symbol. In this way a pre-emphasis pulse is generated that is proportional to the change in the transmit code, but without any digital computation. The reference current for NDAC and PDAC, as well as the pre-emphasis pulse-width are programmable, allowing the transceiver to communicate over a range of track and cable lengths. To further illustrate this transmitter concept, an idealized output waveform with pre-emphasis is shown in Fig. 3 (b).

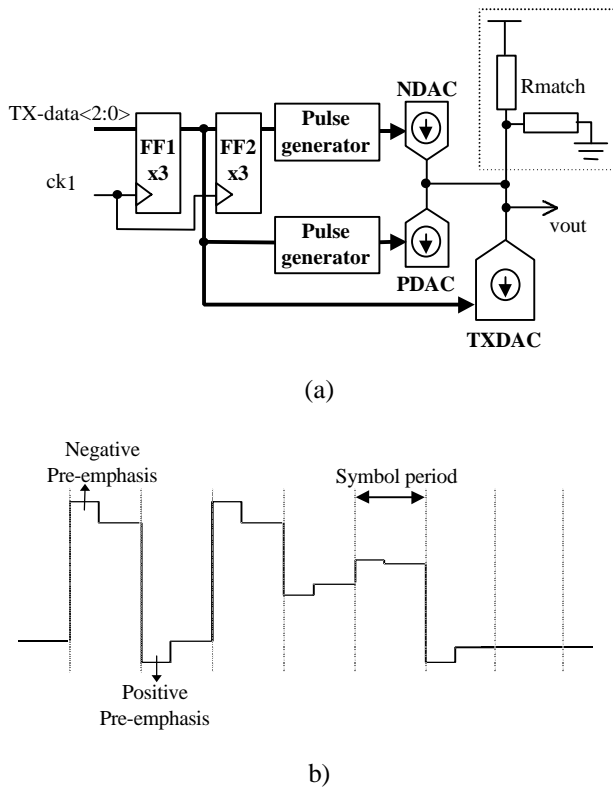


Fig. 3 (a) Transmitter Block Diagram, (b) Typical output waveform.

C. Receiver

A block diagram of the receiver ADC is presented in Fig. 4. For clarity the converter is shown with single-ended comparators, but in practice it accepts a differential input. The resistor ladder is shared by the three flash ADCs. Each ADC consists of 7 comparators, and incorporates 4-level bubble suppression logic and thermometer decode logic. The comparator is shown in Fig. 5. This circuit is similar to that in [4] but is modified to accommodate both a differential reference and a differential input. The comparator is driven

by non-overlapping clocks $F1$ and $F2$. P-channel MOSFETs, MP1 and MP2, are added to reduce kick-back into the ladder and input signal. The comparator MOSFETs are sized to minimize V_T mismatch, removing the necessity to auto-zero.

The receiver can be compensated for a gain error or a common mode offset in the transmitted signal. The reference voltage for the ladder, V_{base} , is set by a programmable current, I_{base} , and an external resistor, R_{ext} . The current in the ladder, I_{gain} , is also programmable permitting modification of the ADC gain. Two extra comparators are included to allow calibration of V_{base} and I_{gain} . During calibration a zero code is transmitted. The on-chip current sink, I_{base_int} , which is added to the external component of I_{base} , I_{base_ext} , is increased until the *over* control signal is activated. In a similar manner I_{gain} is calibrated by transmitting a full-scale code. The on-chip current sink, I_{gain_int} , is increased until the *under* control signal is activated.

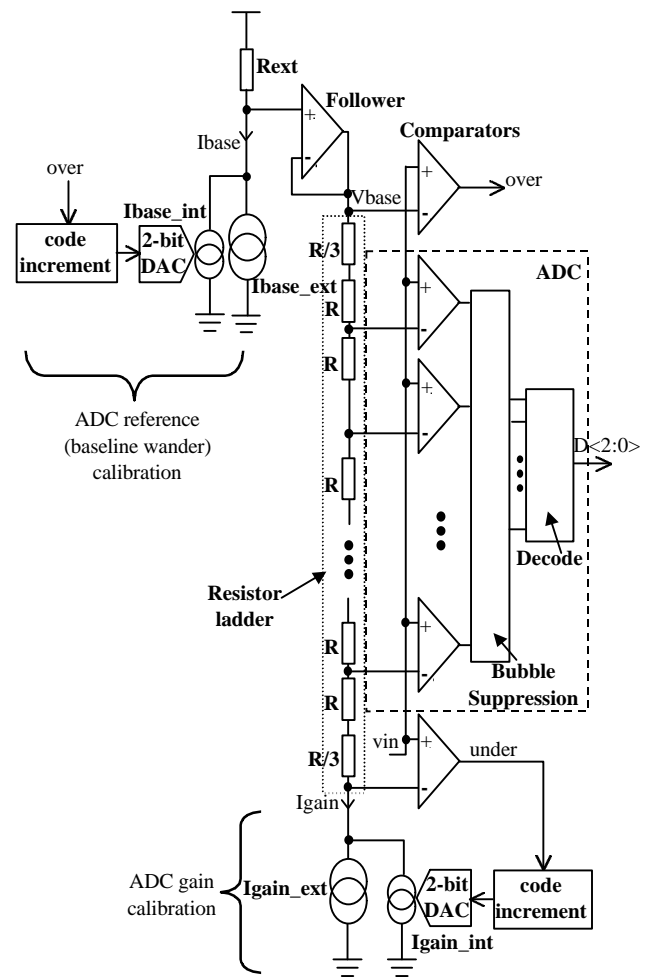


Fig. 4 Receiver ADC Block Diagram

D. DLL Synthesizer

The clock synthesizer employs a self-correcting DLL [3], which overcomes problems of false locking associated with conventional DLLs. A self-correcting circuit detects when the DLL is locked, or is attempting to lock, to an incorrect delay and then brings the DLL into a correct locked-state. Fig. 6 shows a simplified view of the block diagram for the DLL based synthesizer. The nine DLL output phases, $\phi(1:9)$, are combined in optimized AND-OR structures to generate the three clocks, $ck<3:1>$. These three clocks are phase separated by one ninth of a reference clock period and have a frequency three times that of the reference clock.

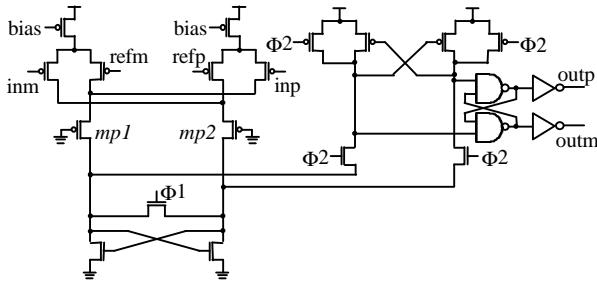


Fig. 5 Comparator schematic

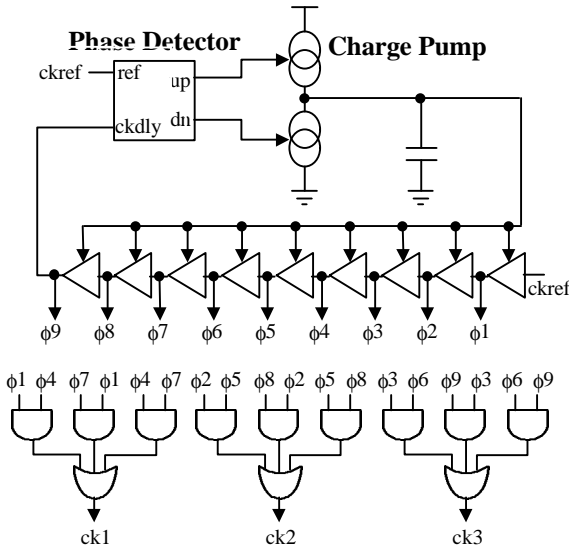
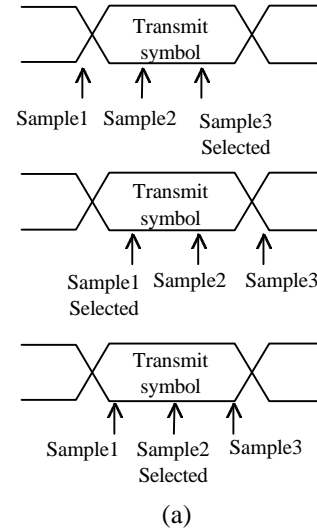


Fig. 6 DLL Synthesizer Block Diagram.

E. Data selection

The receiver takes three samples during each symbol period. One of the 3-bit outputs from the three sampling ADCs is selected as the received data word. The position of the center of the symbol-eye is re-determined during each symbol period. Fig. 7 shows how the sample closest to the centre of the eye is chosen, depending on the location of the code transition for these three samples. This algorithm requires that at least two of the three samples are identical. If all three

samples are different, then the center cannot be identified. In this case, the center position identified for the previous symbol is adopted.



Transition between samples		Select Sample
1 & 2	2 & 3	
Yes	No	3
No	Yes	1
No	No	2
Yes	Yes	Previous

(b)

Fig. 7 (a) Sample selection examples, and (b) Selection algorithm.

Measured Results

The chip photomicrograph is shown in Fig. 8. The transceiver has an active area of 2mm^2 and was fabricated on a generic $0.5\mu\text{m}$ CMOS process. The prototype is capable of a maximum 8-PAM data transmission rate of 1.3Gb/s , Fig. 9. For an 810Mb/s random data transmission no receive errors were detected in 1×10^{13} bits. An on-chip PRBS generator provided the random data for the transmitter. In addition to PRBS data, the self-test circuit can also generate a repetitive staircase pattern. Fig. 10 shows an 8-level transmitted staircase, as well as the 3 received data bits. For a transmitted 8-PAM repetitive staircase pattern, with an effective data rate of 1.1Gb/s , no receive errors were detected in 5×10^{13} bits.

The measured chip performance is summarized in Table I. The device consumes 400mW from a 3.3V supply. The DLL based clock synthesizer has a measured rms jitter of 3.2ps .

A 4-PAM serial transceiver of similar architecture was also prototyped. Similar bit error rates were achieved for this

circuit. A critical part of both designs is the pre-emphasis circuit in the transmitter. The advantage of the pre-emphasis can be appreciated by looking at the 500Mb/s 4-PAM transmission data eye diagrams in Fig. 11(a) without pre-emphasis and in Fig. 11(b) with pre-emphasis.

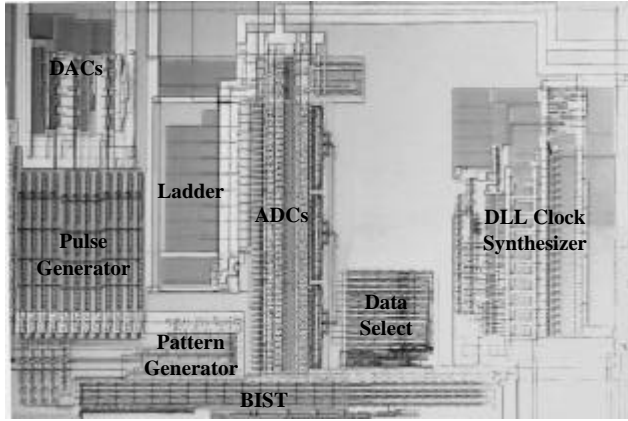


Fig. 8 Transceiver Die Photo.

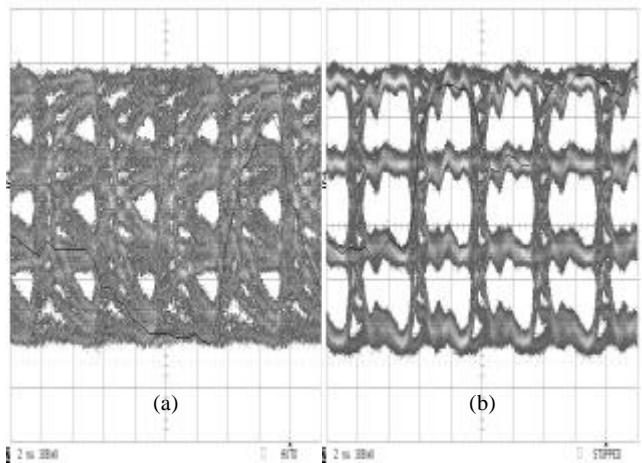


Fig. 11 500Mb/s 4-PAM transmission eye-diagrams (a) without pre-emphasis and (b) with pre-emphasis.

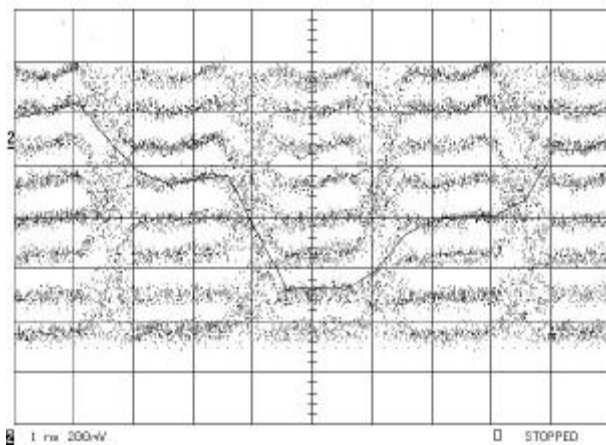


Fig. 9 1.3Gb/s transmission eye diagram

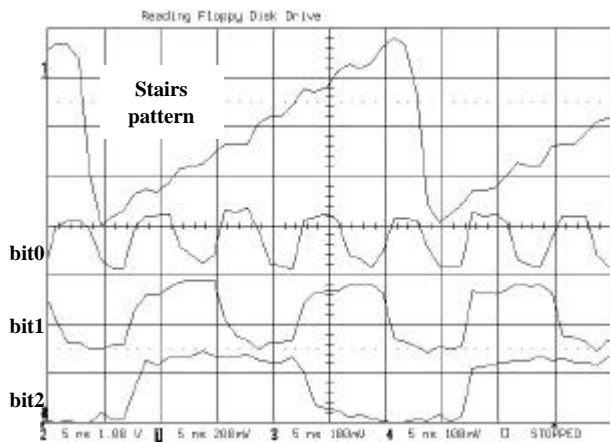


Fig. 10 810Mb/s transmitted stairs pattern and recovered data.

Acknowledgements

The authors thank John Ryan for his helpful suggestions and also acknowledge contributions from Sean Mullins, Pierce Mullarney, Ben Kinsella, Anne O'Connell, Pat Conlon, Finbarr Quinlan, Per Christian Andresen (Nordic VLSI), and ESM.

Table I

Measured Transceiver Characteristics

PAM levels	8 (and 4)
Synthesizer clock jitter	3.2ps (rms), 20ps (pk-pk)
PRBS BER (8 PAM) @ 810Mb/s over 6 inches of PCB track.	< 1 in 1×10^{13}
Periodic stairs pattern BER (8 PAM) @ 1.1Gb/s over 6 inches of PCB track.	< 1 in 1×10^{13}
Package	68 pin Ceramic LCC
Supply	2.8V to 3.3V
Power @ 1Gb/s, 3.3V	400mW
Die size	2mm^2
Process	0.5 μm digital CMOS
PCB	4-layer, FR4 type substrate

References

- [1] A. Fiedler, R. Mactaggart, J. Welch, S. Krishnan, "A 1.0625Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis", ISSCC Digest of Technical Papers, pp. 238-239, Feb. 1997.
- [2] R. Farjad-Rad, C. Ken Yang, M. Horowitz, T. Lee, "A 0.3 μm CMOS 8-Gb/s 4-PAM Serial Link Transceiver", IEEE JSSC, vol. 35, pp. 757-764, May 2000.
- [3] D. Foley and M. Flynn, "CMOS DLL Based 2V, 3.2ps Jitter, 1GHz Clock Synthesizer and Temperature Compensated Tunable Oscillator", in Proc. of CICC, pp. 371-374, May 2000.
- [4] G. Yin, F. Op't Eyende, W. Sansen, "A High-Speed CMOS Comparator with 8-b Resolution", IEEE JSSC, vol. 27, pp. 208-211, Feb. 1992.