

Mikhail Smelyanskiy

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Research Interests

- ILP Compiler Optimizations
- Exact (Integer Programming) Solutions to Compiler Optimizations
- Application-Specific Processor Design
- Computer Systems Modeling and Performance Estimation

Education

Ph.D. Computer Science and Engineering

The University of Michigan

6/2003 (expected)

Ann Arbor, MI

M. S. E. Computer Science and Engineering (7.7/8.0)

The University of Michigan

1/1999

Ann Arbor, MI

- Advanced Compilers (583)
- Compiler Construction (483)
- Computer Architecture (470, 370)
- Parallel Computer Architecture (570)
- Distributed Systems (593)
- Advanced Database Systems (584)
- Computer Networks (489)
- Algorithms (586)
- Numerical Linear Algebra (571)

B. S. E. Computer Science and Engineering (3.7/4.0)

The University of Michigan, Dearborn

1/1996

Dearborn, MI

Department of Applied Mathematics

Odessa State University

8/1989 to 8/1991

Odessa, Ukraine

Professional Experience

Research Assistant and Intel Graduate Fellow

The University of Michigan

1/1999-Present

Ann Arbor, MI

- Designed and implemented Trimaran predicate-aware instruction scheduling and architecture framework to reduce resource constraints in embedded applications
- Proposed and evaluated novel hardware mechanism called Register Queues to dramatically reduce register requirements in software pipelined loops
- Developed and evaluated probabilistic models of superscalar out-of-order processor performance

Graduate Student Instructor

The University of Michigan

8/2002-12/2002

Ann Arbor, MI

- Taught Introduction to Computer Organization course

Summer Intern

IBM Research, T.J. Watson Research Center

5/2001 to 8/2001

Yorktown Heights, NY

- Developed and implemented an analytical model of the out-of-order superscalar processor performance to characterize the benefits of out-of-order processing

Summer Intern

IBM Research, T.J. Watson Research Center

6/1999 to 8/1999

Yorktown Heights, NY

- Designed and implemented a modeling toolkit ACME (A Chip Multiprocessor Evaluator) for evaluating scalability issues and performance trade-offs of single chip multiprocessor architectures on loop-intensive benchmarks

Research Assistant

The University of Michigan

1/1997-12/1999

Ann Arbor, MI

- Characterized, tuned and optimized the performance of several large electromagnetics applications on the variety of message-passing, shared-memory and vector supercomputers, such as IBM SP2, SGI Origin 2000 and Cray C90

Summer Intern, Sparc Optimization/Code Generation Department 6/1998 to 8/1998
Sun Microsystems Menlo Park, CA

- Modified LCC compiler to recognize parallel ('future'-based) extensions to C
- Developed and implemented parallel run-time library

Ford College Graduate 1/96 to 1/97
Ford Motor Company Dearborn, MI

- Participated in the design and implementation of Ford's software development projects, including data analysis and visualization tools

Fall Intern 8/95 to 12/95
Argonne National Laboratory Argonne, IL

- Designed and implemented an efficient numerical domain-decomposition system for the solution of singularly perturbed boundary value problems.

Summer Intern, CAD/CAM Department 6/95 to 8/95
Ford Motor Company Dearborn, MI

- Designed and implemented an efficient algorithm to interactively build fillets (smooth-contoured surfaces) where parametric B-spline surfaces meet

Publications

- M. Smelyanskiy, S.A. Mahlke, E.S. Davidson, and H.S. Lee, "Predicate-aware Scheduling: A Technique for Reducing Resource Constraints," To appear in *Proceedings of the Annual IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, San Francisco, California, March, 2003.
- H.S. Lee, C.J. Newburn, M. Smelyanskiy, and G.S. Tyson, "Optimizing Memory Subsystem Designs by Exploring Region Reference Characteristics," To appear in *IEEE Transactions on Computers*.
- G. Tyson, M. Smelyanskiy and E.S. Davidson, "Evaluating the Use of Register Queues in Software Pipelined Loops," In *IEEE Transactions on Computers*, Vol, 50, No. 8, pp. 769 - 783, August, 2001.
- H.H. Lee, M. Smelyanskiy, C.J. Newburn and G. Tyson, "Stack Value File: Custom Microarchitecture for the Stack," In *Proceeding of the 7th IEEE International Symposium on High Performance Computer Architecture (HPCA-7)*, pp.5-14, Monterrey, Mexico, January, 2001.
- M. Smelyanskiy, G. Tyson and E.S. Davidson, "Register Queues: A New Hardware/Software Approach to Efficient Software Pipelining," In *Proceedings of International Conference on Parallel Architectures and Compilation Techniques (PACT 2000)*, pp.3-12, Philadelphia, Pennsylvania, October, 2000.
- M. Smelyanskiy, J.L. Volakis and E.S. Davidson, "Performance Optimization of an Integral Equation Code for Jet Engine Scattering on CRAY-C90," In *Applied Computational Electromagnetics Society Journal (ACES)*, Vol. 13, No.2, pp. 116-130, August, 1998.
- H.T. Anastassiou, M. Smelyanskiy, S. Bindiganavale and J.L. Volakis, "Scattering from Relatively Flat Surfaces using the Adaptive Integral Method AIM," In *Radio Science*, Vol. 33, No. 1, pp. 7-16, January-February, 1998.

Computer Skills

- Languages: C/C++, Fortran77/90, Yacc, Lex, Perl, csh/sh
- Message-passing libraries: MPI, PVM
- Hardware Design: Verilog
- Operating Systems: Unix, MS Windows

Citizenship

US citizen

Academic Advisors

Professor Edward S. Davidson
davidson@umich.edu
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Assistant Professor Scott A. Mahlke
mahlke@umich.edu
Tel: (734)936-1602

Additional references will be provided on request