



A Power Analyzer for Pocket Computers



First Site Visit. Sept. 25, 2000, Ann Arbor, Michigan

- Attendees
- DARPA: Bob Graybill, Jon Hiller
- AFRL/IFSC: Marvin Soraya, John Ostgaard
- Michigan: Todd Austin, Trevor Mudge⁺, Nam Kim, Jeff Ringenberg, Dan Ernst*, Dave Greene*, Kris Flautner*, Matt Postiff*, Dave Greene*
- Colorado: Dirk Grunwald, Soraya Ghiasi, Jason Casmira*
- Intel: George Cai

+nCoTec Ventures

•other support

Advanced Computer Architecture Lab
University of Michigan





Today's Schedule



- Introduction – Trevor Mudge
- SimpleScalar and StrongARM simulator – Todd Austin
- Component Modeling – Soraya Ghiasi, Nam Park, Jeff Ringenberg
- Voltage Scheduling – Dirk Grunwald
- Lunch
- Related work
 - Threads and power – Kris Flautner
 - Voltage clustering – Jason Casmira
 - Compiler-architecture – Matt Postiff/Dave Greene
- Future plans and changes – Trevor Mudge
- Demos – iPaq, SimpleScalar
- Thoughts on Landwarrior
- Wrap up





Introduction



- **Deliverable: PowerAnalyzer**
- **A power aware cycle-level simulator**
- **Make power a 1st class design consideration like performance**
- **Initial target**
 - **pocket computers where computing and communication place strong demands on the portable power supply.**
- **PowerAnalyzer will calculate dynamic and static power consumption profiles that can be used to measure the impact of power/performance trade-offs for complete systems that include processors, memories and peripherals.**





Related grants and contracts



- Power modeling – Intel
- ARM backend/ Verilog ARM model – DARPA compression
- Voltage scaling – NSF
- CADRE - NSF





Funding profile



- **Period 1: Jul00-Dec00**
- **Period 2: Jan01-Dec01**
- **Period 3: Jan02-Jun02**
- **Faculty**
 - 2 at Michigan
 - 1 at Colorado
- **Students**
 - Michigan: P1 2 - P2 3 - P3 4
 - Colorado: P1 2 - P2 2 - P3 2
- **Equipment**
 - NI Data Acquisition P2
 - 2 PC's P2





Timeline





What's been accomplished



- **Functioning simulator**
- **Component design underway**
- **Implemented clock scheduling – en route to full voltage scheduling**
- **Clustered voltage scaling – out of sequence**
- **SA-1100 simulator underway**
- **O/S simulator underway**

