EECS 373
Design of Microprocessor-Based Systems

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Lecture 4: Memory-Mapped I/O, Bus Architectures
September 11, 2014

Slides developed in part by
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Today…

Memory-Mapped I/O

Example Bus with Memory-Mapped I/O

Bus Architectures

AMBA APB

Memory-mapped I/O

- Microcontrollers have many interesting peripherals
  - But how do you interact with them?
- Need to:
  - Send commands
  - Configure device
  - Receive data
- But we don’t want new processor instructions for everything
  - Actually, it would be great if the processor know anything weird was going on at all

Memory-mapped I/O

- Instead of real memory, some addresses map to I/O devices instead

Example:

- Address 0x80000004 is a General Purpose I/O (GPIO) Pin
  - Writing a 1 to that address would turn it on
  - Writing a 0 to that address would turn it off
  - Reading at that address would return the value (1 or 0)

Smartfusion Memory Map

Memory-mapped I/O

- Instead of real memory, some addresses map to I/O devices instead
- But how do you make this happen?
  - *MAGIC* isn’t a bad guess, but not very helpful

Let’s start by looking at how a memory bus works

Today…

Memory-Mapped I/O

Example Bus with Memory-Mapped I/O

Bus Architectures

AMBA APB

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Bus terminology

- Any given transaction have an "*initiator*" and "*target*"
- Any device capable of being an initiator is said to be a "*bus master*"
  - In many cases there is only one bus master (*single master* vs. *multi-master*).
- A device that can only be a target is said to be a slave device.

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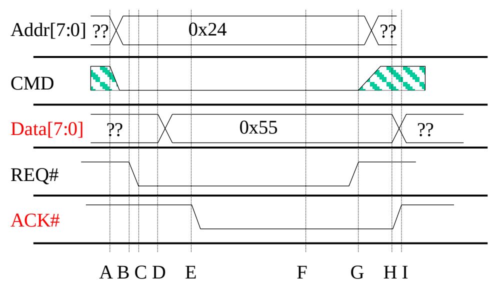
Basic example

Let's demonstrate a hypothetical example bus

- Characteristics
  - Asynchronous (no clock)
  - One Initiator and One Target
- Signals
  - Addr[7:0], Data[7:0], CMD, REQ#, ACK#
    - CMD=0 is read, CMD=1 is write.
    - REQ# low means initiator is requesting something.
    - ACK# low means target has done its job.

Read transaction

Initiator wants to read location 0x24



A read transaction

- Say initiator wants to read location 0x24
  A. Initiator sets Addr=0x24, CMD=0
  B. Initiator *then* sets REQ# to low
  C. Target sees read request
  D. Target drives data onto data bus
  E. Target *then* sets ACK# to low
  F. Initiator grabs the data from the data bus
  G. Initiator sets REQ# to high, stops driving Addr and CMD
  H. Target stops driving data, sets ACK# to high terminating the transaction
  I. Bus is seen to be idle

A write transaction

- Say initiator wants to write 0xF4 location 0x31
  A. Initiator sets Addr=0x24, CMD=1, Data=0xF4
  B. Initiator *then* sets REQ# to low
  C. Target sees write request
  D. Target reads data from data bus
     (only needs to store in register, not write all the way to memory)
  E. Target *then* sets ACK# to low.
  F. Initiator sets REQ# to high, stops driving other lines
  G. Target sets ACK# to high, terminating the transaction
  H. Bus is seen to be idle.

Returning to memory-mapped I/O

Now that we have an example bus, how would memory-mapped I/O work on it?

Example peripherals

0x00000004: Push Button - Read-Only

Pushed -> 1

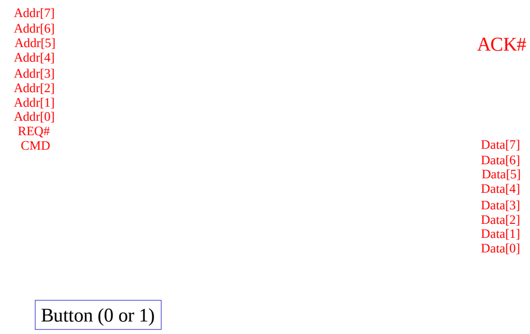
Not Pushed -> 0

0x00000005: LED Driver - Write-Only

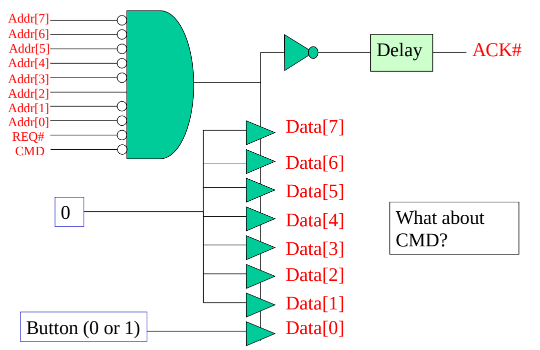
On -> 1

Off -> 0

The push-button (if Addr=0x04 write 0 or 1 depending on button)

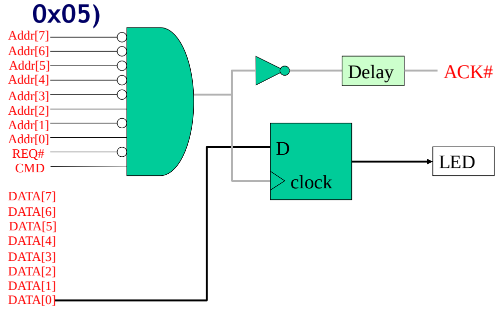


The push-button (if Addr=0x04 write 0 or 1 depending on button)



The LED (1 bit reg written by LSB of address 0x05)

The LED (1 bit reg written by LSB of address 0x05)



Let's write a simple assembly program Light on if button is pressed.

Peripheral Details

0x00000004: Push Button - Read-Only

Pushed -> 1

Not Pushed -> 0

0x00000005: LED Driver - Write-Only

On -> 1

Off -> 0

Today…

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Example Bus with Memory-Mapped I/O

Bus Architectures

AMBA APB

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Driving shared wires

- It is commonly the case that some shared wires might have more than one potential device that needs to drive them.
  - For example there might be a shared data bus that is used by the targets and the initiator. We saw this in the simple bus.
  - In that case, we need a way to allow one device to control the wires while the others "stay out of the way"
    - Most common solutions are:
      - using tri-state drivers (so only one device is driving the bus at a time)
      - using open-collector connections (so if any device drives a 0 there is a 0 on the bus otherwise there is a 1)

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Or just say no to shared wires.

- Another option is to not share wires that could be driven by more than one device…
  - This can be really expensive.
    - Each target device would need its own data bus.
    - That's a LOT of wires!
  - Not doable when connecting chips on a PCB as you are paying for each pin.
  - Quite doable (though not pretty) inside of a chip.

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Wire count

- Say you have a single-master bus with 5 other devices connected and a 32-bit data bus.
  - If we share the data bus using tri-state connections, each device has "only" 32-pins.
  - If each device that could drive data has it's own bus…
    - Each slave would need _____ pins for data
    - The master would need ______ pins for data
- Again, recall pins==$$$$$$.

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What happens when this "instruction" executes?

```
#include <stdio.h>
#include <inttypes.h>

#define REG_FOO 0x40000140

main () {
  uint32_t *reg = (uint32_t *)(REG_FOO);
  *reg += 3;

  printf("0x%x\n", *reg); // Prints out new value
}
```

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"*reg += 3" is turned into a ld, add, str sequence

- Load instruction
  - A bus read operation commences
  - The CPU drives the address "reg" onto the address bus
  - The CPU indicated a read operation is in process (e.g. R/W#)
  - Some "handshaking" occurs
  - The target drives the contents of "reg" onto the data lines
  - The contents of "reg" is loaded into a CPU register (e.g. r0)
- Add instruction
  - An immediate add (e.g. add r0, #3) adds three to this value
- Store instruction
  - A bus write operation commences
  - The CPU drives the address "reg" onto the address bus
  - The CPU indicated a write operation is in process (e.g. R/W#)
  - Some "handshaking" occurs
  - The CPU drives the contents of "r0" onto the data lines
  - The target stores the data value into address "reg"

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Details of the bus "handshaking" depend on the particular memory/peripherals involved

- SoC memory/peripherals
  - AMBA AHB/APB

- NAND Flash
  - Open NAND Flash Interface (ONFI)

- DDR SDRAM
  - JEDEC JESD79, JESD79-2F, etc.

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Why use a standardized bus?

- Downsides
  - Have to follow the specification
  - Probably has actions that are unnecessary
- Upside
  - Generic systems
  - Allows modules to be reused on different systems

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Today…

Memory-Mapped I/O

Example Bus with Memory-Mapped I/O

Bus Architectures

AMBA APB

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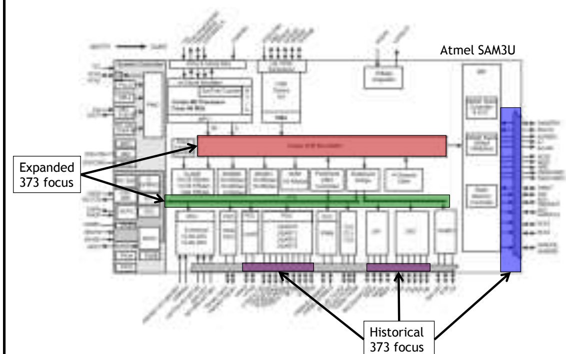
Modern embedded systems have multiple busses



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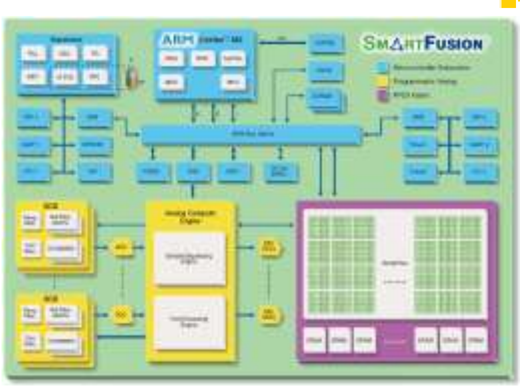
Actel SmartFusion system/bus architecture



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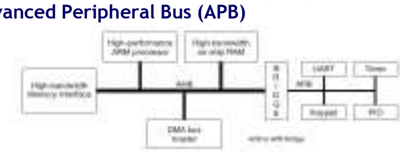
Advanced Microcontroller Bus Architecture (AMBA)
- Advanced High-performance Bus (AHB)
- Advanced Peripheral Bus (APB)



AHB
- High performance
- Pipelined operation
- Burst transfers
- Multiple bus masters
- Split transactions

APB
- Low power
- Latched address/control
- Simple interface
- Suitable of many peripherals

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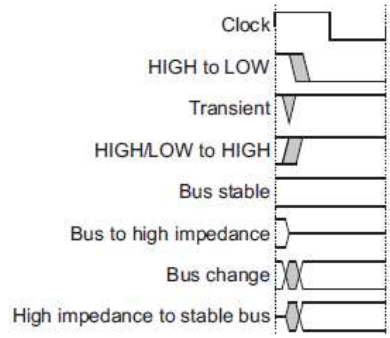
APB is a fairly simple bus designed to be easy to work with.

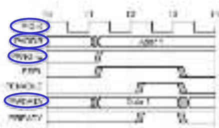
- Low-cost
- Low-power
- Low-complexity
- Low-bandwidth
- Non-pipelined
- Ideal for peripherals

Notation



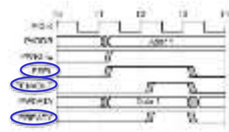
APB bus signals

- PCLK
  - Clock
- PADDR
  - Address on bus
- PWRITE
  - 1=Write, 0=Read
- PWDATA
  - Data written to the I/O device. Supplied by the bus master/processor.

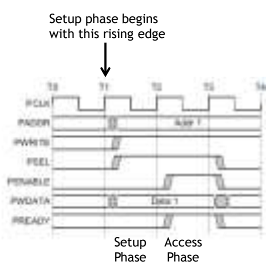


APB bus signals

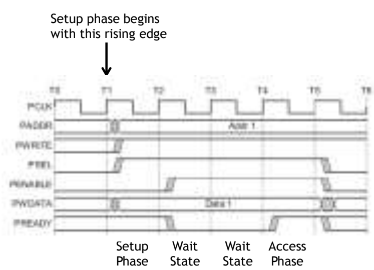
- PSEL
  - Asserted if the current bus transaction is targeted to ***this*** device
- PENABLE
  - High during entire transaction *other than* the first cycle.
- PREADY
  - Driven by target. Similar to our #ACK. Indicates if the target is *ready* to do transaction. Each target has it's own PREADY



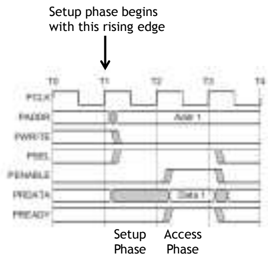
A write transfer with no wait states



A write transfer with wait states



A read transfer with no wait states



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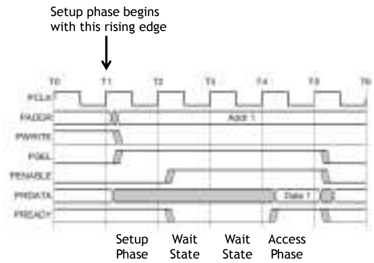
A read transfer with wait states



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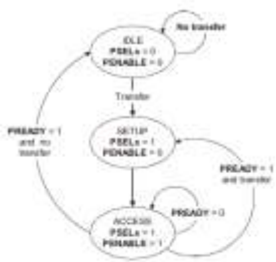
APB state machine

- IDLE
  - Default APB state
- SETUP
  - When transfer required
  - PSELx is asserted
  - Only one cycle
- ACCESS
  - PENABLE is asserted
  - Addr, write, select, and write data remain stable
  - Stay if PREADY = L
  - Goto IDLE if PREADY = H and no more data
  - Goto SETUP is PREADY = H and more data pending



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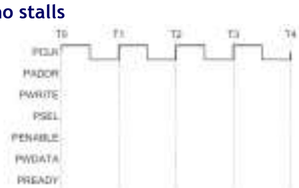
Example setup

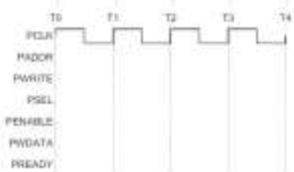
- For the next couple of slides, we will assume we have one bus master “CPU” and two slave devices (D1 and D2)
  - D1 is mapped to 0x00001000-0x0000100F
  - D2 is mapped to 0x00001010-0x0000101F

Say the CPU does a store to location 0x00001004 with no stalls

D1



D2



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Writes

Let’s do some hardware examples!

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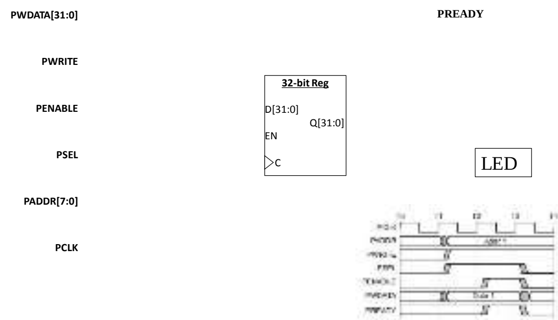
What if we want to have the LSB of this register control an LED?



We are assuming APB only gets lowest 8 bits of address here…

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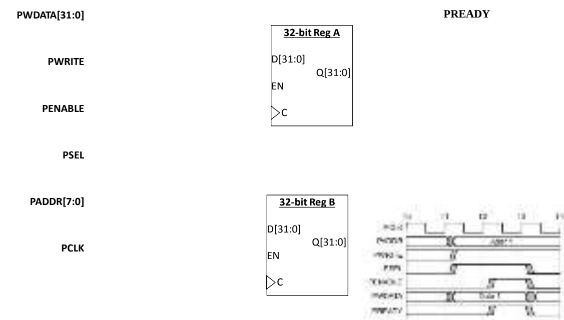
Reg A should be written at address 0x00001000
Reg B should be written at address 0x00001004



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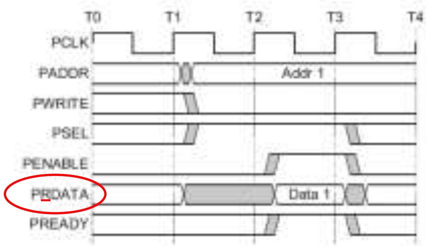
Reads…



The key thing here is that each slave device has its own read data (PRDATA) bus!

Recall that "R" is from the initiator's viewpoint—the device drives data when read.

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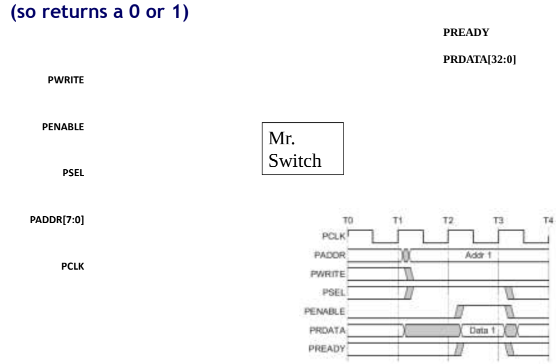
Let's say we want a device that <u>provides</u> data from a switch on a read to any address it is assigned. (so returns a 0 or 1)



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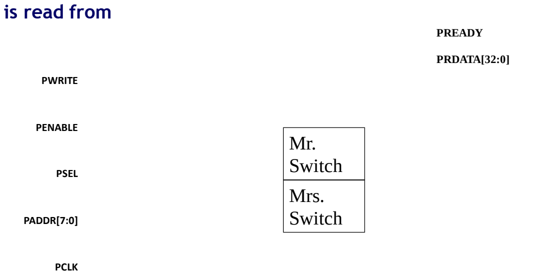
Device provides data from switch A if address 0x00001000 is read from. B if address 0x00001004 is read from



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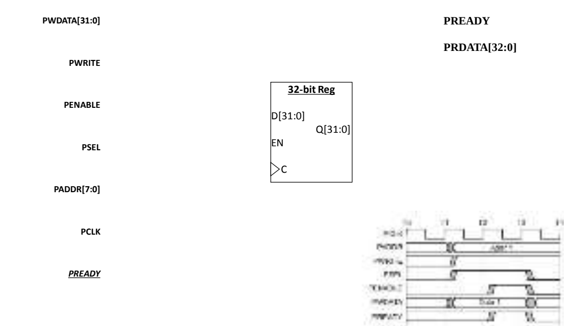
All reads read from register, all writes write…



We are assuming APB only gets lowest 8 bits of address here…

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Things left out…

- There is another signal, PSLVERR (APB Slave Error) which we can drive high if things go bad.
  - We'll just tie that to 0.
- PRESETn
  - Active low system reset signal
  - (needed for stateful peripherals)
- Note that we are assuming that our device need not stall.
  - We could stall if needed.
    - I can't find a limit on how long, but I suspect at some point the processor would generate an error.

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Verilog!

```
/*** APB3 BUS INTERFACE ***/
input PCLK,                    // clock
input PRESERN,                 // system reset
input PSEL,                    // peripheral select
input PENABLE,                 // distinguishes access phase
output wire PREADY,            // peripheral ready signal
output wire PSLVERR,           // error signal
input PWRITE,                  // distinguishes read and write cycles
input [31:0] PADDR,            // I/O address
input wire [31:0] PWDATA,      // data from processor to I/O device (32 bits)
output reg [31:0] PRDATA,      // data to processor from I/O device (32-bits)

/*** I/O PORTS DECLARATION ***/
output reg LEDOUT,             // port to LED
input SW                       // port to switch
);

assign PSLVERR = 0;
assign PREADY = 1;
```

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Questions?

Comments?

Discussion?

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