# Batch-Processed Vacuum-Sealed Capacitive Pressure Sensors

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***Abstract*—This paper reports two multitransducer vacuum-sealed capacitive barometric pressure sensors, one using single-lead and the other using multiple-leads to transfer the electrical signal out of the vacuum-sealed reference cavity. The first device operates with a resolution of 37 mtorr over a pressure range from 600 to 800 torr. The sensitivity is 27 fF/torr (3000 ppm/torr). The TCO at 750 torr is 3900 ppm/°C and the TCS is 1000 ppm/°C. The second device has a resolution of 25 mtorr over a range from 500 to 800 torr, with individual transducer sensitivity of 39 fF/torr. The TCO at 750 torr is 1350 ppm/°C and TCS is 1000 ppm/°C. Both devices have an on-chip compensation capacitor and are read out using an electronically-trimmed switched-capacitor charge integrator. [611]**

***Index Terms*—Capacitive sensor, MEMS, pressure, vacuum sealing.**

## I. Introduction

With an established market of $2.5B [1], pressure sensors are among the most important MEMS devices, with applications in areas such as automotive systems, industrial process control, medical diagnostics, and environmental monitoring (including distributed weather forecasting networks). While a majority of the silicon pressure transducers in use today are piezoresistive, capacitive devices have become the focus for most new developments to achieve higher pressure sensitivity, lower temperature sensitivity, and reduced power consumption. The sensors described here are multitransducer capacitive devices suitable for barometric applications [2]. They have a wide dynamic range (500–800 torr) as well as very high resolution (25 mtorr, equivalent to an altitude difference of about one foot at sea level). These requirements are especially challenging because this resolution must be maintained over a temperature range from −25 °C to 85 °C. To meet this temperature range requirement it is essential that the effects of trapped gas expansion be eliminated [3] through the use of a vacuum-sealed reference cavity. This also results in a device with wider bandwidth by avoiding the damping effects associated with a gas-filled cavity [4]. The first device transfers a single lead (the electrode on the glass) from inside the cavity to the outside world. Parasitic capacitance in parallel with the sensor capacitance has a different thermal behavior than the actual sensing element and thus complicates temperature compensation. The second device has multiple signal transfer leads and significantly reduces such parasitics. During the development of these sensors, specific emphasis was put on making them suitable for planar batch processing and low cost applications. The devices described here are bonded at wafer level and avoid use of glass drilling, epoxy seals, or special metal seals [6], [7].

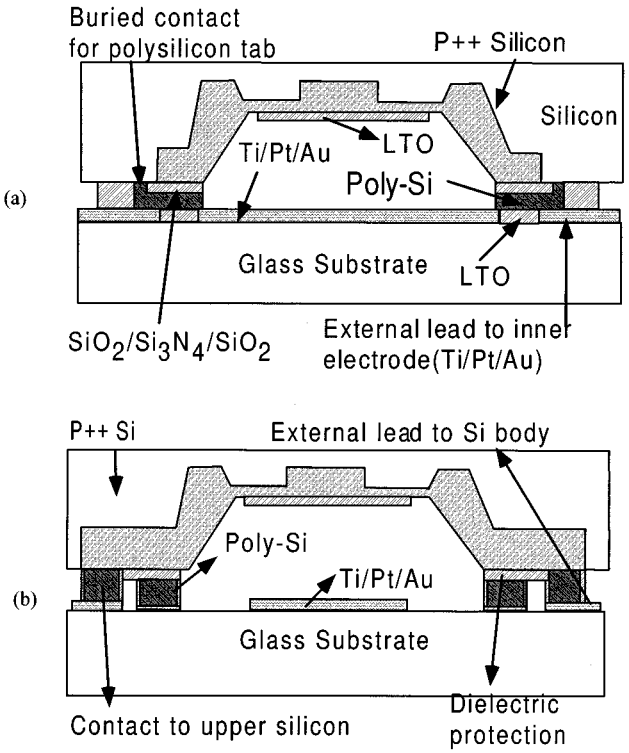


Fig. 1. Cross sections of the capacitive sensor using a single transfer lead from the sealed cavity. (a) The cut is shown through the lead transferring the glass electrode out of the cavity. A tab used to contact the wafer bulk during bonding is also shown. (b) The cut is shown along a device diagonal. The inner ring forms the vacuum seal; the outer ring provides a permanent contact to the silicon electrode.

## II. Single-Lead Transfer Sensor

The sensor cross-section is shown in Fig. 1 and consists of vacuum-sealed capacitors realized in a silicon-on-glass dissolved-wafer process. In bringing the glass electrode out from the reference cavity and sealing that cavity in vacuum, one approach is to bring the lead out using polysilicon embedded in a planarizing low temperature oxide (LTO) layer; a second level

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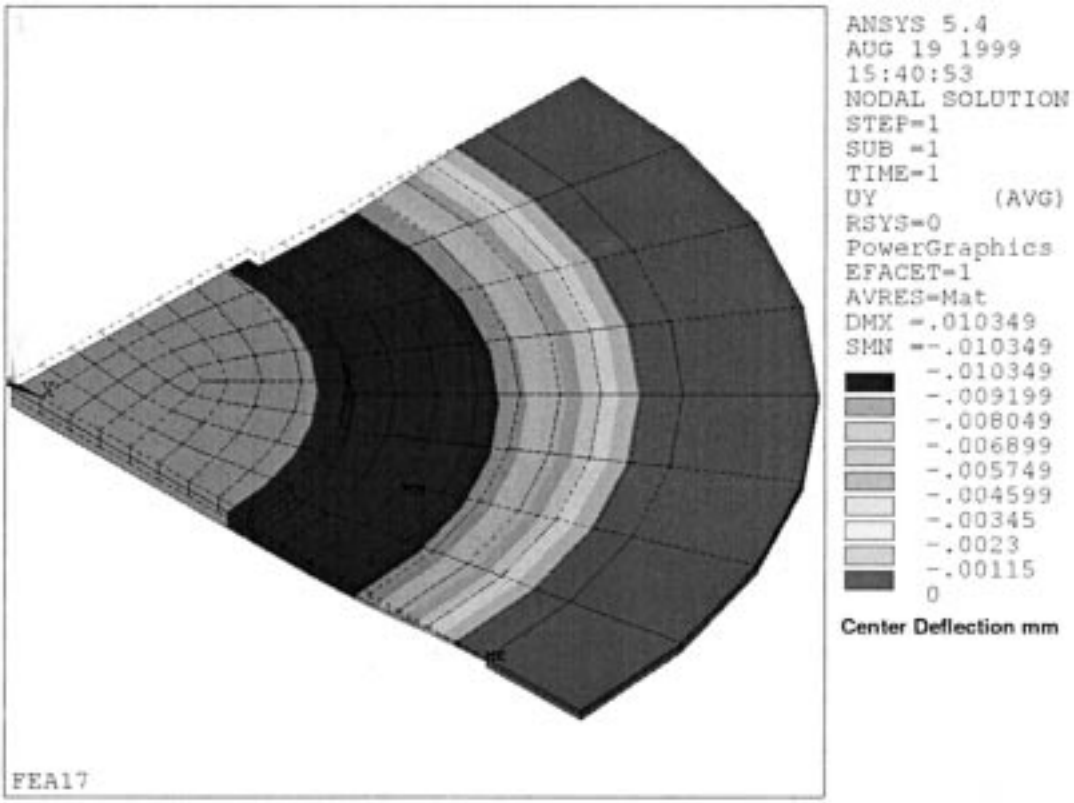


Fig. 2. FEA results for one quarter of a circular bossed diaphragm, showing center deflection for applied atmospheric pressure of 101 kPa.

of polysilicon could then be bonded to the glass substrate. Such seals are known to be hermetic [5]. In the device described here, these two polysilicon layers are collapsed into one layer that functions both as a lead transfer and as a sealing base for the cavity. As shown in Fig. 1(a), the internal sensing lead on the glass is transferred to the polysilicon and then back to metal externally using Pt–Pt bonds formed during the electrostatic bonding operation. Since the polysilicon must be electrically connected to the silicon bulk during bonding but must be well isolated later, lateral polysilicon tabs are used to contact to the lightly-doped portion of the bulk. This area is automatically removed during the etch-back process to provide the required isolation. Permanent contacts to the top silicon electrode are made via similar transfers to the p+ body region as shown in Fig. 1(b). Using this approach, the process flow is much simplified and wafer-level bonds can be made to both 7740 and Hoya SD2 glasses. In addition, since the vacuum seal is done at wafer level before etch-back, the cavity is never exposed to the etch and stiction problems are avoided.

The device has multiple transducers to segment the overall pressure range [2]. The diaphragm diameters vary from 920 to 1100 $\mu$m with a gap separation of $\sim$10 $\mu$m and a diaphragm thickness of $\sim$3 $\mu$m. The device is designed to operate with a resultant diaphragm tensile stress of about 25 MPa. The diaphragm design is done using the ANSYS finite element analysis tool. The center deflection, $z$, for a circular diaphragm with a rigid center can be obtained to a first order as [16]

$$P = \frac{Et^3}{A_p a^4}\, y + \frac{B_p E h}{a^4}\, y^3.$$

Here, $P$ is pressure, $E$ is the Young's modulus, $t$ is diaphragm thickness, $a$ is diaphragm radius, and $y$ is the center deflection. $A_p$ and $B_p$ are constants, which in this case are 0.1135 and 12.4059, respectively. In order to ensure that the diaphragm does not buckle under compressive stress, some residual tensile stress is present in the diaphragm and reduces the center deflection, $y$. The effect of this residual stress is not accounted for in the equation above. In case of heavily-boron-doped membranes compensated by a thin layer of oxide, this stress is about 25–30 MPa. Fig. 2 gives the finite element analysis (FEA) output, showing the center deflection with all the stress factors present for this diaphragm.

Fig. 3(a) shows a complete five-transducer sensor with an on-chip reference capacitor in the center of the lower row. Fig. 3(b) depicts a single transducer. A scanning electron micrograph (SEM) view of a single transducer is seen in Fig. 3(c).

## III. Single-Lead Fabrication Process

A compressed process flow is shown in Fig. 4. The device is fabricated using an eight-mask bulk-micromachined dissolved wafer process. The silicon processing starts with a KOH recess etch of about 9 $\mu$m. Small variations in this depth can be compensated in later dielectric deposition steps. A patterned masking oxide [see Fig. 4(b1)] is used to define the anchor area using a solid-source boron diffusion at 1175 °C. A nominal etch-stop depth of 15 $\mu$m is obtained. This is followed by a similar masked [Fig. 4(b2)] shallow boron diffusion step to define the diaphragm thickness at about 3 $\mu$m. This is followed by 0.08 $\mu$m dry thermal oxide grown in $O_2$ ambient to ensure capping of the boron diffused areas. Next, low-pressure chemical-

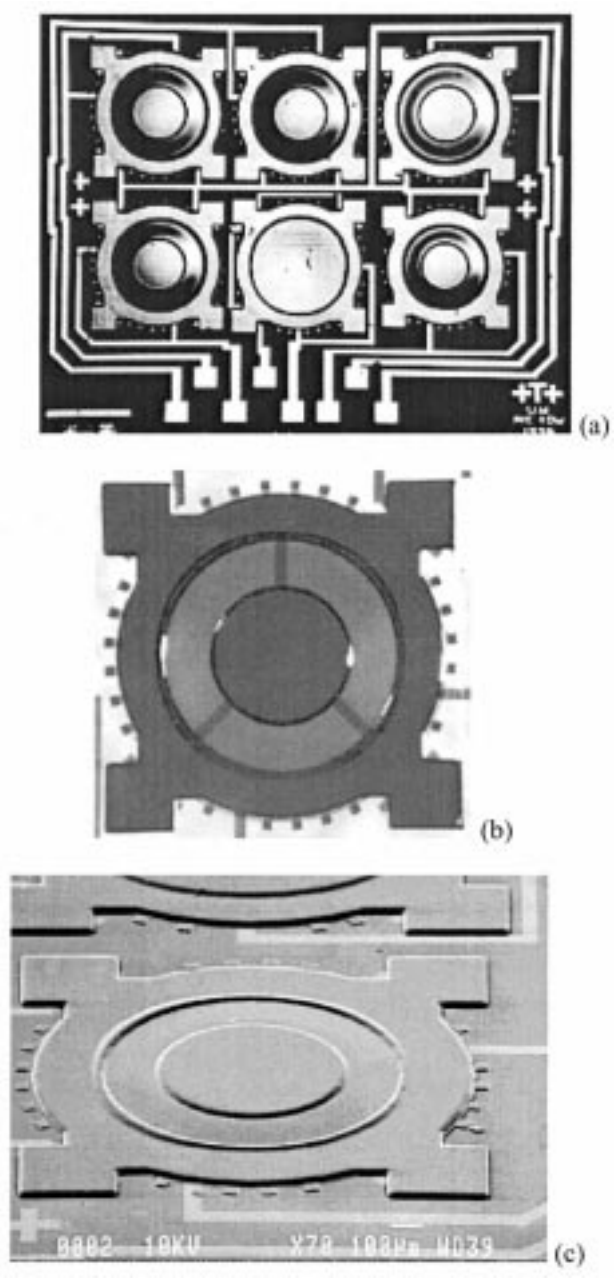


Fig. 3. Top views of the fabricated single-lead-transfer devices. (a) Five transducers are formed per die, having staggered diameters and pressure ranges. A reference capacitor can be seen in the center of the lower row. (b) A back-illuminated view of a single transducer is shown. (c) An SEM picture gives a three-dimensional view of the transducer.

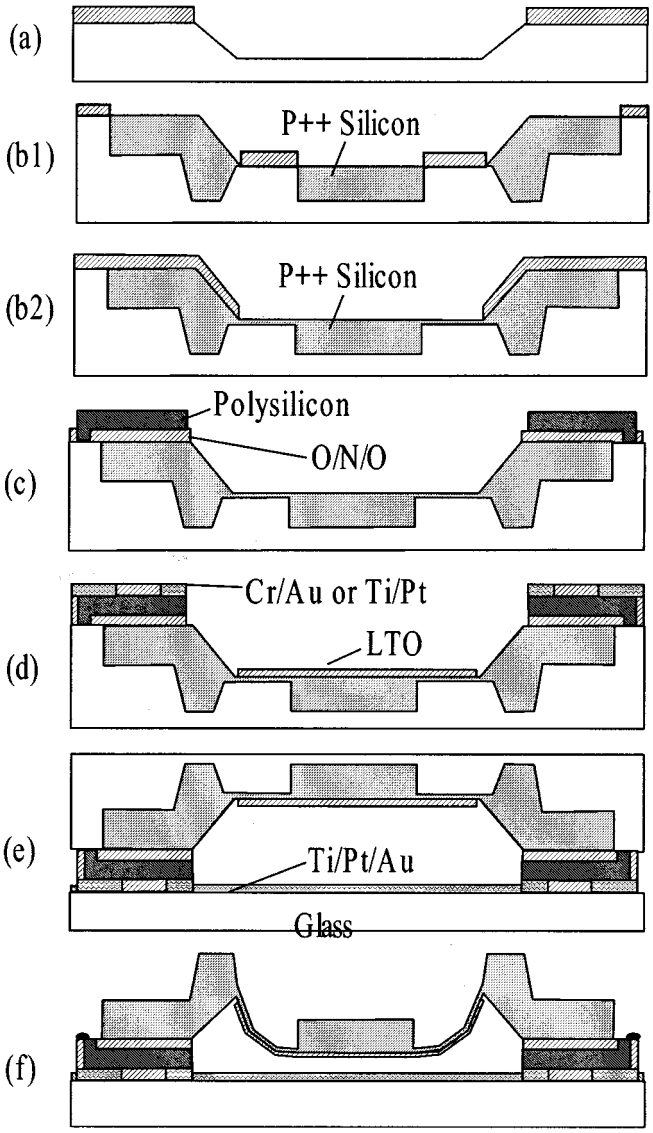


Fig. 4. Process flow for the vacuum-sealed capacitive pressure sensor.

vapor deposition (LPCVD) $SiO_2/Si_3N_4/SiO_2$ dielectrics with thickness of 0.3/0.15/0.3 $\mu$m are deposited. Contact openings are patterned to allow the subsequent 1.5 $\mu$m-thick polysilicon layer to make contact to the silicon bulk. After depositing the polysilicon, a short boron diffusion at 950 °C is done to reduce the resistance of polysilicon. This also reduces the rate of EDP attack if the protective dielectric coating on polysilicon is broken. Boron diffusion increases the surface roughness of polysilicon to between 80 nm–300 nm. An optional chemical–mechanical polishing (CMP) step can be used to achieve higher yield during vacuum bonding. The use of CMP reduces this roughness below 7 nm and also helps to overcome yield loss due to minor wafer bowing, which may occur in earlier high temperature steps. It is necessary to adopt proper cleaning procedures after CMP [8] to deal with heavy metals from the polishing slurry being embedded in the polished surface. Other options include using *in-situ* doped polysilicon [9], [10] or ion-implantation.

The polysilicon is patterned using an $SF_6$ plasma. The dielectric layer on the diaphragm area is then removed using wet etching. A 280-nm-thick LTO layer is deposited to protect the polysilicon from attack by EDP. The LTO layer on the diaphragm area also provides isolation for the two electrodes of the capacitor and stress compensation. The LTO layer is patterned to provide for contact openings. Ti–Pt is evaporated with the resist mask for the LTO contact opening still in place, followed by lift-off to provide contacts to the polysilicon with a total height of about 70 nm. This avoids any misalignment between the metal and the LTO contact opening. At this point the polysilicon is completely enclosed in a dielectric layer and has two metal contact areas. Due to the loss of some

polysilicon during boron diffusion and CMP, the total height of the dielectric layers and the polysilicon is about 2 $\mu$m. Thus, the total recess depth is 10.5 $\mu$m. This forms the working gap of the capacitor.

The glass processing consists of depositing 25/35/100 nm of a composite Ti-Pt-Au layer. The Au is then etched back in the areas that will contact the silicon. The glass is partially diced at this point so that the devices can be easily separated after the wafer dissolution step. Wafer-level anodic bonding to 7740 glass is next performed in vacuum ($1 \times 10^{-6}$ torr) [see Fig. 4(e)]. Due to poor heat transfer in vacuum, it is important to first heat the wafers to 400 °C at $1 \times 10^{-3}$ torr and then pump down the bonding chamber to vacuum levels. Preheating the wafers for 30 minutes helps the out-diffusion of gases from the inner-walls of the sealed cavity, which are subsequently evacuated via drainage areas between the cavities. The next step is to dissolve the wafer in EDP to obtain the final structure shown in Fig. 4(f). As can be seen, the diaphragm is heavily deflected under normal atmospheric conditions. After the devices were mounted on a test board, they were characterized and then coated with 110 nm of parylene. This makes device suitable for applications where condensation can be expected. The parylene coating increases the pressure sensitivity by 50 to 70 ppm/torr due to small compressive stresses in the parylene film.

## IV. Multilead Transfer Sensor

An alternative device structure with multiple stacked polysilicon and dielectric layers is employed in this sensor. Each transducer can have several lead transfers from the internal reference cavity to the outside world and provides additional Ti/Pt electrodes to block the electric field across the entire cavity and getter any outdiffusing oxygen ions. To achieve multiple leads, two levels of polysilicon are used. The seal is formed between the second level of polysilicon and the glass. Leak rate for polysilicon–glass seals is less than $1.1 \times 10^{-8}$ atm cm$^3$/s [18]. The sensor cross-section is diagrammed in Fig. 5 and consists of vacuum-sealed capacitors realized in a silicon-on-glass dissolved-wafer process. Two versions of the multilead transfer device were fabricated. In the structure shown in Fig. 5(a), the polysilicon-1 layer near the glass forms a continuous sealing ring while the polysilicon-2 layer forms a bridge for the individual lead transfers. Using this approach, wafer-level bonds can be made to 7740 glass. A second version of this device has a metal or polysilicon electrode on the p++ silicon diaphragm inside the cavity, which is isolated from the diaphragm electrically using an intermediate oxide layer. This eliminates the need to passivate the exposed p++ silicon surface in case of operation under moist and dirty conditions because the p++ housing forms only the physical transducer but is electrically isolated from the electrode. Fig. 5(c) shows a cross section of this scheme.

The overall pressure range is segmented similar to the single-lead transfer sensor using multiple transducers. In Fig. 5(a), the internal sensing lead on the glass is transferred to poly1 and then through a contact opening to poly2, back again to poly1, and then back to metal externally using Pt–Pt compression bonds formed during the electrostatic bonding operation.

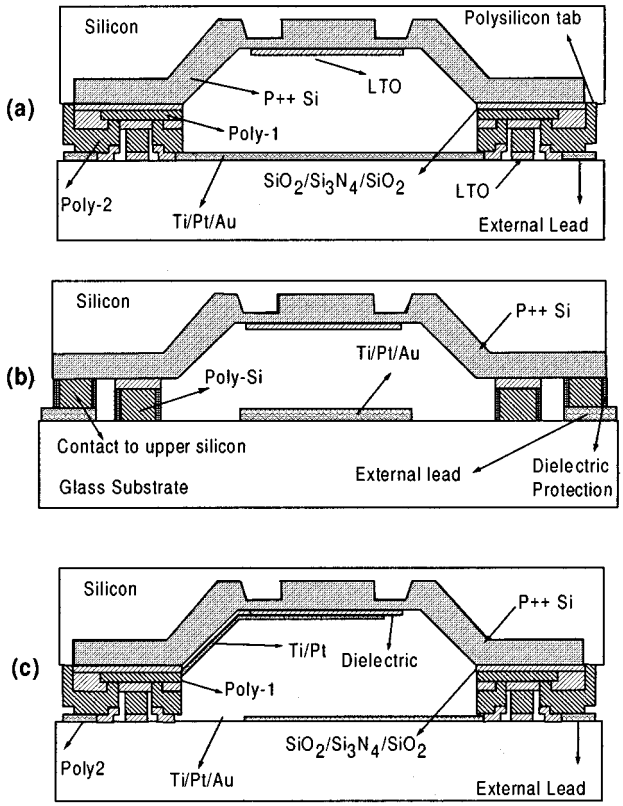


Fig. 5. Cross sections of the multilead capacitive sensor. (a) The cut is shown through the lead transfer that brings the glass electrode out of the cavity. A tab used to contact the wafer bulk during bonding is also shown. (b) The cut is shown along a device diagonal. The inner ring forms the vacuum seal; the outer ring provides a permanent contact to the silicon electrode. (c) Scheme showing the lead transfers with both electrodes isolated from the silicon bulk.

Lateral polysilicon tabs similar to the single-lead transfer device but formed from poly2, are used to create the bonding potential between the polysilicon and glass. The tab contact area is automatically removed during the etch-back process to provide the required isolation. Permanent contacts to the top silicon electrode are made via similar transfers to the p+ body region as shown in Fig. 5(b). In the case of a multilead device, the majority of the anchor formed by the polysilicon ring is electrically isolated from the leads themselves. Thus, it is important to be able to do probe (batch) testing to verify this isolation. Special contacts are provided to the rim to test for this isolation. Fig. 6(a) shows a complete five transducer sensor with an on-chip reference capacitor in the center of the lower row. This pressure-independent reference capacitor tracks the pressure dependent transducers over temperature and is used differentially with a switched-capacitor readout circuit. Fig. 6(b) views a single transducer, showing all lead transfers as seen through the glass.

## V. Multilead Fabrication Process

A compressed process flow for the multilead sensor is shown in Fig. 7. The device is fabricated using a ten-mask bulk-micromachined dissolved wafer process. As shown in Fig. 7(a), the silicon process starts with a KOH recess etch of about 7 $\mu$m. Subsequently-deposited layers can compensate for any variation

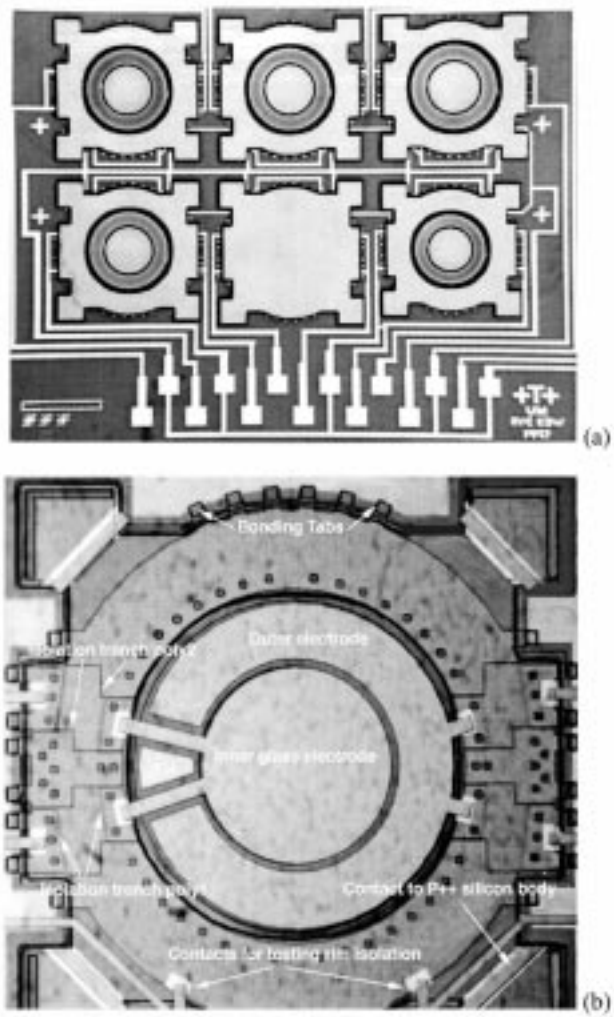


Fig. 6. Top views of the fabricated multilead devices. (a) Five transducers are formed per die having staggered diameters and pressure ranges. A reference capacitor can be seen in the center of the lower row. (b) The view is through the glass side of a completed transducer.

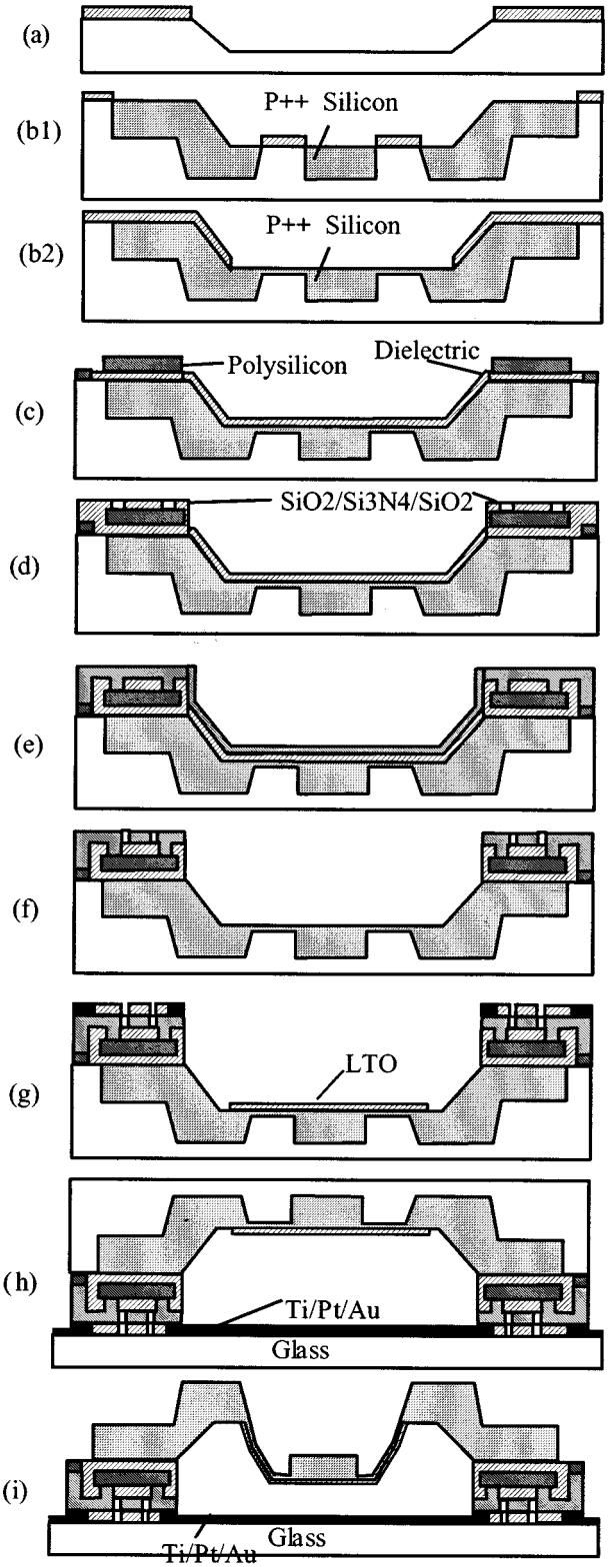


Fig. 7. Process flow for the multilead vacuum-sealed capacitive pressure sensor.

in this etch depth. A patterned masking oxide [see Fig. 7(b1)] is used to define the anchor area using a solid-source deep boron diffusion at 1175 °C. A nominal etch-stop depth of 15 $\mu$m is obtained. This is followed by a masked [see Fig. 7(b2)] shallow boron diffusion step to define the diaphragm, which is approximately 3 $\mu$m thick. After growing a 500-Å thermal oxide, a composite LPCVD $SiO_2/Si_3N_4/SiO_2$ layer having a total thickness of $\sim$0.6 $\mu$m is deposited. 0.8 $\mu$m of polysilicon is deposited followed by a short boron diffusion at 1000 °C to reduce the resistance of the polysilicon. In addition, p+ doping reduces the rate of attack from EDP if the protective dielectric coating on the polysilicon is broken. It is adequate to dope the polysilicon at low temperatures due to the ease of boron diffusion through the grain boundaries. The polysilicon is patterned using $SF_6$ plasma etching. This etch step is done using a two-step lithography. In the first step, the individual leads are patterned. This is done on the polysilicon that is on top of the anchor area. The isolation formed must have straight sidewalls because of the subsequent isolation refill using $SiO_2/Si_3N_4/SiO_2$. In the second etch step, the polysilicon from the recesses is etched. The need for two steps is due to the substantial difference in height for patterns on the anchor and patterns in the recess. After etching, the polysilicon and the dielectric layer on the diaphragm area are removed using wet etching. This is followed by a

second LPCVD $SiO_2/Si_3N_4/SiO_2$ layer with a total thickness of 0.6 $\mu$m. Contact openings are made for the subsequent polysilicon-1 layer to make contact to the: a) silicon bulk along the periphery to form the tabs useful in bonding, and b) along the leads to form the electrical bridges for lead transfer. This is followed by the deposition of a 1.5-$\mu$m-thick layer of polysilicon-1, which is p++ doped at 1000 °C. A CMP (chemical mechanical polishing) step is used to achieve a surface roughness of <500 Å-rms and overcome any nonplanarities due to wafer bowing [15]. For polishing polysilicon, it has been observed that colloidal silica-based slurries give a good surface finish devoid of any scratches and other CMP related defects [13]. A 2800 -Å-LTO layer is now deposited to provide isolation for the two electrodes of the capacitor and provide stress compensation. The LTO layer on the anchor areas is patterned so as to cover only the anchor area and permit contact openings. Ti–Pt is evaporated and lift-off performed with the LTO contact resist mask still in place so as to contact the polysilicon and produce a total height of about 500 Å. At this point, the polysilicon is completely covered by a dielectric layer and has two metal contact areas. Due to the loss of some polysilicon during boron diffusion and CMP, the total height of the dielectric layer and polysilicon stack is about 3 $\mu$m. Thus, we have a total recess depth of 10 $\mu$m. This forms the working gap distance for the capacitor.

The glass processing consists of depositing approximately 250/350/1000 Å of a composite Ti–Pt–Au layer. The Au is then etched back in the contact areas. The glass is partially diced at this point so that the devices can be easily separated after the wafer dissolution step. After this step, we perform wafer-level anodic bonding to 7740 glass in vacuum ($1 \times 10^{-6}$ torr); the structure is as shown in Fig. 7(g). Due to poor heat transfer in vacuum, it is important to first heat the wafers to 400 °C in rough vacuum and then pump down the bonding chamber to higher vacuum levels. While trying to bond wafers which have disjointed bond surfaces, a continuous bond front which can pull in the nonuniform parts of a wafer cannot be formed, and it is imperative that the surface flatness of the silicon wafer be uniform to obtain a high yield. Use of a graphite disk which covers the entire glass surface and an electrode pressure of at least 2500 mbar also contribute significantly to a better bond yield. The next step is to dissolve the wafer in EDP to obtain the final structure as shown in Fig. 7(h). As can be seen, the diaphragm is heavily deflected under normal atmospheric conditions.

## VI. Test Results

### A. Single-Lead Transfer Sensor

The device was tested after interfacing it to a switched-capacitor readout circuit [19] and microcontroller as shown in Fig. 8. Each device has three parallel lead-transfer contacts using the polysilicon sealing rim to transfer the electrode on glass out of the cavity. The lead nominal resistance was about 100 ohms with a TCO of 1200 ppm/ °C. The other electrode is the p++ silicon body, which also uses a poly contact. Its nominal resistance is 46 Ω with a TCO of 1600 ppm/°C.

As mentioned earlier, the single-lead structure was developed as a precursor to a multilead structure. Since the lead transfer

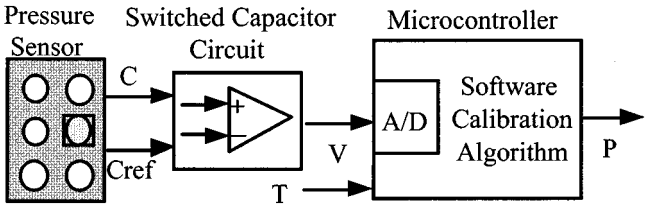


Fig. 8. System configuration for pressure readout.

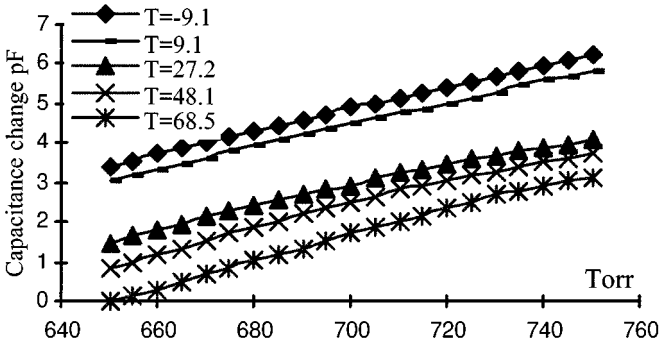


Fig. 9. Typical pressure response for a single-lead-transfer transducer.

and the sealing polysilicon are collapsed into a single layer, a parasitic capacitance is formed in parallel with the sensor. This capacitance is primarily dependent on the width of the rim and the thickness of the dielectric layer between the p++ silicon and the polysilicon. Rim widths from 80 $\mu$m to 200 $\mu$m have been studied. For wafers that were anodically bonded without using CMP, the vacuum bonding yield was larger for devices with narrower rims. This is attributed to the fact that during polysilicon deposition some nucleation sites can occur having heights greater than 50 nm, inhibiting the vacuum seal [10]. The larger the width of the rim, the higher the probability of these sites occurring in the bond area. For devices with anchor widths of 80 $\mu$m, the parasitic capacitance was about 25% of the total capacitance. For devices with anchor widths of 200 $\mu$m, the parasitic capacitance was about 50% of the total capacitance. In both cases, the effects of the parasitic capacitance were effectively canceled using the on-chip reference capacitor.

Fig. 9 shows the behavior of a typical single-lead-transfer device. The nominal sensitivity for the segment devices is 27 fF/torr (3000 ppm/torr). The TCO at 750 torr is 3969 ppm/°C, primarily due to the mismatch between the expansion coefficients of the anchor materials and the glass. The TCS is about 1000 ppm/°C. A resolution of 25 mtorr is achieved after readout and digital compensation. Fig. 10 shows the behavior of the device after interfacing to a programmable gain switched-capacitor readout circuit [19]. The parasitic fixed capacitance between the polysilicon lead transfer and the underlying silicon is overcome using a matched on-chip reference capacitance (see Fig. 2) that tracks process/alignment variations. This is differenced with the transducer capacitance during readout using a switched-capacitor integrator. Taking into consideration process variations and temperature effects, the operating range for a 5-V system is about 3.5 V. Each transducer has a range of about 50 torr. The maximum sensitivity which can be obtained while still covering the entire 50 torr range is thus about 0.07 mV/mtorr. To resolve 25 mtorr

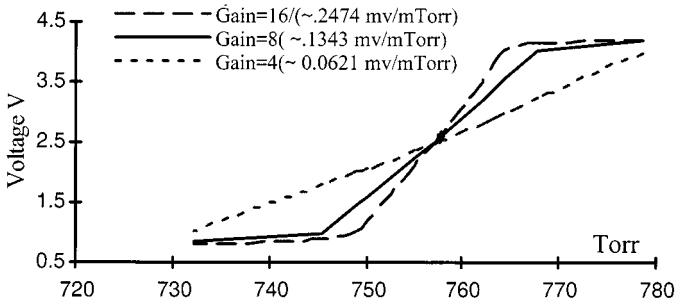


Fig. 10. Output voltage characteristics with programmable gain switched capacitor circuit.

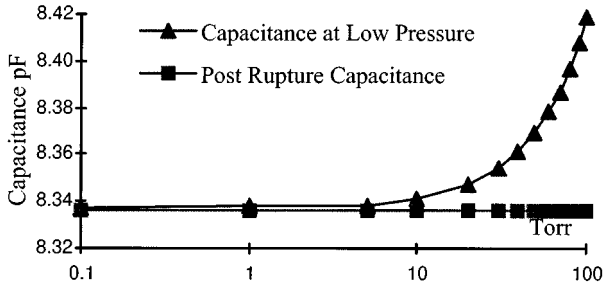


Fig. 11. Capacitance measurements for trapped gas.

after accounting for noise, the LSB on the analog-to-digital converter (ADC) must be 1.75 mV. Thus, at least a 12-bit A/D is required to resolve 25 mtorr with high accuracy. Since we have software-programmable gain, we can use different transducers with higher gain to achieve a resolution of 25 mtorr.

It has been reported [11], [12] that there is some $O_2$ out-diffusion during and after the anodic bonding process. Ti/Pt metal is used in this device for forming the electrode on the glass and covers ~80% of the glass surface inside the sealed cavity. The Ti layer is covered with Pt on one side and is in direct contact with the glass on the other side. At the elevated bonding temperature, Ti effectively getters any $O_2$ out-diffusing from the metal covered portion of the glass in the cavity. To quantify the effects of trapped $O_2$, devices were fabricated which responded in the range below 100 torr. The devices were measured at pressures down to 100 mtorr using an HP4284A LCR meter. A typical response is plotted in Fig. 11. The device diaphragms were then perforated using a low-power (1 $\mu$m sq.) laser beam. The capacitances were measured again for the case of no differential pressure. The results indicate that any residual gas pressure in the sealed cavity is less than 200 mtorr. Dummy Ti/Pt islands could also be used to getter oxygen still further. There is considerable additional area around the cavities that could allow for efficient removal of any out-diffusing gas.

### *B. Multilead Transfer Sensor*

The device was characterized for both dynamic behavior and dc parameters such as lead resistance and parasitic capacitance. The device was also tested after interfacing it to a switched-capacitor readout circuit. Calibration/compensation is done in software to achieve the resolution of 25 mtorr. Each transducer has two redundant parallel lead transfers for each electrode with a nominal resistance of about 50 $\Omega$and a TCO of 1000 ppm/°C. As mentioned earlier, the high parasitic capacitance observed

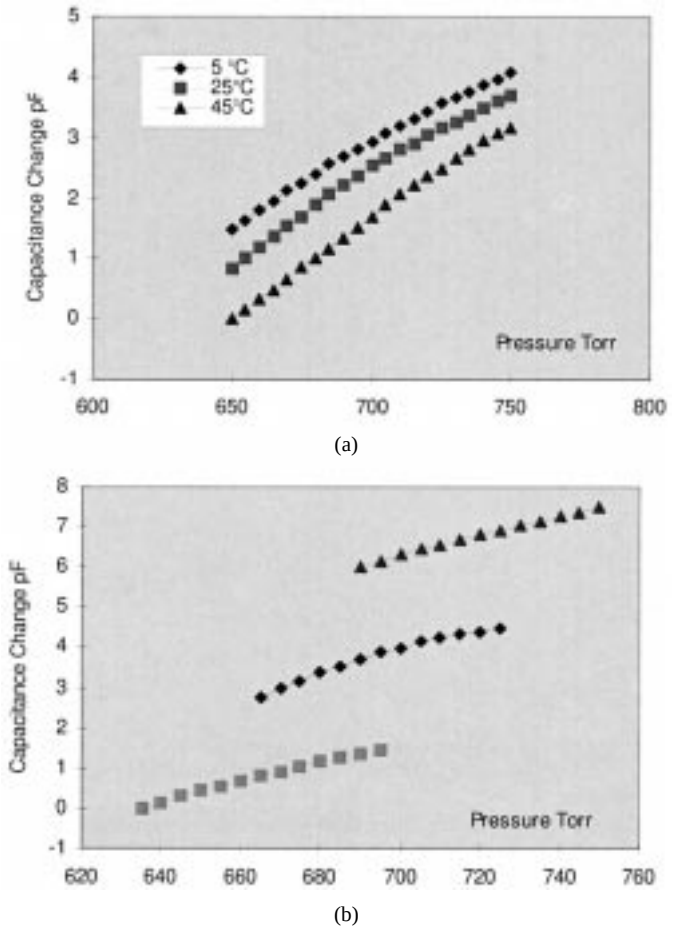


Fig. 12. (a) Typical pressure response for a single transducer over temperature. (b) Response of three different segment transducers.

with the first-generation device has been reduced to 500 fF, which is about 5% of the nominal sensor capacitance. The parasitic capacitance is primarily dependent on the width of the rim, the thickness of the dielectric layer between the p++ silicon and the polysilicon, and the width of the polysilicon bridge formed in the poly-2 layer. An additional ring of Ti/Pt metal is used on the glass to reduce the open glass surface exposed to the cavity and act as a getter. The additional Ti/Pt ring as seen in Fig. 2(b) along with the main metal electrode on glass effectively blocks the high electric field during bonding from the entire cavity. This is a necessary feature if circuitry is to be placed inside the cavity [16]. In devices where a small ($<3$ $\mu$m) working gap is required, this feature prevents bonding of the diaphragm area itself. The multilead structure also makes it feasible to have an independent metal electrode on the silicon isolated from the silicon body, thereby eliminating the need to protect the etched back silicon bulk during operation in humid environments. Fig. 12 shows the behavior of a typical device.

The nominal sensitivity for the segment devices is 39 fF/torr (3800 ppm/torr). The TCO at 750 torr is 1350 ppm/°C and is primarily due to the mismatch of expansion coefficients of the anchor materials and the glass. The TCS is about 1000 ppm/°C. In the case of this sensor, each transducer in the device has a range of about 50 torr. The maximum pressure sensitivity after interfacing to a switched-capacitor circuit, while still covering the entire 50 torr range, is 0.06 mV/mtorr. In a 5-V system, 25 mtorr

resolution is obtained using a 12-b A/D after allowing some margin for noise. As in the case of the single-lead device, software-programmable gain [19], [21] and transducers with higher gain enable a resolution of 25 mtorr.

In order to evaluate the long-term stability of the highly deflected boron-diffused membranes and the integrity of the polysilicon vacuum seals, we have monitored a number of devices for over two years. The total observed variation in sensitivity of the global transducer was less than $\pm 30$ ppm/mmHg for a baseline sensitivity of 1050 ppm/mmHg. At room temperature, the variations in $C_0$ (the 760 torr, 25 °C baseline capacitance) for the global transducer were less than $\pm 12$ fF for a baseline $C_0$ of 12.050 pF, measured using a HP4284A LCR meter. In case of a segment transducer with a $C_0$ of 14.020 pf the variation in sensitivity was less than $\pm 50$ ppm/mmHg for a baseline sensitivity of 3000 ppm/mmHg. At room temperature the average change in $C_0$ over two years was $-22$ fF. The shift is conjectured to be due to outgassing from the sealed cavity because there was no unidirectional shift in sensitivity. This shift is equivalent to an offset of $-800$ ppm/year. Some of these changes are likely due to present measurement accuracy. Long-term detailed testing of the devices is continuing using DH Instruments PPC2 calibrator.

## VII. Conclusion

Vacuum-sealed capacitive barometric pressure sensors employing a batch lead-transfer process have been fabricated. By operating at a gap spacing between 0.3 $\mu$m and 0.8 $\mu$m, the sensor achieves a resolution of 25 mtorr under atmospheric offset pressures. Polysilicon is used to achieve sealing as well as a lead transfer from the inside of the cavity. The advantages include the elimination of stiction problems, high bandwidth, and adaptability to other glass–Si sensors. In addition, the multilead extension of this technique could also be used for active circuit packaging. CMP is used to improve the bonding yield. The sensors show no significant sensitivity change after two years of shelf storage under atmospheric conditions.

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