Designing a ZigBee-ready IEEE 802.15.4-compliant radio transceiver

Besides highlighting the overall characteristics of the physical (PHY) and MAC layers of the IEEE 802.15.4 standard, and the network, security and application layers of the ZigBee wireless technology, this article focuses on efficient implementation of IEEE 802.15.4-compliant radio-on-a-chip by identifying potential low-power features in the standard, suitable transceiver architectures and considering standard CMOS design issues. In addition, it also presents system-level considerations and implementation choices for a commercially available low-cost, low-power Zigbee-ready CMOS RF transceiver compliant to the IEEE 802.15.4 standard.

By Khanh Tuan Le

Wireless connectivity of a vast number of industrial and home applications has modest transmission data requirements, but demands reliable and secure communication using simple low-cost and low-power radio systems. In the quest for high-bandwidth, multimedia-capable wireless networks, the need for cost and power-effective radio solutions for this vast number of fairly simple applications was only recently addressed by a standardized technology. The IEEE 802.15.4 standard and Zigbee wireless technology are designed to satisfy the market's need for a low-cost, standard-based and flexible wireless network technology, which offers low power consumption, reliability, interoperability and security for control and monitoring applications with low to moderate data rates. The complexity and cost of the IEEE802.15.4/Zigbee-compliant devices are intended to be low and scalable (application dependent) in order to enable broad commercial adaptation in cost-sensitive applications. In addition, the compliant system implementations will enable long battery life by using the power-saving features at the physical, MAC and network layers specified by this standard.

In this respect, the implementation of the physical layer of the IEEE 802.15.4 standard, including the RF, IF and de-/modulation must be optimized to meet the challenging low-cost and low-power targets.

IEEE 802.15.4 and ZigBee overview

The IEEE 802.15.4 standard and the ZigBee technology address easy, low-cost deployment of power-friendly and flexible implementations of a virtually unlimited number of wireless low data rate monitoring and control applications. The application sphere of this wireless personal area network (WPAN) technology ranges from industrial monitoring and control, home automation, sensor networks to gaming, medical and automotive solutions. The various layers of the IEEE 802.15.4/Zigbee technology together with the interaction between the IEEE standard, the Zigbee Alliance and end-user providers are shown in Figure 1.

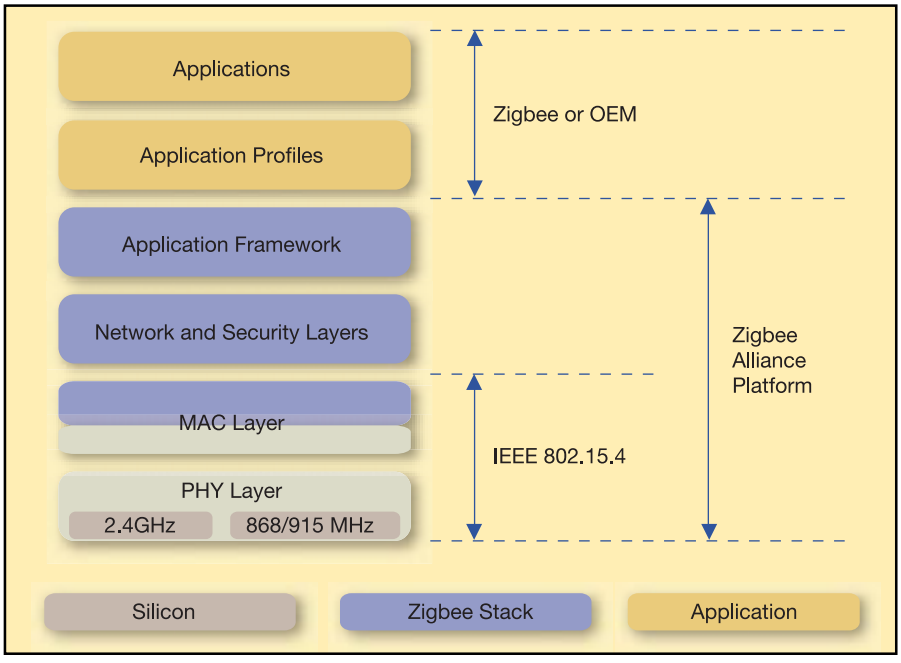

Figure 1. IEEE 802.15.4 and ZigBee working model.

The IEEE 802.15.4 standard[1] specifies the PHYsical (PHY) and Media Access Control (MAC) layers at the 868 MHz, 915 MHz and 2.4 GHz ISM bands, enabling global or regional deployment. The air interface is direct sequence spread spectrum (DSSS) using BPSK for 868 MHz and 915 MHz and O-QPSK for 2.4 GHz. The access method in IEEE 802.15.4-enabled networks is carrier sense multiple access with collision avoidance (CSMA-CA). The IEEE 802.15.4 PHY includes receiver energy detection (ED), link quality indication (LQI) and clear channel assessment (CCA). Both contention-based and contention-free channel access methods are supported. The IEEE 802.15.4 standard employs 64-bit IEEE and 16-bit short addresses to support theoretically more

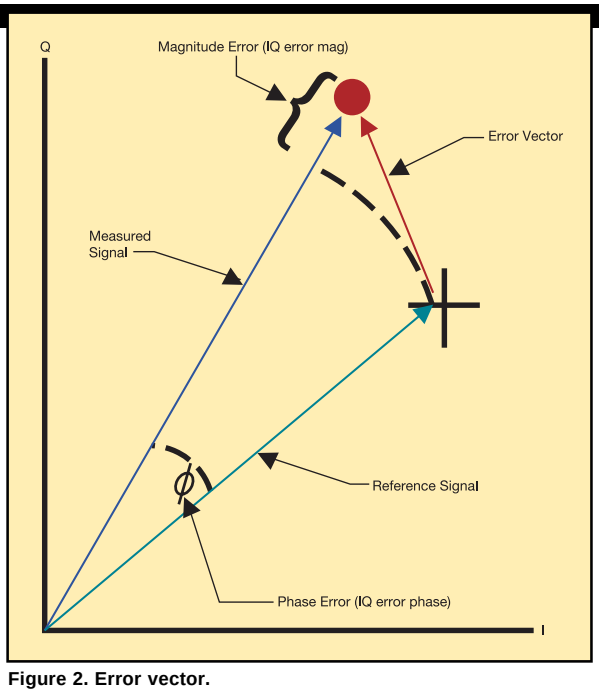

Figure 2. Error vector.

than 65,000 nodes per network. The IEEE 802.15.4 MAC handles network association and disassociation, has an optional superframe structure with beacons for time synchronization, and a guaranteed time slot (GTS) mechanism for high- priority communications.

The Zigbee alliance is responsible for the Zigbee wireless technology[2], which defines the network, security, and application layers upon the IEEE 802.15.4 PHY and MAC layers, and also provides interoperability and conformance testing specifications.

The Zigbee network layer handles device discovery and network configuration and supports three networking topologies: Star, mesh (peer-to-peer) and cluster-tree (hybrid star/mesh). Zigbee-enabled products will be based on physical (full function device and reduced function device), logical (coordinator, router and end device) and application (application profile) device types. To ensure reliable and secure wireless networks, Zigbee offers a security toolbox including access control lists, data freshness timer and 128-bit encryption.

Parameter	2.4 GHz PHY	868/915 MHz PHY
Sensitivity @ 1% PER	-85 dBm	-92 dBm
Receiver Maximum Input Level	-20 dBm	
Adjacent Channel Rejection	0 dB	
Alternate Channel Rejection	30 dB	
Output Power (Lowest Maximum)	-3 dBm	
Transmit Modulation Accuracy	EVM<35% for 1000 chips	
Number of Channels	16	1/10
Channel Spacing	5 MHz	single-channel/2 MHz
Transmission Rates Data Rate Symbol Rate Chip Rate	 250 kb/s 62.5 ksymbol/s 2 Mchip/s	 20/40 kb/s 20/40 ksymbol/s 300/600 kchip/s
Chip Modulation	O-QPSK with half-sine pulse shaping (MSK)	BPSK with raised cosine pulse shaping
RX-TX and TX-RX turnaround time	12 Symbols	

Table 1. IEEE 802.15.4 PHY parameters.

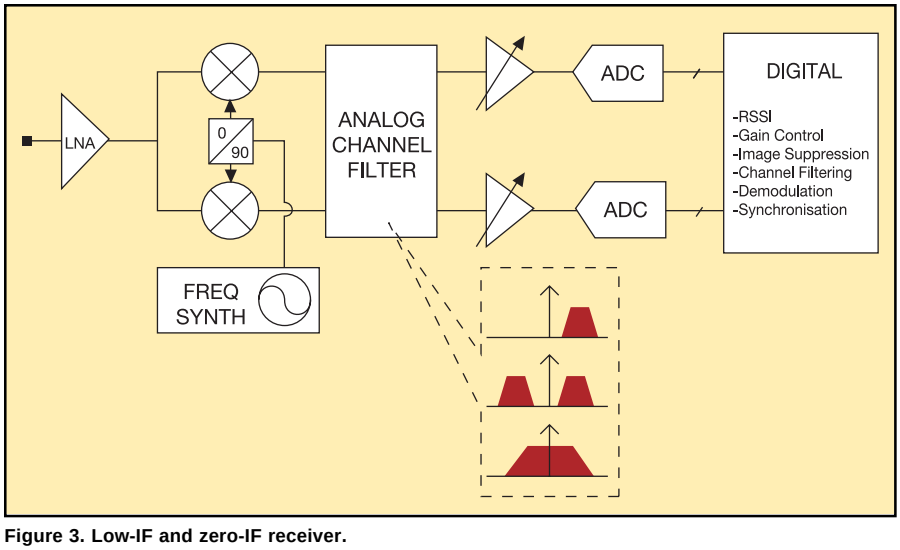

Figure 3. Low-IF and zero-IF receiver.

Physical layer

The IEEE 802.15.4/Zigbee technology is specified with a wide range of low-power features at physical (implementation-wise) and higher (operational) levels. The operational power-saving features include low duty cycle operation together with strict power management and low transmission overhead.

The implementation of standard-compliant radio-on-a-chip is mainly governed by the PHY specification. At the PHY level, which is the main topic of this discussion, low-power silicon devices can be implemented by exploiting relatively low and controllable output power, constant-envelope modulation, and relatively relaxed channel spacing and blocking requirements. The main parameters of the IEEE 802.15.4 PHY are summarized in Table 1.

The 2.4 GHz PHY of the IEEE 802.15.4 standard attracts a lot of focus from the wireless industry because the globally available 2.4 GHz ISM band with the largest bandwidth promotes world-wide market and flexibility of application designs. The technical considerations in the following are specifically related to the 2.4 GHz PHY implementation, but most of them are also valid for the 868/915 MHz PHY devices.

Two parameters in Table 1 deserve some comments. The modulation accuracy of an IEEE 802.15.4 transmitter is determined with an error vector magnitude (EVM) measurement, which is graphically detailed in Figure 2. EVM is the scalar distance between the two phasor end points representing the ideal and the actual measured chip positions. Expressed another way, it is the residual noise and distortion remaining after an ideal version of the signal has been stripped away.

The offset-QPSK with half-sine pulse shaping modulation selected for the 2.4 GHz PHY is equivalent to minimum shift keying (MSK), which is a constant envelope modulation scheme. This allows the use of simple, low-cost and relatively non-linear power amplifier designs.

CMOS approach

The foremost benefits of CMOS are low cost and single-chip integration capability. CMOS enables the integration of digital baseband processing, RF/analog circuits and

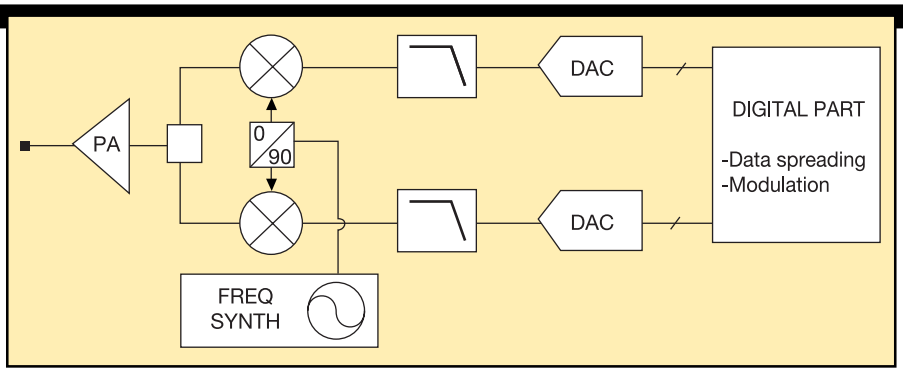

Figure 4. I/Q-modulation transmitter topology.

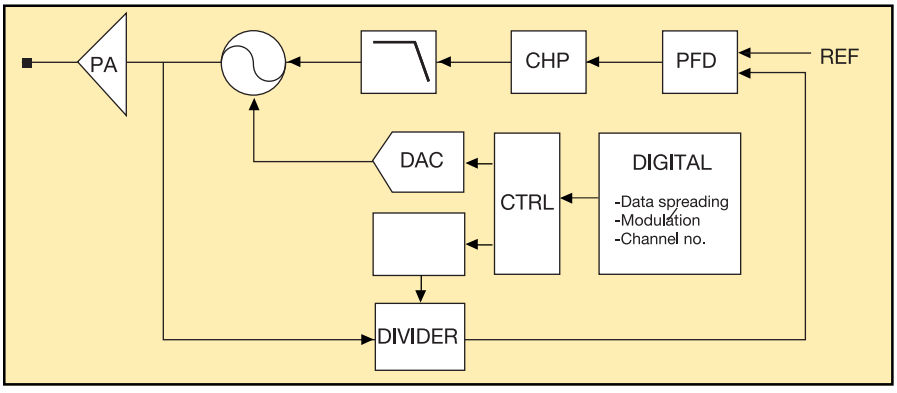

Figure 5. Two-point modulation transmitter topology.

system memory in the same physical silicon.

The refinement and scaling of CMOS processes result in strong improvement in RF performance of MOSFET devices (active devices are no longer the bottleneck, the challenge is to move the signal between them without too much signal degradation or burning a lot of power) and high quality of on-chip passives. For CMOS RF and analog design, the inherent trade-offs between speed, noise and power can be remedied by concurrent system and circuit design, optimum choice of transceiver and frequency synthesiser architectures, calibration techniques in the analog and/or digital domains, and careful floor-planning and layout. These features together with CMOS's unparalleled digital processing capability make CMOS the most viable technology for low cost, highly integrated wireless silicon devices, and the technology of choice for the implementation of system-on-a-chip solutions.

The IEEE 802.15.4 PHY specification has been developed focusing on highly integrated and low-cost, low-power silicon solutions. The specified transmit output power and receiver sensitivity can be conveniently achieved using CMOS technology. ZigBee products built upon the IEEE 802.15.4 specification will for sure rely on CMOS radio-on-chip and system-on-chip solutions.

Transceiver architecture considerations

The selection of a specific receiver-transmitter architecture combination requires careful examination of issues such as functional performance, power consumption, ease-of-integration, silicon area, and requirement of external components.

Receiver architecture

Traditional heterodyne receivers with one or more intermediate frequency (IF) stages offer good channel selectivity and robustness, but they require expensive and bulky off-chip filters resulting in low degree of integration, high bill-of-material and increased power consumption of on-chip drivers. The heterodyne receiver architectures are not optimal solutions for achieving the low-cost, low-power targets of the IEEE 802.15.4 PHY specification.

Driving IEEE 802.15.4/Zigbee silicon to the cost level and power performance necessary for mass market of low data rate applications requires pushing the channel filtering function on-chip to lower frequencies through the selective use of single-conversion architectures, i.e. the zero-IF and low-IF receiver architectures. The zero-IF (also often referred to as direct-conversion) and low-IF receiver architectures are excellent candidates for completely integrated receivers with good performance at low power and small silicon area.

In a zero-IF receiver, the RF signal is downconverted directly to baseband, minimizing the number of signal processing stages, and subsequent signal processing can be performed with high accuracy and flexibility at low power consumption. The troublesome image in this case is a replica of the signal itself that can be adequately removed by the quadrature-mixing scheme. Obviously, direct-conversion receivers require no expensive and bulky external filter for analog channel selectivity. Among the weaknesses of this topology, the most prominent are static and dynamic DC offsets and 1/f-noise (especially in deep submicron CMOS technologies). However, the challenges related to zero-IF receivers can be overcome by careful design and layout combined with recent advances in digital signal processing.

In a low-IF receiver, the RF signal is mixed down to a non-zero low or moderate frequency, typically a few megahertz for IEEE 802.15.4 2.4 GHz PHY signals. Low-IF receiver topologies have many of the desirable properties of zero-IF architectures, but avoid the dc offset and 1/f-noise problems. However, the use of a non-zero IF re-introduces the image issue. Fortunately, the relatively relaxed image and neighbouring channel rejection requirements of the IEEE 802.15.4 PHY can be satisfied by carefully designed low-IF receivers. Image signal and unwanted blockers are rejected by the quadrature downconversion (complex mixing) and subsequent filters in both analog and digital domains.

After the I/Q-downconversion, which enables complex signal processing in all zero-IF and low-IF receiver architectures, a wide range of solutions exist for the tasks of image rejection, analog channel filtering (low-pass, bandpass, complex) and analog-to-digital

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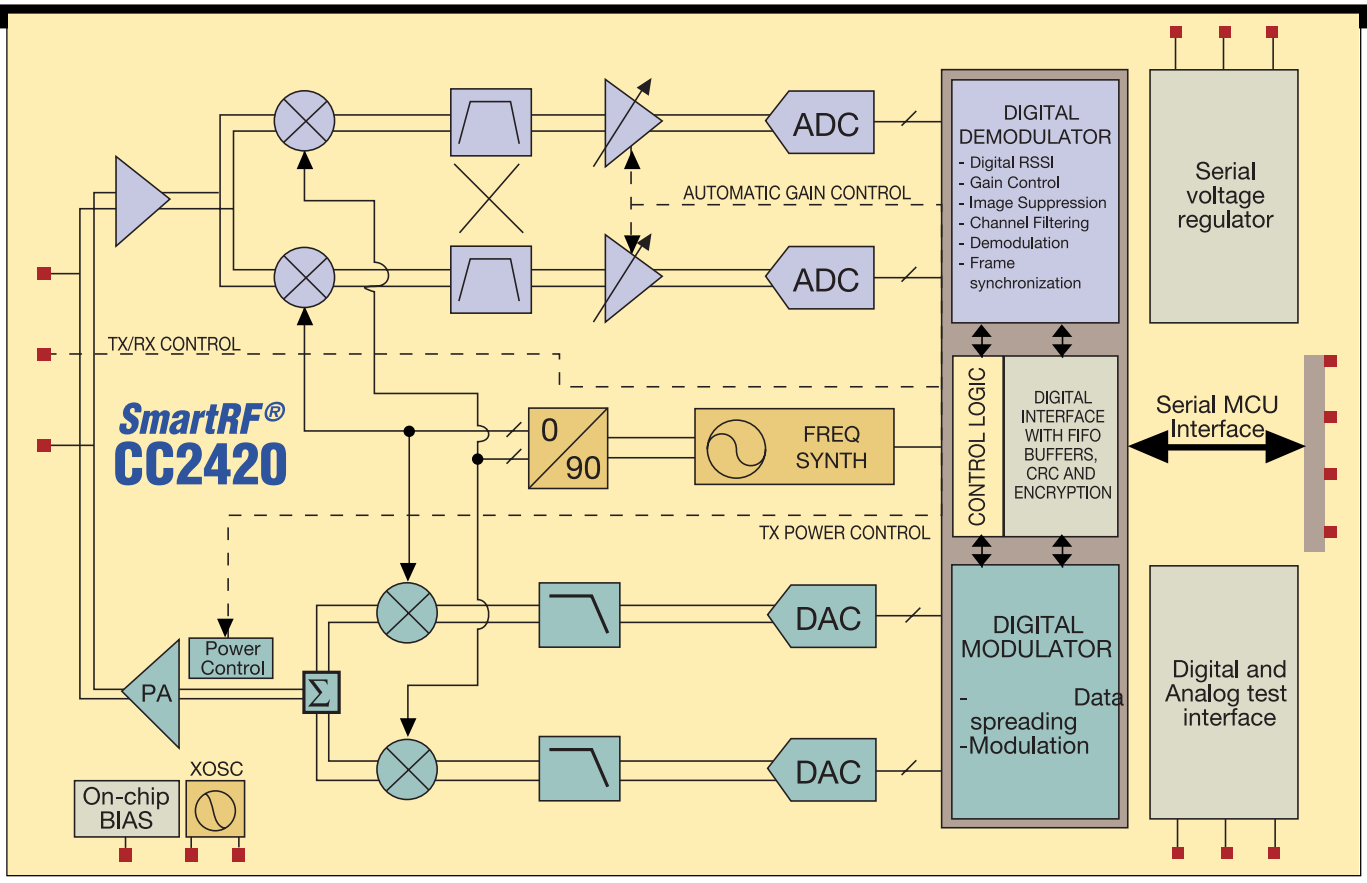

Figure 6. IEEE 802.15.4-compliant and ZigBee-ready CC2420 radio transceiver.

conversion (ADC)-Nyquist, sigma-delta etc.

Figure 3 illustrates an example of a typical receiver chain with quadrature path ADCs employing either the zero-IF or the low-IF architecture. In this receiver, the type and rejection requirements of the analog filtering stage usually differ for the two topologies affecting the dynamic range and hence the performance of the succeeding stages. Possible filtering techniques are also indicated in the same figure.

Efficient generation of the transmit signal according to the IEEE 802.15.4 PHY can be achieved by using single-step I/Q upconversion or VCO modulation transmitter technologies.

Transmitter architecture

Similar to their heterodyne receiver counterparts, transmitters based on multiple upconversion and filtering stages do not comply with the low-cost and low-power philosophy of the IEEE 802.15.4 standard. Efficient generation of the transmit signal according to the IEEE 802.15.4 PHY can be achieved by using single-step I/Q-upconversion or VCO modulation transmitter topologies.

In an I/Q-modulator, the signal is upconverted using quadrature mixers resulting in a single-sideband RF output. This transmitter architecture is universal, provides excellent performance and is extremely flexible with respect to supporting high data rates and different modulation formats of constant and non-constant envelope nature. The performance and flexibility of I/Q-modulators are achieved by a slightly higher number of on-chip modules due to the quadrature signal paths.

Figure 4 shows the block diagram of a typical transmitter employing the single-step I/Q-modulation technique: The in-phase and quadrature baseband signals carrying transmit data are precisely processed and modulated in the digital domain before they progress through two digital-to-analog converters (DACs) followed by simple smoothing filters to drive the I/Q-modulator.

Alternatively, a low-power transmitter architecture for constant-envelope modulation schemes, such as the MSK modulation of the 2.4 GHz PHY, can be achieved by modulating the VCO in closed-loop or open-loop operation.

The underlying principle of the open-loop technique is to open the loop after the PLL settles to the desired channel frequency and directly modulate the VCO. In the closed-loop approach, the modulation is done by varying the division ratio in the PLL or a combination of varying the division ratio and modulation of the VCO directly (two-point modulation). A block diagram of a commonly used two-point modulation transmitter is shown in Figure 5.

Both open-loop and closed-loop transmitter architectures are hardware and power efficient for constant envelope modulation schemes as the modulated VCO can drive the power amplifier directly, and several analog circuit blocks are eliminated. However, the open-loop approach has a severe drawback in terms of frequency drift or instability, which is caused by one or combination of several effects such as charge leakage, change in operating conditions and mechanical disturbances. The closed-loop VCO modulation does not suffer from the frequency instability, but usually requires calibration and pre-compensation of the loop bandwidth response or signal transfer characteristic. Fortunately, the required calibration and compensation can be solved efficiently using digital signal processing techniques.

The I/Q-modulation and closed-loop VCO modulation topologies are the most promising candidates to provide an efficient and robust IEEE 802.15.4-compliant transmitter.

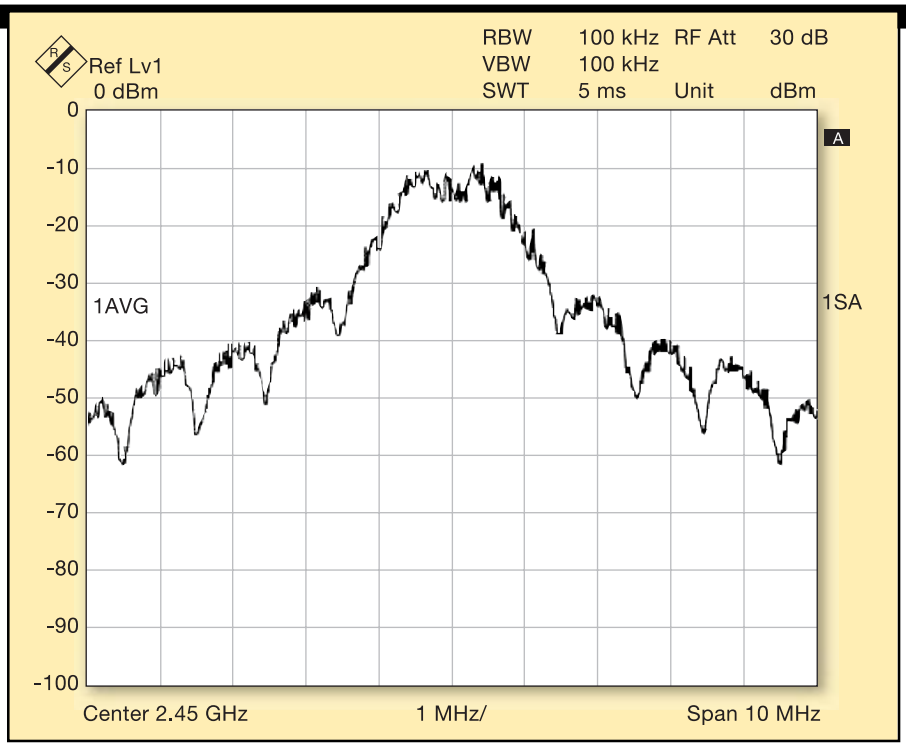

Figure 7. Output spectrum of the CC2420 transmitter.

Ultra-low power RF transceiver

System-level considerations and implementation choices of a representative device, the CC2420, is described in the following to demonstrate the preceding discussion. This device integrates all PHY-related digital functionalities with the RF and analog circuitries using a mainstream 0.18 µm CMOS technology for cost and integration benefits. The principle block diagram of the CC2420 is shown in Figure 6. Communication with an external microcontroller is through a standard four-wire serial peripheral interface (SPI).

In transmit mode, the device buffers the supplied data in a 128 byte TX FIFO and generates automatically preamble, start of frame delimiter (SFD) and frame check sequence (FCS). The bit mapping and modulation are performed according to the IEEE 802.15.4 specification. The data bitstream is coded into predefined 4-bit symbols where each of the 16 symbols consists of a nearly orthogonal 32-chip pseudo-random sequence. The overall data bit to symbol mapping effectively implements a direct sequence spread spectrum (DSSS) scheme with a chip rate of 2 Mchips/s from a data rate of 250 kbps. The signal spreading and O-QPSK modulation with half-sine pulse shaping are performed digitally. The modulated and spread I/Q baseband signals are applied to the DACs, whose outputs are low-pass-filtered and upconverted to RF by a single-sideband modulator. Finally, the RF signal is amplified to a programmable level by the on-chip power amplifier before entering the external antenna. A plot of the modulated spectrum from CC2420 is shown in Figure 7. The main lobe occupies a bandwidth of approximately 3 MHz. The transmitted signal has an EVM of 20% (at worst case), well within the specified requirement of 35%.

The receiver is based on the low-IF architecture, wherein the received RF signal is amplified by the low-noise amplifier and downconverted in quadrature to a 2 MHz IF. The IF signal is filtered and amplified and then digitized by two ADCs. Automatic gain control, fine channel filtering, and symbol correlation (including despreading and byte synchronization) are performed in the digital domain for high accuracy and area efficiency. The cyclic redundancy check (CRC) of the received data is carried out automatically on-chip, and up to 128 bytes of data can be buffered in the RX FIFO, which is accessible through the SPI. The CC2420 receiver achieves a sensitivity of -94 dBm (IEEE 802.15.4 spec. -85 dBm) and better than 35 dB (spec. 0 dB) and 55 dB (spec. 30 dB) adjacent and alternate channel rejection, respectively. Good sensitivity increases the communication range and reliability, while high rejection of unwanted interferers enhances co-existence robustness in the 2.4 GHz ISM band.

The frequency synthesizer is fully integrated, eliminating any need for loop filter or VCO external passives. The on-chip LC VCO operating at twice the LO frequency range together with a divide-by-2 circuit provide the quadrature LO signals, which are shared by the transmit and receive complex (quadrature) mixers.

An external TX/RX switch is not required because the CC2420 handles this switching internally. The chip-to-antenna RF interface consists of a few low-cost capacitors and inductors. This passive network provides impedance matching, some filtering and the conversion between single-ended and differential RF signals that allows the use of fully balanced circuits on-chip for enhanced noise immunity.

The ZigBee-ready CC2420 CMOS device surpasses the IEEE 802.15.4 specification in terms of transmit modulation accuracy and receive sensitivity and selectivity performance enabling effective and reliable communication links. It achieves this performance using the I/Q-modulation transmitter and low-IF receiver architectures with ultralow power consumption.

Conclusion

ZigBee and the underlying IEEE 802.15.4 standard promise a low-cost, low-power and reliable wireless network technology for a wide range of control and monitoring applications within the private sphere and industrial environment.

The IEEE 802.15.4 PHY has been specified with focus on highly integrated and low-power chip solutions, which promote simple and flexible end application designs at low cost.

For IEEE 802.15.4-compliant and Zigbee-ready silicon devices, CMOS is the technology of choice because it can deliver the required performance at the lowest cost and highest integration level. The single-conversion zero-IF and low-IF receiver architectures in combination with the I/Q-modulation and closed-loop VCO modulation transmitter topologies have the fundamental merits to satisfy the low-cost and low-power philosophy of the IEEE 802.15.4 standard. RFD

References

1. IEEE 802.15.4 Standard Specification, downloadable at standards.ieee.org/getieee802/.

2. Zigbee technical documents at www.zigbee.org.

3. CC2420 Datasheet, downloadable at www.chipcon.com.

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