Shruti Padmanabha

Curriculum Vitae

Current Position

2011–Present **Research Assistant**, University of Michigan, Ann Arbor.

Research Interests

My research interests lie in the area of energy-efficient heterogeneous multicore systems. I actively work on both designing such systems as well as optimally scheduling applications on them.

Education

2012–2016 **Ph.D. Computer Science & Engineering**, *The University of Michigan*, Ann Arbor, MI.
Thesis Title: Exploiting fine-grain heterogeneity to build energy-efficient processors

2011–2012 **M.S. Computer Science & Engineering**, *The University of Michigan*, Ann Arbor, MI.
GPA: 4.0

2007–2011 **B.E. Computer Science**, *Birla Institute of Technology and Science Pilani*, Goa, India.
GPA: 9.83/10

Prior Experience

2011–Present **Graduate Student Research Assistant**, University of Michigan, Ann Arbor, MI.
- My project achieves energy-efficient processor design by providing customization of hardware within a core. Intelligent scheduling mechanisms allow applications to switch between the best hardware suited for the current instructions at a granularity of hundreds of instructions, improving efficiency.
- I use the Gem5 architectural simulator to explore and evaluate novel hardware designs and efficient schedulers to achieve optimal efficiency.

2015 **Software Engineer Intern**, *Cross Data-center (XDC) - Facebook*, Menlo Park, CA.
- Worked on optimizing allocation of servers in Facebook's data centers based on their dynamic utilization, while constraining increase of user-observed latencies. We found sources of under-utilization in the front-end servers, and built a reliable algorithm to dynamically reallocate them based on current user traffic patterns.
- We deployed the algorithm deployed on production data-center clusters and showed that servers could be reallocated even during peak usage, while maintaining latency constraints.

2012 **Graduate Technical Intern**, *Microprocessor Research Group, Intel Labs*, Santa Clara, CA.
- Worked with the Platform Architecture Research group to explore energy efficient cache alternatives CPU-GPU heterogeneous cores. I analyzed GPGPU applications characteristics, particularly their memory access behavior, from the Rodinia Benchmark Suite.
- Using their in-house processor simulator and the memory model of graphite, I proposed that smaller caches private to execution slices of the GPU is more energy efficient than the shared configurations prevalent today.

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2011 **Undergraduate Intern**, *ARM Ltd.*, Bangalore, India.
- Worked with the Memory Management Unit development group, as part of the Architecture Verification Suite for ARM's 64-bit v8 architecture. In particular I was involved with the page table generation flow of the processor, and have researched, improved, and completed the verification tasks related to the memory system.

Publications

Conference Proceedings

MICRO'15 1. **"DynaMOS: Dynamic Schedule Migration for Heterogeneous Cores"**, ***Shruti Padmanabha***, *Andrew Lukefahr, Reetuparna Das, and Scott Mahlke*, *The International Symposium on Microarchitecture (MICRO-48), To Appear, Dec. 2015.*

PACT'14 2. **"Heterogeneous Microarchitectures Trump Voltage Scaling for Low-Power Cores"**, *Andrew Lukefahr,* ***Shruti Padmanabha****, Reetuparna Das, Ronald G. Dreslinski, Thomas F. Wenisch, and Scott Mahlke*, *The International Conference on Parallel Architectures and Compilation Techniques (PACT-23), Aug. 2014.*
- *Acceptance Rate 37/144 ≈ 25%*

MICRO'13 3. **"Trace-Based Phase Prediction For Tightly-Coupled Heterogeneous Cores"**, ***Shruti Padmanabha***, *Andrew Lukefahr, Reetuparna Das, and Scott Mahlke*, *The International Symposium on Microarchitecture (MICRO-46), Dec. 2013.*
- *Acceptance Rate 39/239 ≈ 16%*

MICRO'12 4. **"Composite Cores: Pushing Heterogeneity into a Core"**, *Andrew Lukefahr,* ***Shruti Padmanabha****, Reetuparna Das, Faissal M. Sleiman, Ronald G. Dreslinski, Thomas F. Wenisch, and Scott Mahlke*, *The International Symposium on Microarchitecture (MICRO-45), Dec. 2012.*
- *Acceptance Rate 40/228 ≈ 18%*

Journal Articles

IEEE TC 5. **"Exploring Fine-Grained Heterogeneity with Composite Cores"**, *Andrew Lukefahr,* ***Shruti Padmanabha****, Reetuparna Das, Faissal Sleiman, Ronald G. Dreslinski, Thomas F. Wenisch, Scott Mahlke*, IEEE Transactions on Computers, To Appear. 2015.

Workshops

PRISM'15 6. **"Adaptive Cache Partitioning on a Composite Core"** , *Jiecao Yu, Andrew Lukefahr,* ***Shruti Padmanabha****, Reetuparna Das, and Scott Mahlke*, *The PRISM-3 Workshop at The International Symposium on Computer Architecture (ISCA-45), June, 2015.*

GEM5'12 7. **"Performance Prediction Models"** , ***Shruti Padmanabha****, Andrew Lukefahr, Reetuparna Das, and Scott Mahlke*, *Gem5 Users Workshop at The International Symposium on Microarchitecture (MICRO-45), Dec, 2012.*

Patents

WO 2014060393 1. **Control of Switching Between Executed Mechanisms**, ***Shruti Padmanabha****, Andrew Lukefahr, Reetuparna Das, and Scott Mahlke*, World Patent Pending #2014060393, Filed: October 14, 2014.

WO 2014093042 2. **Trace Based Phase Prediction for Tightly-Coupled Heterogeneous Cores**, ***Shruti Padmanabha****, Andrew Lukefahr, Reetuparna Das, and Scott Mahlke*, World Patent Pending #2014093042, Filed: November 29, 2013.

US 2014093090 3. **Heterogeneity Within A Processor Core**, *Andrew Lukefahr,* ***Shruti Padmanabha****, Reetuparna Das, and Scott Mahlke*, US Patent Pending #201409309, Filed: November 29, 2013.

Invited Talks

2016 Energy Efficient Heterogeneous Processor Architectures for General Purpose Applications, *Microarchitecture Research Lab*, Intel Labs, Bangalore, India.

2016 Introduction to Research in Computer Architecture, as part of the 2015 Alumni Research Talks Series, *BITS Pilani*, Pilani, India.

Awards and Honors

Graduate Awards

2015 Finalist in the Richard and Eleanor Towner Prize for Outstanding Ph.D. Research, *College of Engineering*, The University of Michigan.

2015 Grace Hopper Celebration Scholarship, *Houston, TX*.

2014 CSE Nominee for the Rackham Predoctoral Fellowship, *Computer Science and Engineering*, The University of Michigan.

2011–2012 Rackham graduate fellowship, *Computer Science and Engineering*, The University of Michigan.

Undergraduate Awards

2007–2011 Merit scholarship for the top 5 cumulative GPA holders, *BITS Pilani*, Goa, India.

Conference Attendance Grants

2015 MICRO-48, *Portland, OR*.

2015 Career Workshop for Women and Minorities in Computer Architecture, *Waikiki, Hawaii*.

2015 ISCA-43, *Waikiki, Hawaii*.

2015 Rackham Travel Grant (ISCA-43), *Portland, OR*.

2015 CRA-W Early-Career Mentoring Workshop (CMW) at FCRC, *Portland, OR*.

2013 MICRO-46, *Davis, CA*.

2013 Rackham Travel Grant (MICRO-46), *Davis, CA*.

2012 MICRO-45, *Vancouver, Canada*.

2011 Ratan Tata travel grant, *Mumbai, India*.

Technical Skills

Architectural Simulators: M5/GEM5, Graphite (memory subsystem).

Compilers: LLVM.

Programming Lanugages: C, C++, Python, Bash, Verilog VHDL, Perl.

Design Software: MATLAB, Xilnx Software Development Kit.

Relevant Class Projects

2011 **Computer Architecture (EECS470)**, University of Michigan, Ann Arbor, MI.
- Designed and implemented a 64 bit, 2 way superscalar out of order processor in Verilog with features like non- blocking cache, adaptive instruction prefetcher, store-load forwarding, early tag broadcast, RAS, g-share branch predictor
- Achieved highest performance in class for the course

2012 **Parallel Computer Architecture (EECS570)**, University of Michigan, Ann Arbor, MI.
- Explored the viability and implementation issues of introducing non-volatile memories like PCM on 3D stacked architectures

2010-2011 **Undergraduate projects**, BITS Pilani, Goa, India.
- Learnt and researched about load balancing algorithms in parallel computing by completing an independent study under Dr. Bharat M. Deshpande
- Evaluated the performance of embedded multiplier blocks on FPGAs and compared its performance to that of a logic-based multiplying unit
- Built a floating point Scientific Calculator on an 8051 microcontroller for a course on Embedded System and Design

Relevant Graduate Courses

Micro-architecture Parallel Computer Architecture Computer Architecture Advanced Compilers

Teaching Experience

2010 **Professional Assistant**, *Digital Electronics and Computer Organization*.

2010 **Professional Assistant**, *Microprocessor Programming and Interfacing*.

Professional Activities and Service

Conference Reviewer

2015 International Symposium on Computer Architecture (ISCA)

2013, 2015 International Conference on Microarchitecture (MICRO)

2016 International Symposium on High-Performance Computer Architecture (HPCA)

2015, 2016 International Symposium on Code Generation and Optimization (CGO)

2015,2016 International Conference on Parallel Architectures and Compilation Techniques (PACT)

2014 International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES)

Services

2012–Present U-M Ensemble of Computer Science & Engineering Ladies, *Founding member & Officer*.