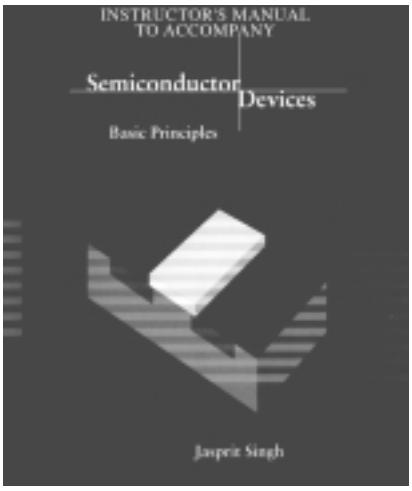
# Chapter

# 10

# FIELD EFFECT TRANSISTORS: MOSFET



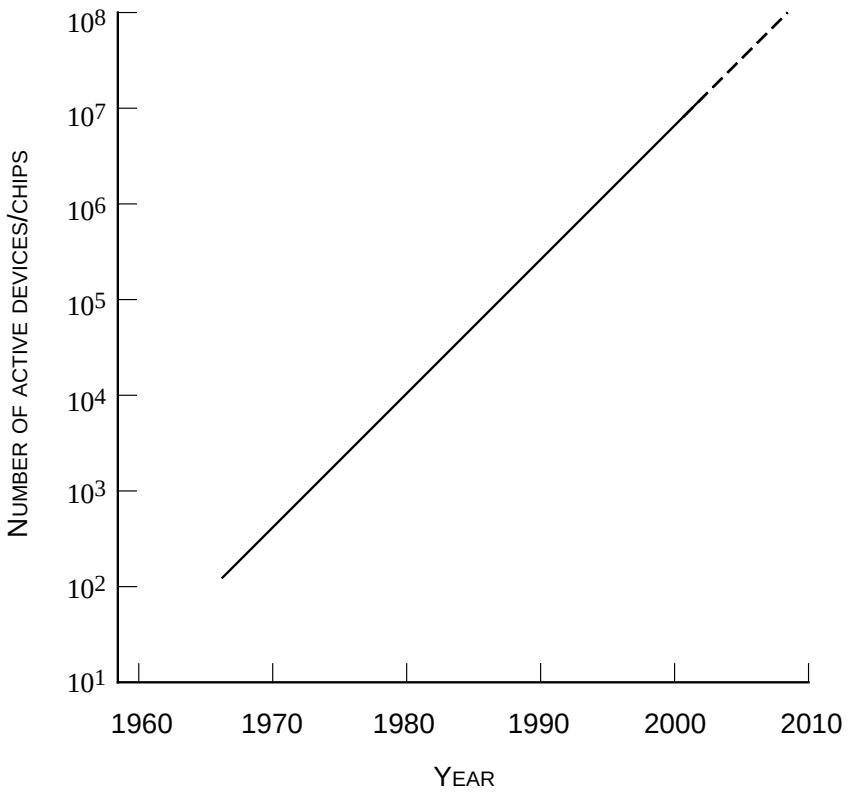

The following overview figures describe important issues related to the most important electronic device.

# MOORE'S LAW

Gordon Moore, co-founder of Intel:

1st law: Complexity (number of active devices) of a chip doubles every 18 months.
2nd law: Cost of a fabrication facility grows on a semi-log scale with time.

- Complexity increases at ~59% per year!
- At current pace, semiconductor fabrication facilities will cost $250 billion by 2010!

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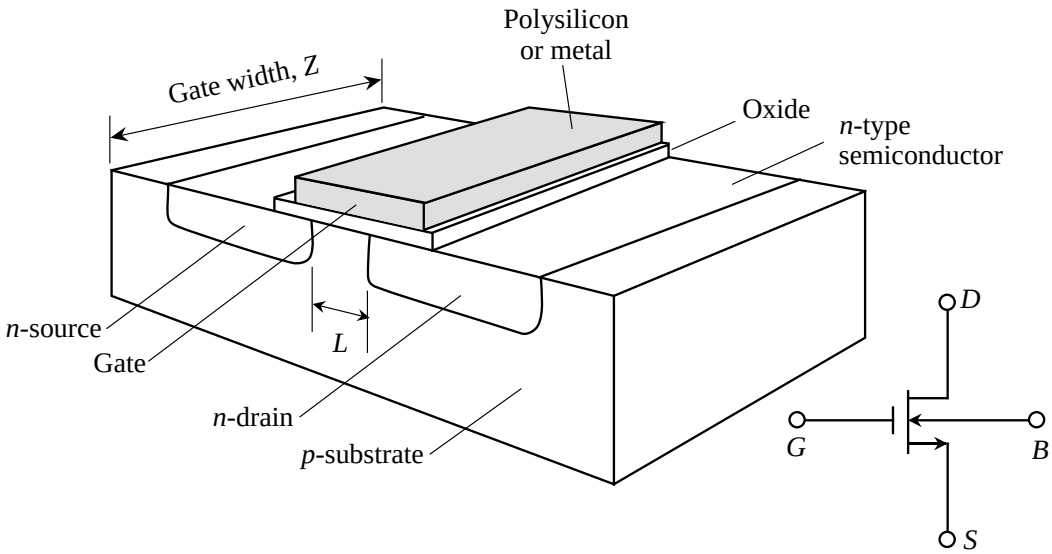
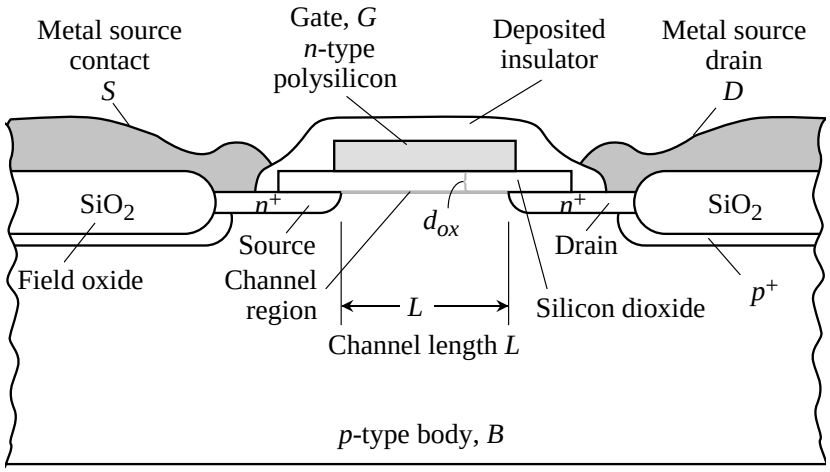
# An overview of the MOSFET sturcture




(a)
Structure Schematic symbol




(b)
Cross-sectional view

Modern MOSFETs are enormously complex devices with great care taken to reduce parasitic elements.

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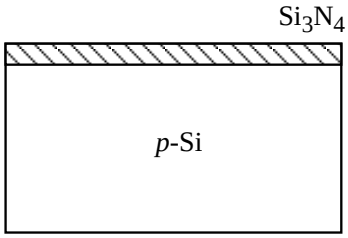
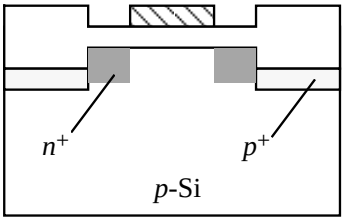
# A SIMPLE SCHEMATIC OF PROCESSES IN A MOSFET FABRICATION

Coat the entire wafer with $Si_3N_4$. $Si_3N_4$ is impervious to dopants.



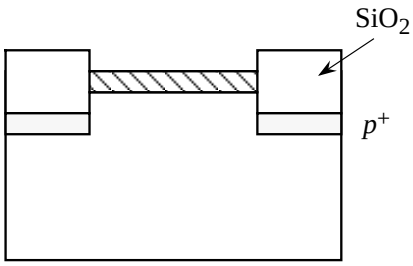

(a)

$n^+$ source and drain are produced by ion implantation.



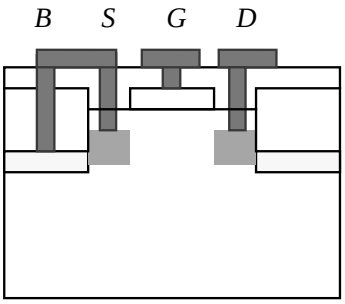

(d)

First mask: Define transistor area and remove $Si_3N_4$. Implant $p^+$ regions to serve as device isolation. Grow thick field oxide.



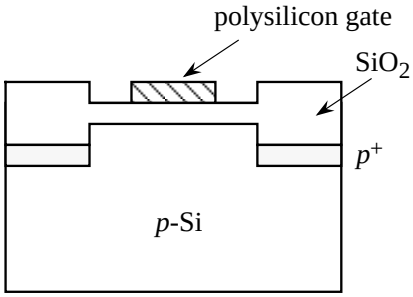

(b)

$SiO_2$ is deposited on the entire structure. A mask is used to open windows for contacts. Al is evaporated.



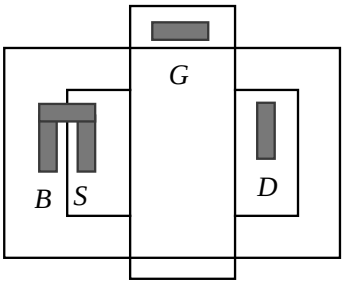

(e)

Etch $Si_3N_4$ and grow thin gate oxide. On the gate oxide, grow polysilicon and define the gate via a mask.




(c)

Top view of the device




(f)

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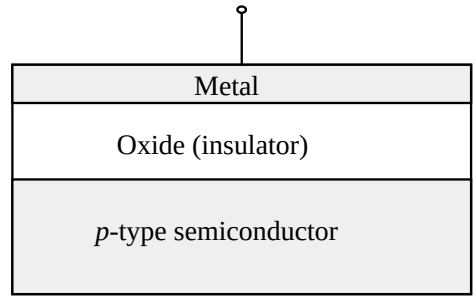
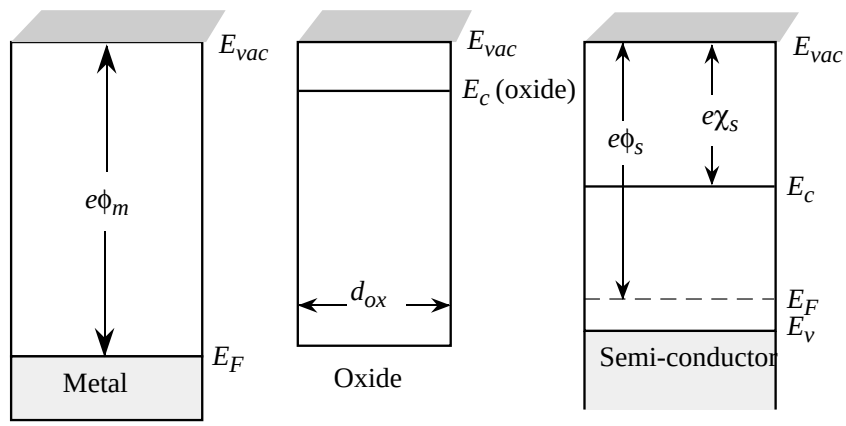
# BAND PROFILES IN A METAL, OXIDE, SEMICONDUCTOR, AND A MOS



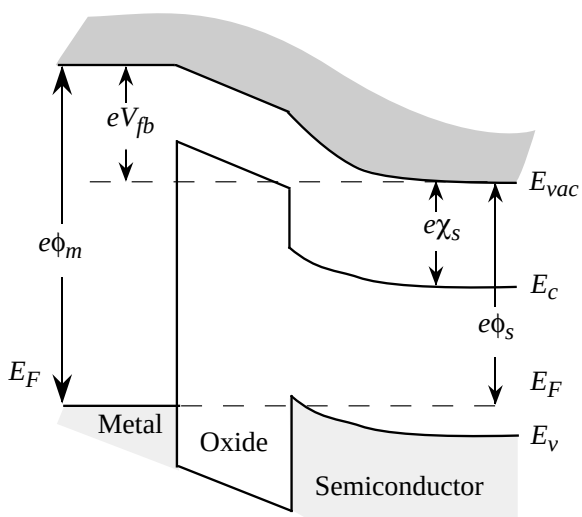

(a)

Band profiles in a metal, $SiO_2$, and $p$-Si.




(b)

Band profile in a MOS structure




$eV_{fb} = e\phi_m - e\phi_s$

(c)

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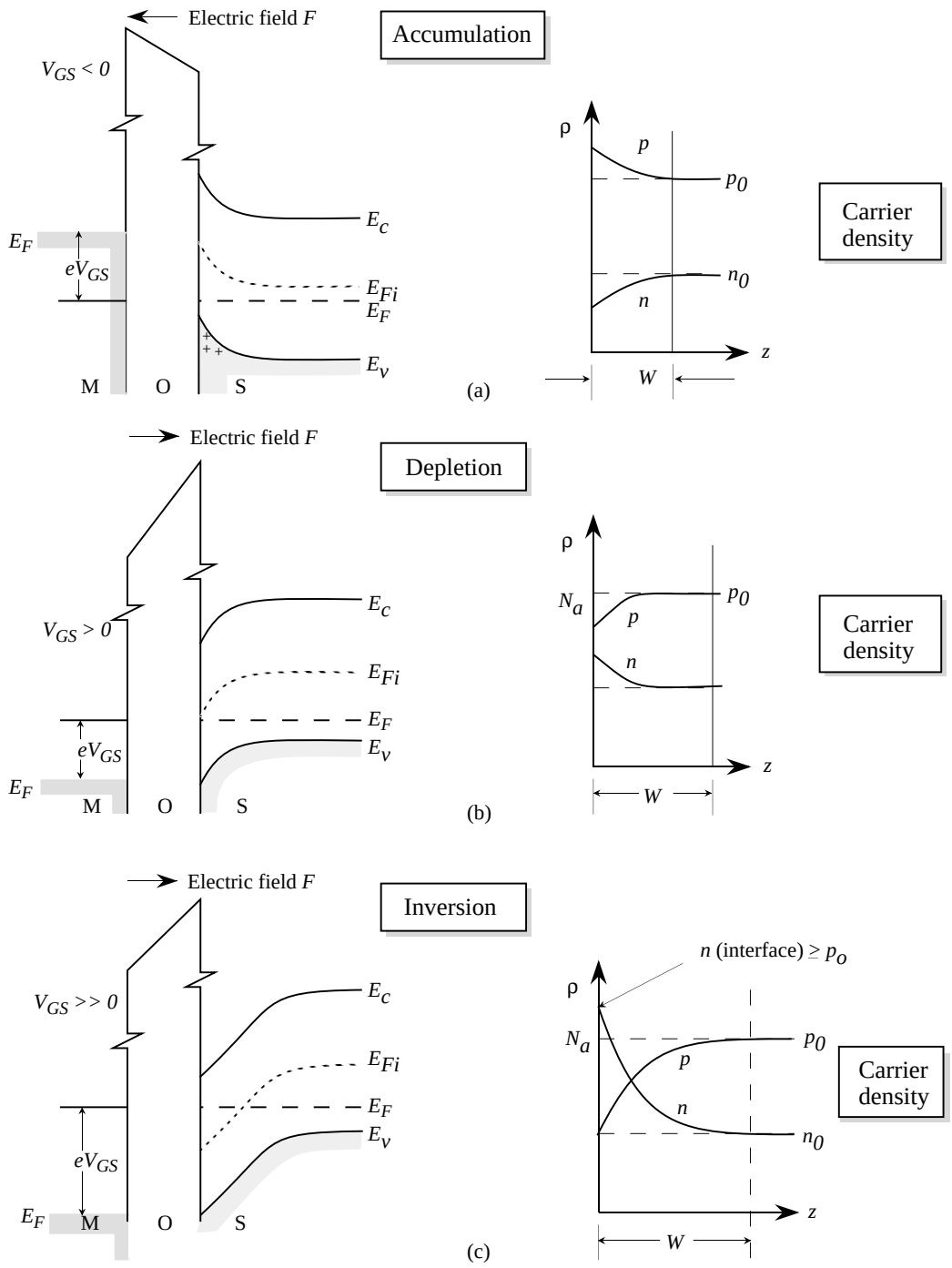
# BAND PROFILES AND CARRIER DENSITY IN ACCUMULATION, DEPLETION AND INVERSION

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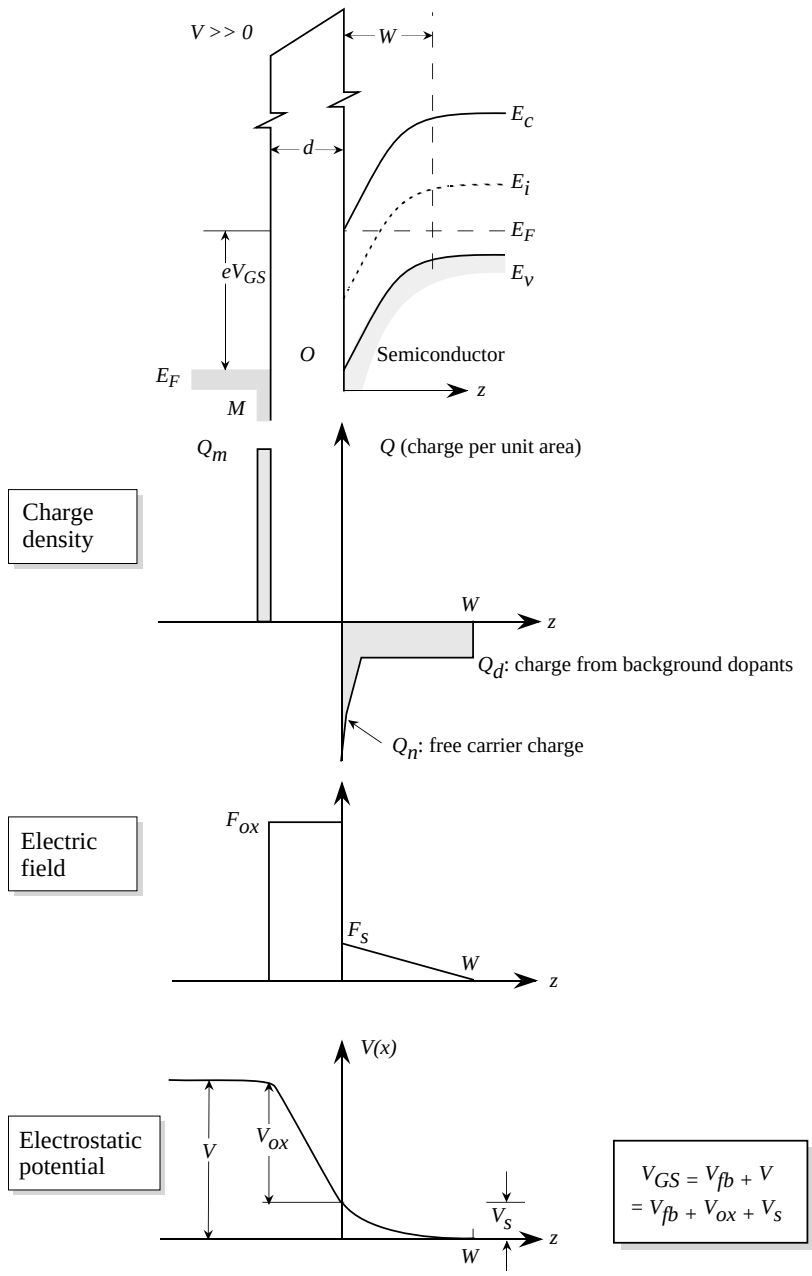
# An MOS structure under inversion




$$V_{GS} = V_{fb} + V$$
$$= V_{fb} + V_{ox} + V_s$$

$$W_{max} = \left(\frac{4\varepsilon_s|\phi_F|}{eN_a}\right)^{1/2} \quad ; \quad \phi_F = E_F - E_{Fi}$$

$$V_T = V_{fb} - 2\phi_F + \left[2e\varepsilon_s N_a\left|-2\phi_F + V_{SB}\right|\right]^{1/2}\frac{1}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}$$

$Q_{ss}$ = interface areal charge density

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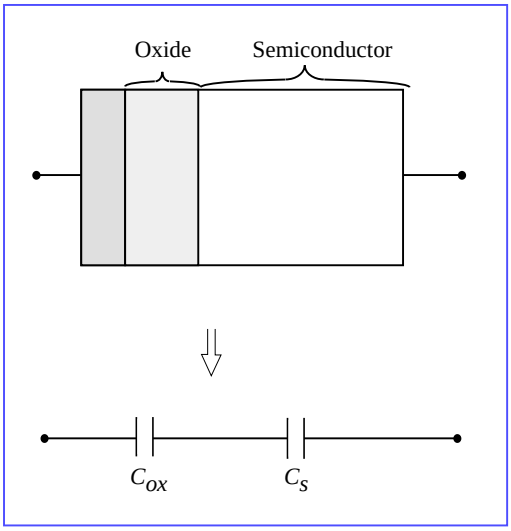
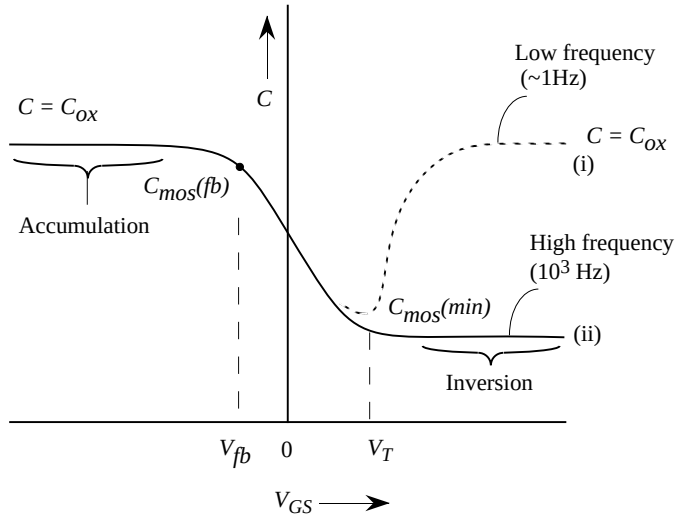
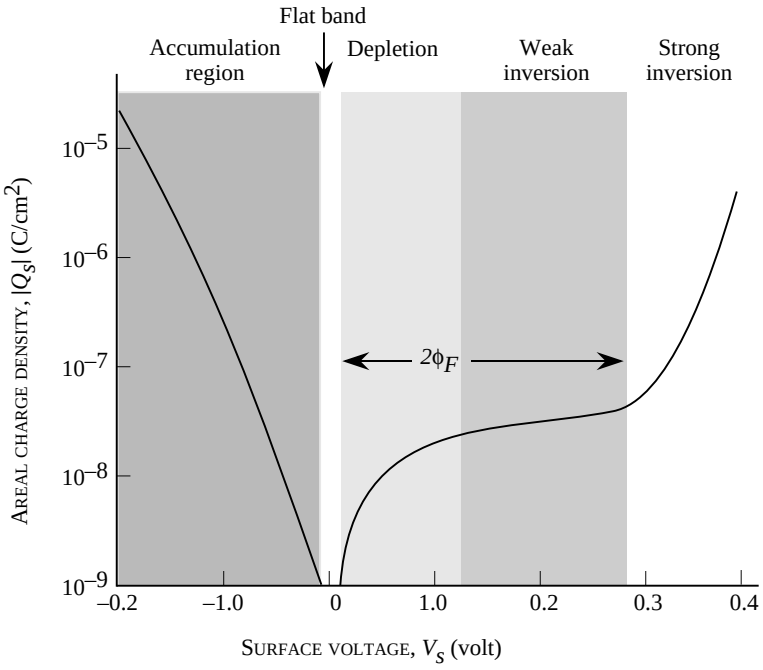
# CAPACITANCE-VOLTAGE RELATION IN




Once the MOS is in inversion, the sheet charge density increases rapidly with bias.

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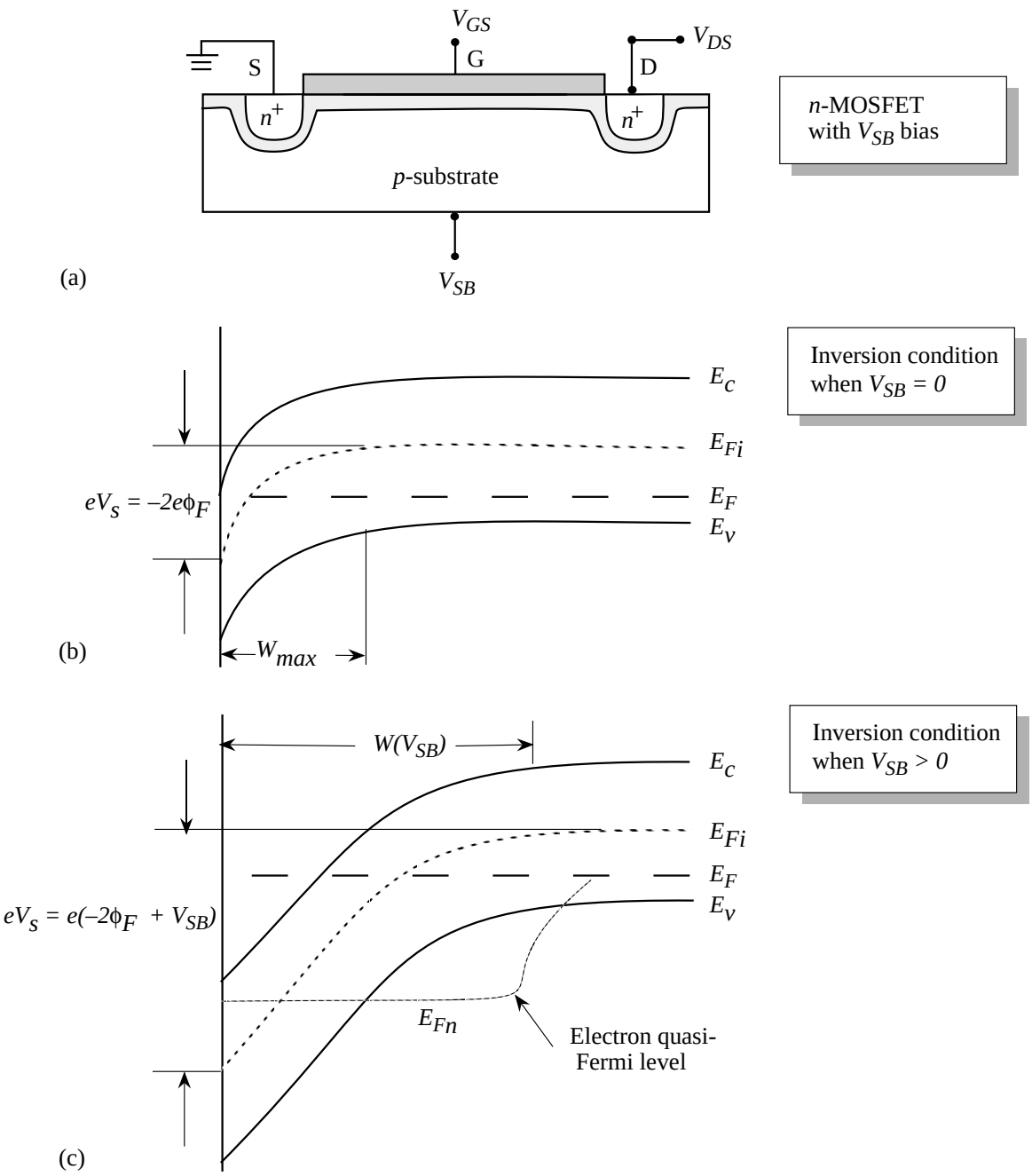
# EFFECT OF BODY BIAS ON MOSFET PROPERTIES




Shift in threshold voltage

$$\Delta V_T = \frac{2e\varepsilon_s N_a}{C_{ox}}\left[\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right]$$

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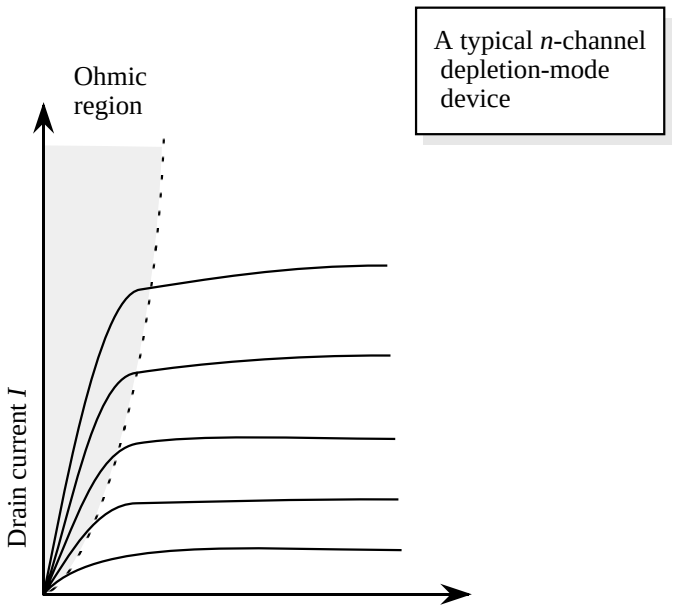


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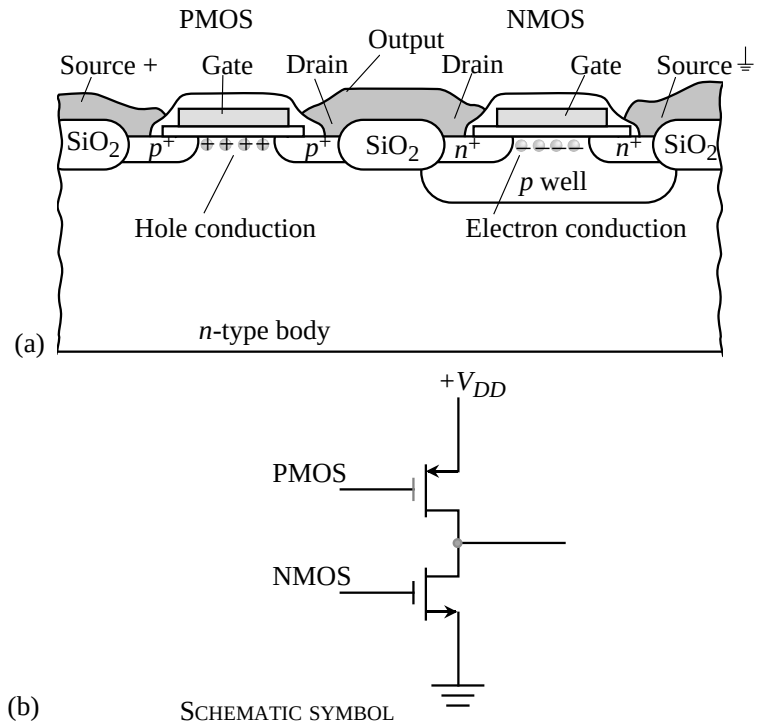
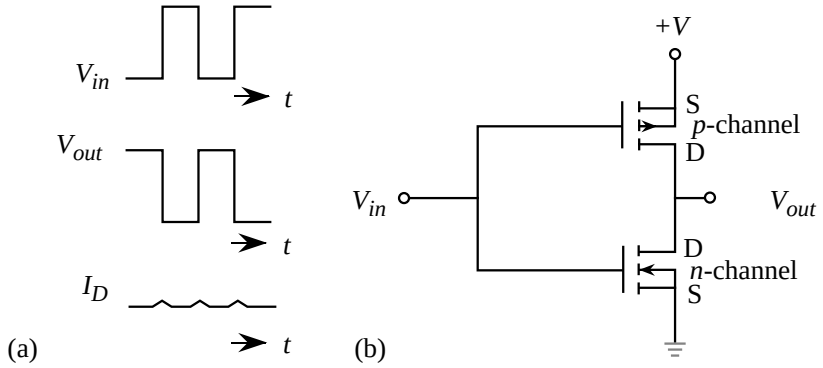
# COMLIMENTARY MOSFET: LOW POWER FET

By combining an NMOS and a PMOS a CMOS is constructed. Since only one device (NMOS or PMOS) conducts for any gate bias the CMOS does not draw any current and is very useful for low power applications.




(a) A cross-section of a CMOS device. (b) Symbol representing the CMOS.




(a) A complimentary MOS structure shown to function as an inverter. The circuit draws current only during the input voltage switching. (b) A schematic of the CMOS structure.

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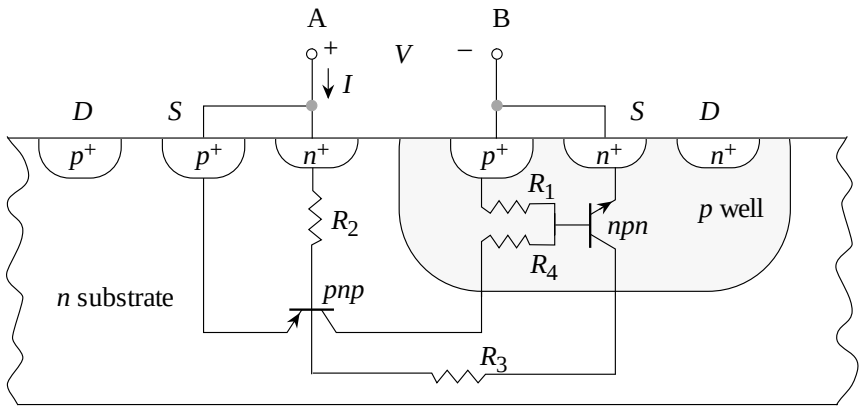
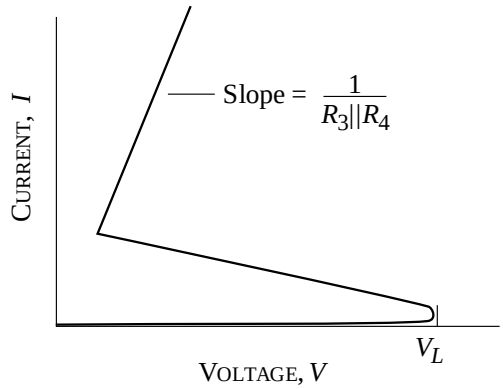
# LATCHUP PROBLEM IN CMOS TECHNOLOGY

The presence of *npn, pnp* bipolar pathways in a CMOS can lead to parasitic transistor action and unintentional current flows.




(a)




(b)

(a) A schematic of the parasitic effects that lead to CMOS latch-up problems.
(b) Current versus voltage effect. The onset of latch-up is represented by a sharp rise in the parasitic current.

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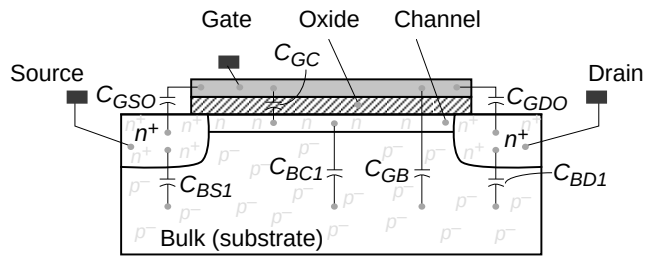
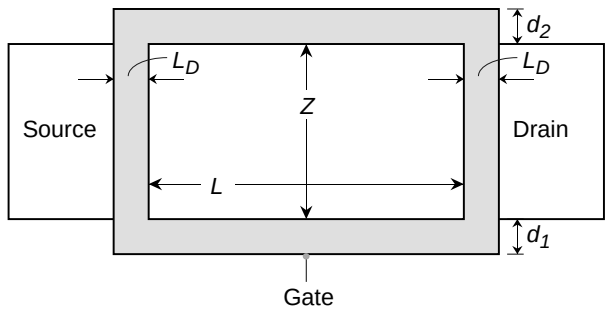
# CAPACITANCES OF IMPORTANCE IN A MOSFET




(a)

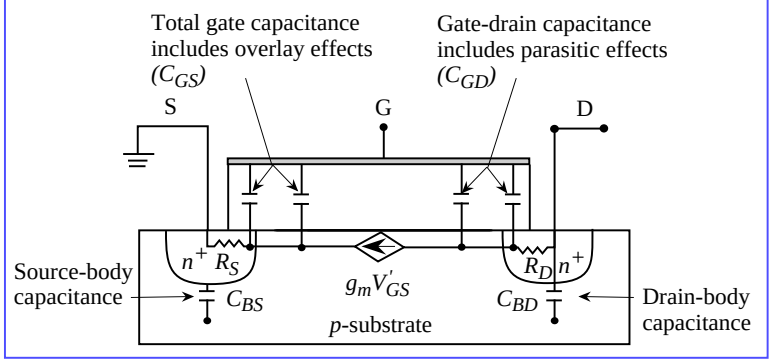



(b)

| | Region | | |
|---|---|---|---|
| | Cutoff | Ohmic | Saturation |
| $C_{GD}$ | $C_{ox} Z L_D$ | $C_{ox} Z L_D + 1/2\, ZL\, C_{ox}$ | $C_{ox} Z L_D$ |
| $C_{GS}$ | $C_{ox} Z L_D$ | $C_{ox} Z L_D + 1/2\, Z\, LC_{ox}$ | $C_{ox} Z L_D + 2/3\, Z\, LC_{ox}$ |
| $C_{BG}$ | $C_{ox} Z L$ | 0 | 0 |
| $C_{BD}$ | $C_{BD1}$ | $C_{BD1} + \frac{C_{BC1}}{2}$ | $C_{BD1}$ |
| $C_{BS}$ | $C_{BS1}$ | $C_{BS1} + \frac{C_{BC1}}{2}$ | $C_{BS1} + 2/3\, C_{BC1}$ |

(c)

A CIRUIT MODEL FOR A MOSFET




Miller capacitance:

$C_M + C_{GD}(1+g_m R_L)$

Cutoff frequency:

$f_T = \frac{g_m}{2\pi(C_{GS}+C_M)}$

Self-aligned gate technology to minimize $C_M$ or $C_{GD}$.

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# SCALING ISSUES IN MOSFET TECHNOLOGY

| PARAMETER | FULL SCALING | CONSTANT-VOLTAGE SCALING |
|---|---|---|
| Gate width, $Z$<br>Gate length, $L$<br>Oxide thickness, $d_{ox}$ | 1/S | 1/S |
| Drain bias, $V_{DS}$<br>Threshold bias, $V_T$ | 1/S | 1 |
| Oxide capacitance for the device | 1/S | 1/S |
| Drain current, $I_D$ | ~1/S | ~S |
| DC power consumption | ~$1/S^2$ | ~S |
| Device switching time | ~1/S | ~$1/S^2$ |
| Power-delay product | ~$1/S^3$ | ~1/S |

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# SEMICONDUCTOR INDUSTRY ASSOCIATES ROADMAP

| YEAR | 1997 | 1999 | 2001 | 2003 | 2006 | 2009 | 2012 |
|---|---|---|---|---|---|---|---|
| DRAM cell half-pitch (nm) | 250 | 180 | 150 | 130 | 100 | 70 | 50 |
| Gate length for MPU (nm) | 200 | 140 | 120 | 100 | 70 | 50 | 35 |
| Maximum substrate diameter (mm) | 200 | 300 | 300 | 300 | 300 | 450 | 450 |
| Acceptable defect density at 60% yield for DRAM | 2080 | 1455 | 1310 | 1040 | 735 | 520 | 370 |
| Defect density for MPU | 1940 | 1710 | 1510 | 1355 | 1120 | 940 | 775 |
| Power supply (V) | 1.8-2.5 | 1.5-1.8 | 1.2-1.5 | 1.2-1.5 | 0.9-1.2 | 0.6-0.9 | 0.5-0.6 |
| Power dissipation with heat sink (W) | 70 | 90 | 110 | 130 | 160 | 170 | 175 |
| Power dissipation without heat sink (for portable electronics) (W) | 1.2 | 1.4 | 1.7 | 2.0 | 2.4 | 2.8 | 3.2 |
| Cost per function DRAM (µcents/function) | 120 | 60 | 30 | 15 | 5.3 | 1.9 | 0.66 |
| Cost per function MPU (µcents/function) | 3000 | 1735 | 1000 | 580 | 255 | 110 | 49 |

KEY ISSUES: Gate tunneling current
Defect density
Interconnect delays will dominate

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