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**Technical Background and Career Objectives** I am looking for a R&D position to work on challenges of next-generation EDA software in logic and physical synthesis, formal verification, system reliability, and/or algorithms for multicore CPUs. My technical background in these diverse fields and extensive experience with EDA software, both as a user and as a developer, has allowed me to identify and demonstrate new, unexpected synergies that lead to faster and more reliable ICs, as well as more efficient verification. Results of this cross-disciplinary research have been published at competitive conferences (ICCAD, DATE, HPCA, ASP-DAC). Finally, my interests are not limited to my past work, and I would also enjoy learning about other upcoming EDA challenges.

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<b>Education</b>	Ph.D. in Comp. Science and Eng, University of Michigan Ann Arbor	May 2008
	MSE Comp. Science and Eng, University of Michigan (GPA: 8.0)	May 2004
	B.S.E. Comp. Eng, University of Michigan (GPA: 3.9– <i>Summa Cum Laude</i> )	May 2003

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**Research** **Dissertation: Simulation Driven Hierarchical Synthesis and Verification**  
(advisers: Prof. Igor Markov and Prof. Valeria Bertacco)

#### **Logic and Physical Synthesis**

As physical characteristics become a more dominant factor in determining circuit performance, achieving design closure requires logic optimizations that can utilize accurate physical information available late in the design flow. We introduce a post-placement logic resynthesis strategy that exploits logic flexibility through simulation-based approximations. In particular, we guide efficient local optimizations with flexible objectives using global information.

#### **Publications and software**

- "Optimizing Non-Monotonic Interconnect using Functional Simulation and Logic Restructuring," S. Plaza, I. Markov, and V. Bertacco, pp. 95-102, *ISPD*, 2008.  
**(Won Best Paper Award)**
- "Node Mergers in the Presence of Don't Cares," S. Plaza, K-H. Chang, I. Markov, and V. Bertacco, pp. 414-419, *ASP-DAC*, 2007.
- "Boolean Operations on Decomposed Functions," S. Plaza and V. Bertacco, pp. 310-317, *IWLS*, 2005.
- "STACCATO: Disjoint Support Decompositions from BDDs through Symbolic Kernels," S. Plaza and V. Bertacco, pp. 276-279, *ASP-DAC*, 2005.
- Public software (STACCATO): <http://www.eecs.umich.edu/vips/staccato/>

#### **Verification and Test**

The intractability of fully verifying large designs necessitates intelligent strategies for uncovering design bugs that elude engineer-specified test suites. We introduce verification coverage metrics which we use to guide constrained-random simulation. Our simulation strategy evenly stimulates a design to expose corner-case behavior.

#### **Publication**

"Random Stimulus Generation using Entropy and XOR Constraints," S. Plaza, I. Markov, and V. Bertacco, pp. 664-669, *DATE*, 2008.

### ***Analysis and Improvement of Circuit Reliability***

As device density increases, circuits become more susceptible to transient and permanent faults. We improve the reliability of a circuit by introducing techniques for automatically adding minimal amounts of redundancy. In particular, we expose combinational gate-level redundancies in logic to improve transient and permanent fault resilience.

#### ***Publications and Software***

- "Enhancing Design Robustness with Reliability-aware Resynthesis and Logic Simulation," S. Krishnaswamy, S. Plaza, I. Markov, and J. Hayes, pp. 149-154, *ICCAD*, 2007.
- "AnSER: A Lightweight Reliability Evaluator for use in Logic Synthesis," S. Krishnaswamy, S. Plaza, I. Markov, and J. Hayes, pp. 171-173, *IWLS*, 2007.
- "Architecting a Reliable CMP Switch Architecture," K. Constantinides, S. Plaza, J. Blome, B. Zhang, V. Bertacco, S. Mahlke, T. Austin, and M. Orshansky, Vol.4, No. 1, Article 2, *ACM Transactions on Architecture and Code Optimization*, March 2007.
- "BulletProof: A Defect Tolerant CMP Switch Architecture," K. Constantinides, S. Plaza, J. Blome, B. Zhang, V. Bertacco, S. Mahlke, T. Austin, and M. Orshansky, pp. 5-16, *HPCA*, 2006.
- "Assessing SEU Vulnerability via Circuit-Level Timing Analysis," K. Constantinides, S. Plaza, J. Blome, B. Zhang, V. Bertacco, S. Mahlke, T. Austin, and M. Orshansky, *Workshop on Architectural Reliability*, 2005.
- Public software (AnSER): to be part of OAGear (<http://opendatools.si2.org/oagear/>)

#### ***Algorithms for Distributed and Parallel EDA Tools***

As the growing complexity of IC designs challenges the scalability of CAD tools, commercial EDA development must embrace multicore systems, which have recently reached dominance in the server, workstation and desktop segments. However, the efficiency of CAD tools often depends on the throughput in solving multiple instances of computationally-hard problems. We introduce a priority-based scheduler, along with intelligent parallelization strategies, to efficiently solve multiple SAT problem instances on multicore systems.

#### ***Publications***

- "Low-latency SAT Solving on Multicore Processors with Priority Scheduling and XOR Partitioning," S. Plaza, I. Markov, and V. Bertacco, *to appear in IWLS*, 2008.
- "Advances and Insights into Parallel SAT Solving," S. Plaza, I. Kountanis, Z. Andraus, V. Bertacco, and T. Mudge, pp. 188-194, *IWLS*, 2005.

#### **Background and Training**

- EDA courses taken<sup>1</sup>: logic synthesis (EECS 478), verification (EECS 578), physical design (EECS 527), compilers and architecture (EECS 570, 573, 583), algorithms (EECS 586)
- Experience
  - synthesis tools: DesignCompiler (Synopsys), ABC & SIS (Berkeley)
  - placement tools: Capo (UCLA & Michigan)
  - industry data models and databases: OpenAccess (Si2)
  - industry EDA software: OAGear (2nd place IWLS 2007 programming contest)
- Software development using the binary decision package CUDD
- Software development using the SAT solvers MiniSAT and zChaff
- Teaching (graduate student instructor): object oriented programming (EECS 381)—3 semesters, logic synthesis (EECS 478)—2 semesters
- Grading: introduction to electronic circuits (EECS 215)

#### **Activities**

- Organized weekly reading group on synthesis, verification, and test
- Service: reviewer for DAC, TCAD, TODAES; member of Eta Kappa Nu
- Personal: volunteer weekly at hospital; member of roller-hockey league

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<sup>1</sup> All course numbers given refer to the University of Michigan course catalogue