



# **PowerAnalyzer for Pocket Computers**

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**University of Michigan**

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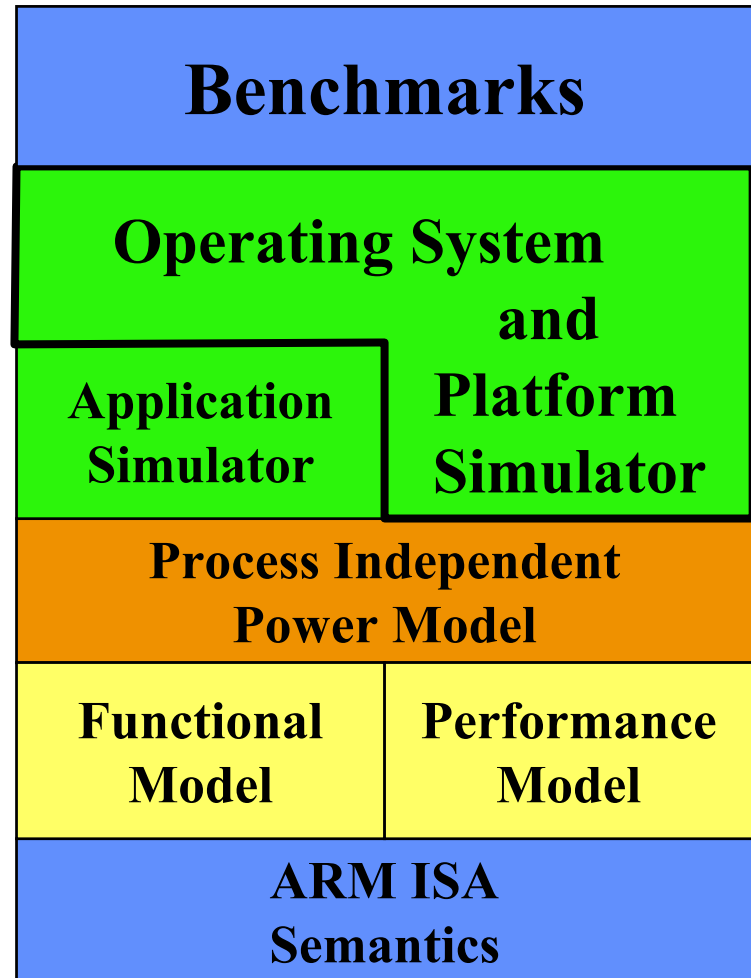
**University of Colorado**



# Project Overview



- **Project Goal**
  - Develop the first high-performance validated architectural-level power model of a power-sensitive embedded target
- **PowerAnalyzer**
  - Cycle-level architectural simulator for early power/performance studies
  - Calibrated against detailed physical models and real systems (Compaq Itsy & iPAQ)
- **Deliverables**
  - SimpleScalar ARM simulator and iPAQ device performance models
  - MiBench embedded benchmark suite
  - PowerAnalyzer technology integrated into SimpleScalar/ARM models
- **Additional Research Items**
  - Architectural Slack Scheduling
  - Operating support for Dynamic Voltage Scheduling





# Team Members



## ■ University of Michigan

- Trevor Mudge
- Todd Austin
- Students:
  - Rajeev Krishna
  - Nam Kim
  - Jeff Ringenberg

## ■ University of Colorado

- Dirk Grunwald
- Students:
  - Soraya Ghiasi
  - Jason Casmira

## ■ Industrial Partners

- Intel
  - Support for two students
  - Mentors George Cai (Texas),  
Doug Carmean and Rich Uhlig (Portland)  
Chris Newburn (Santa Clara)  
Mike Morrow (Chandler, AZ)
- Cobalt Networks
  - Equipment for System Level modeling & optimization
- Compaq Computer
  - Itsy motherboards (V1.5 & V2)



## ■ Validated core ARM components

- ARM 7 and FPA emulation, SA-pipeline, memory system, basic I/O
- ARM cross-compiler kit now available, with pre-built libraries
- Download from <http://www.eecs.umich.edu/~taustin/simplescalar>
- Used by 7 PACC groups

## ■ Validation effort

- Functional validation via random testing
  - 500+ billion instructions tested against ARMulator and SA-1110 references
  - 6 bugs found in the ARMulator! (reported to ARM Ltd)
- Performance validation via micro/macro-benchmark testing
  - Against SA-1110 reference hardware using cycle counter

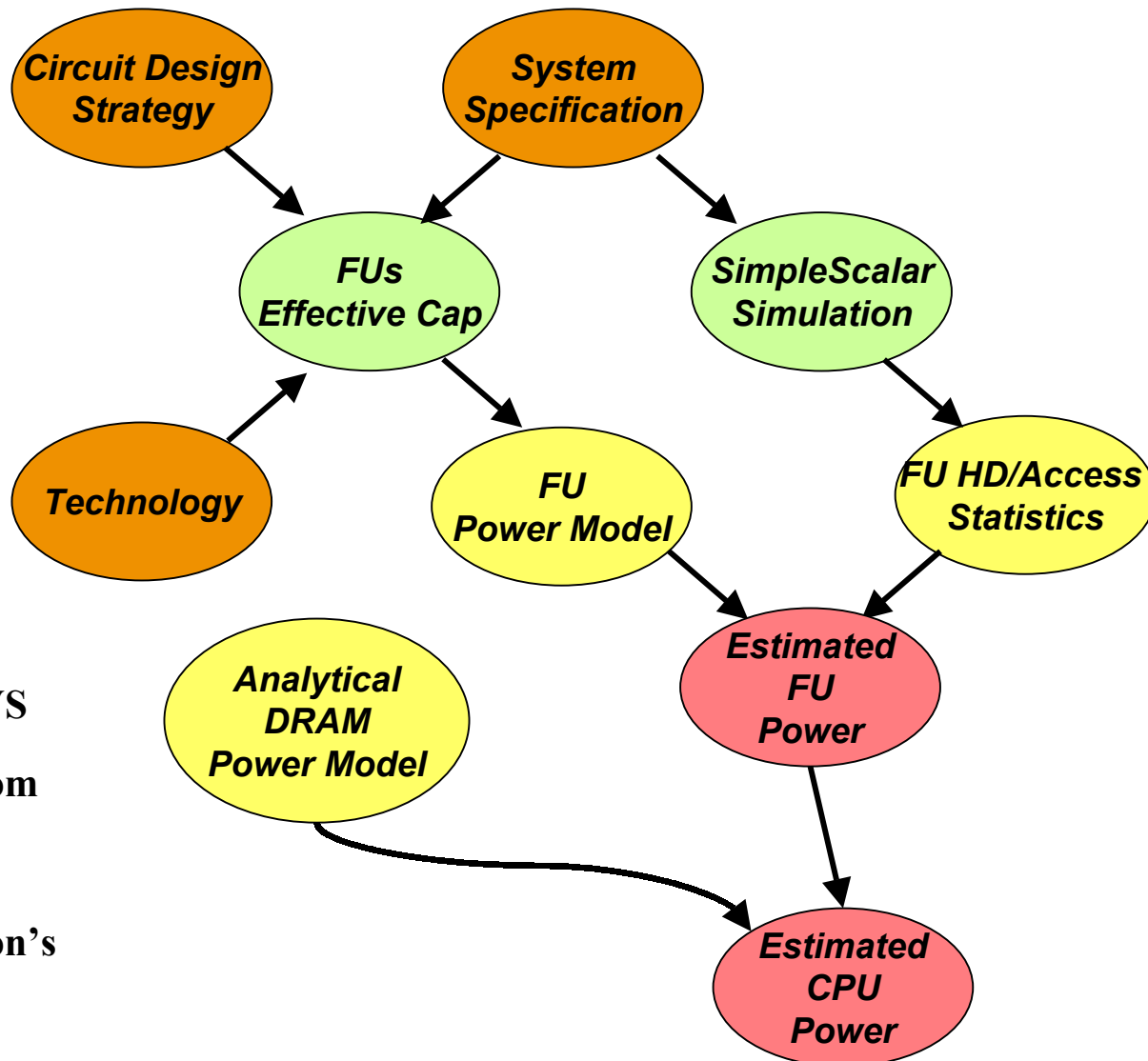
	Benchmark	SimpleScalar	SA-1110	% Difference
microbenchmarks	cache_hit	1.02	1.01	0.9
	cache_miss	33.87	33.70	0.5
	br_taken	1.04	1.02	1.9
	br_nottaken	1.97	1.91	3.1
	bzip2 10	3.20	3.10	3.2
	cc1 -O cc1in.i	2.84	2.90	2.1
	fft short.pcm	1.45	1.44	0.1
	macrobenchmarks			



# Functional Unit Power Model



- Value-sensitive activity based model
  - Similar to Wattch, Cai & Lim
  - Include grey-coded value sensitive modeling of cache
- “Open” validation process
  - Netlist extraction from Verilog ARM model
  - Functional Unit Power analysis using Synopsys PowerGate
- Support for Dynamic Voltage Scaling
  - Simulated “syscall” for DVS control - power values extrapolated using data from LART group
- Analytical DRAM model
  - Adding support for Infineon’s “Mobile DRAM”

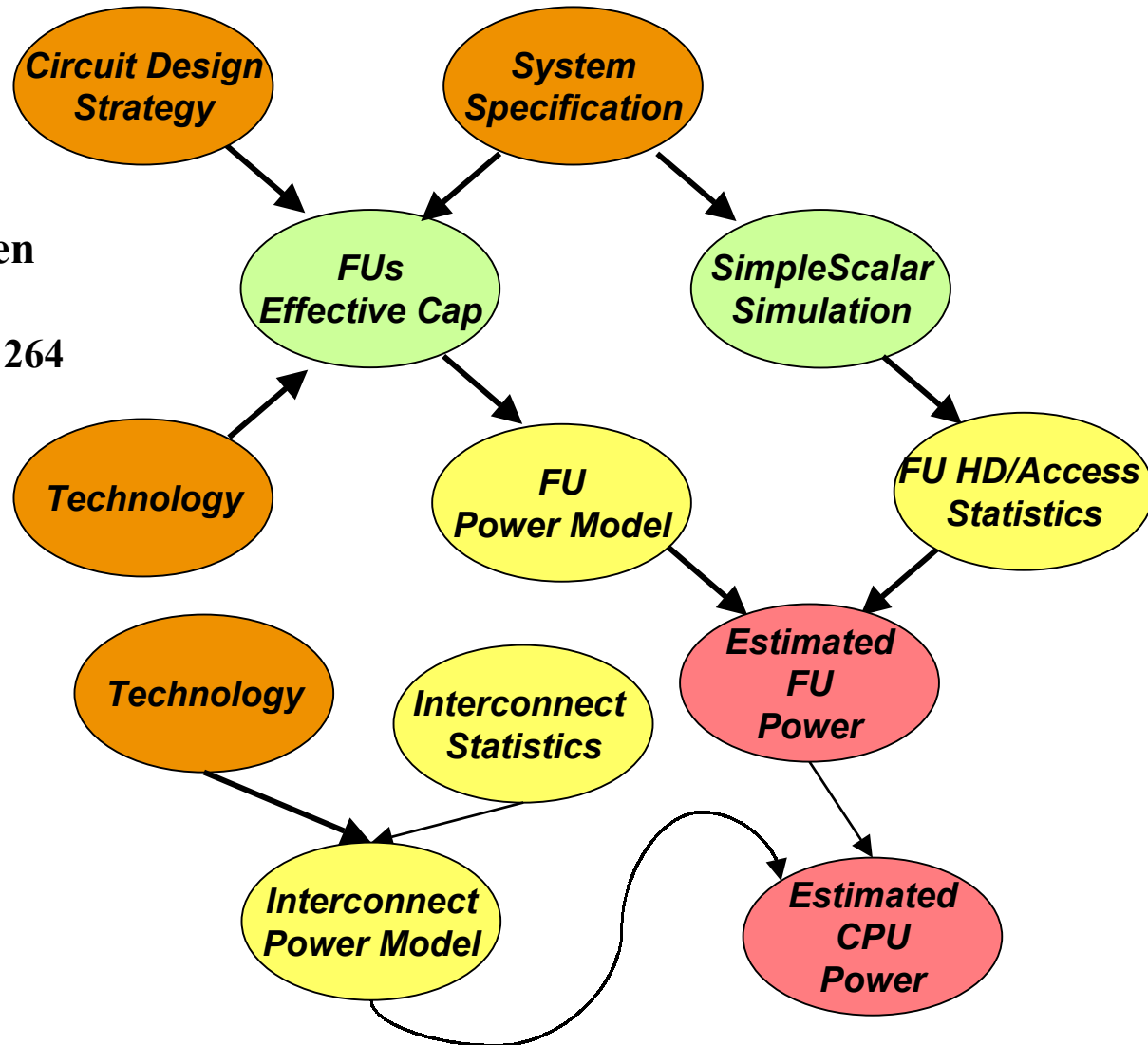




# Adding Interconnect Power Model



- Interconnect & clock distribution need floor-plan estimates
- Significant variance between major processor variants
  - E.g. PentiumPro vs. Alpha 264
- Use analytical models (Rents Rule) for interconnect



## ■ System simulation development

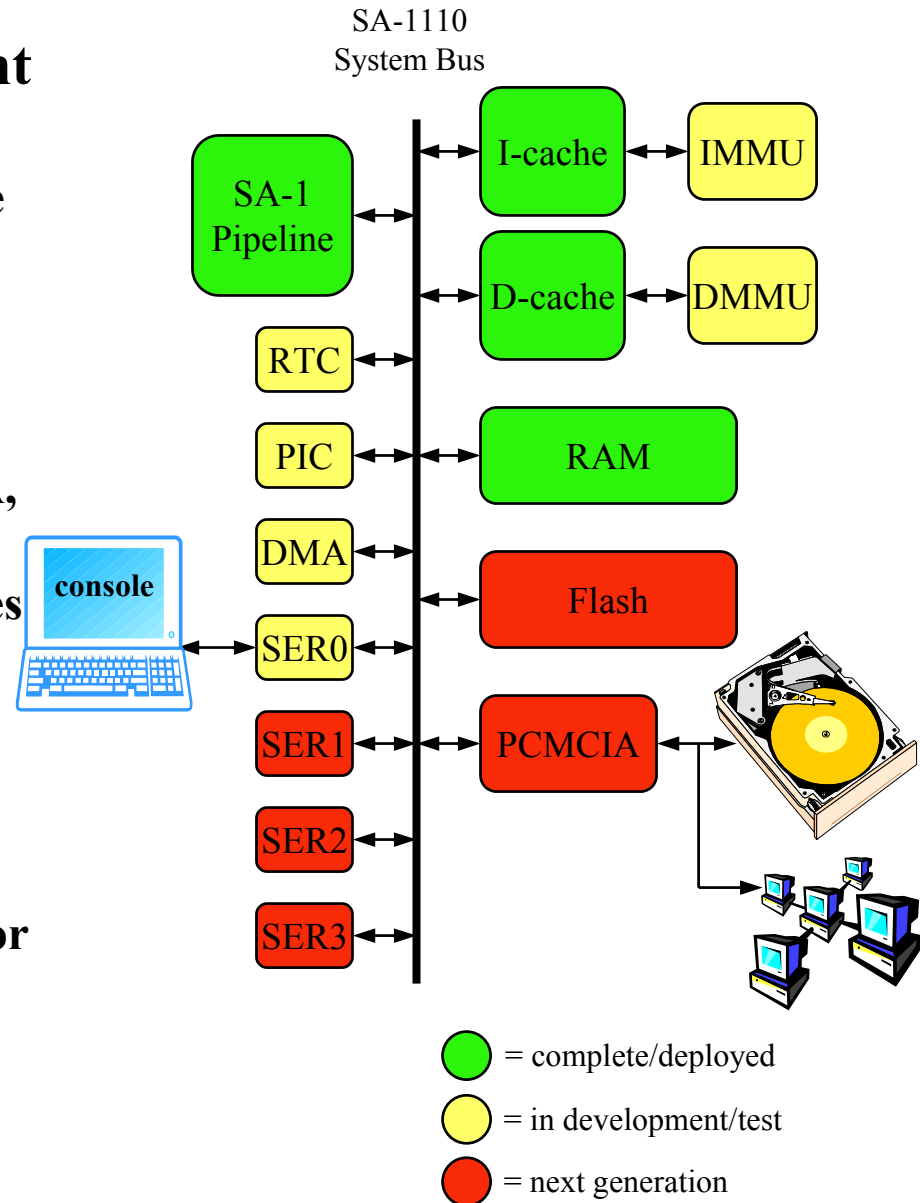
- SA-1110 device set
- Compaq IPaq reference hardware
- Linux + MiBench workload

## ■ Status

- Core components deployed
- Virtual memory, RTC, PIC, DMA, SER0 development ongoing
- Booting Linux kernel only requires serial, DMA, PIC, RTC, MMU

## ■ Concurrent Development

- Develop SA-1100 specific devices
- Integrate Bochs platform simulator

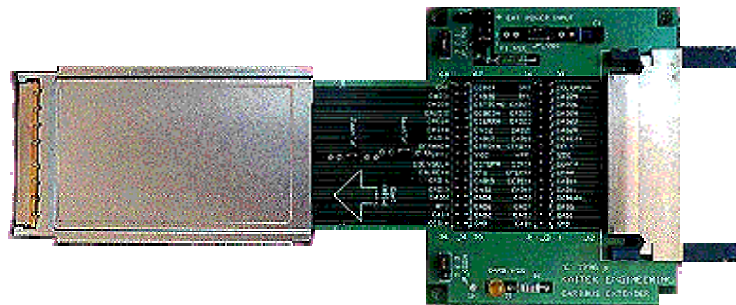


## ■ Bochs Platform Simulator

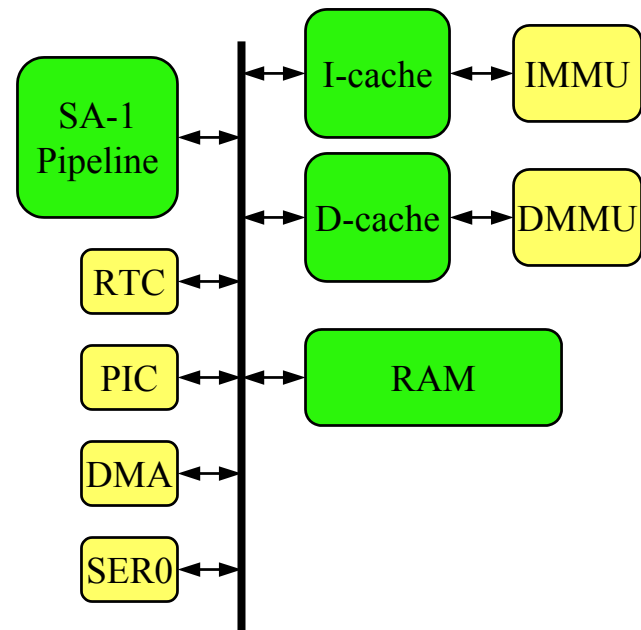
- Liberally harvesting components from “Bochs” x86 platform simulator
- Functional models for IDE, Ethernet, VGA, Cdrom, *etc*
- Goal: Common devices & interfaces across x86 & ARM simulators

## ■ Augmenting Devices with Approximate Power Models

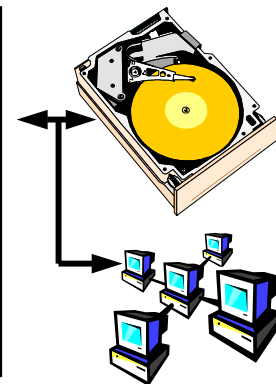
- Empirical measurements of 802.11, microdrive, flash, *etc.*



SA-1110  
System Bus



**Bochs  
Device  
Model**

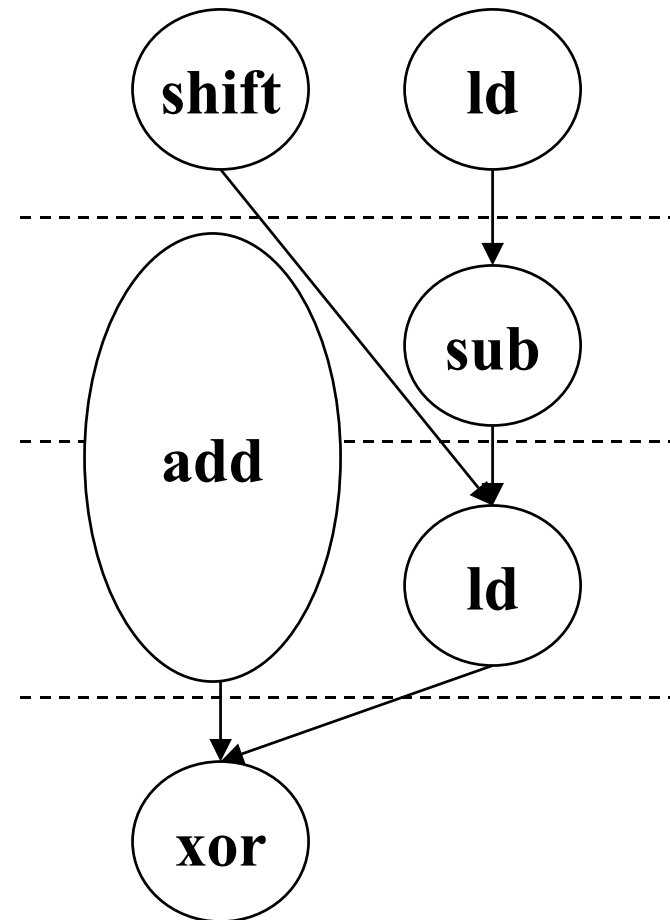




# Test Drive: Slack Scheduling



- Program dependence & machine constrains mean some instructions have “scheduling slack”
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  - Add can execute in cycle 2 or 3
- Alternatively, add can execute during both cycles
  - Slower component
  - Simpler component
- About 15-55% of all integer instructions can execute in 2 cycles w/o performance penalty





# Test Drive: DVS Scheduling



## Colorado

- **Extend interval methods (OSDI'00)**
  - PID controller w/optional signal for responsiveness
  - Accurately hits rate based applications w/o real time interface
- Implementation on SA-1100, AMD K6
  - Allows comparison to RTLinux
- Multi-architecture DVS interface

## Michigan

- Use models of process interaction
- Daemon mediates voltage scaling
- Implementation on TransMeta

•Application  
(optional hints – “I’m Important”)

•GUI Library  
(optional hints)

•Application  
(optional hints)

Vertigod daemon

•User-mode process.  
•Implements performance-setting algorithm.

## Linux Kernel

H  
O  
O  
K  
S

D  
V  
S

Modular Scheduler  
•Policy Daemon  
•Event tracing.  
•/proc interface.

## Linux Kernel

H  
O  
O  
K  
S

Vertigo Module

•Episode detection & tracking.  
•Comm. with policy daemon.  
•Event tracing.  
•/proc interface.



# Schedule & Releases



2000	H2	SA-1 processor core simulator Component-level power design
2001	H1	SA-1110 processor simulator Power model calibration & integration
	H2	System-level simulator (iPAQ running Linux) Whitebox calibration of existing design (MARM)
2002	H1	Demonstration experiments with Power Analyzer Blackbox calibration of pocket computer (iPAQ)

- **SS/ARM available since mid-November, used by 7 PACC groups**
- **Power model design nearly completed**
  - **Pending: Integration of DVS, DRAM power, Interconnect, framework for external device power**
- **Platform simulator on-target for end-of-summer / early fall**
  - **Initial release targets SA-1100, later release for full system**
- **DVS interface available for SA-1100, AMD K6 w/PowerNow! (untested module for Xscale, IP issue with SpeedStep?)**
- **Validation target moving to Xscale w/help from Intel**



# Publications



- T. Mudge. *Power: A first class design constraint*. Computer, vol. 34, no. 4, April 2001, pp. 52-57.
- T. Mudge. *Power: A first class design constraint for future architectures*. Proc. 7th Int. Conf. on High Performance Computing - HiPC, (Springer Lecture Notes in Computer Science), Dec. 2000, Bangalore, India, pp. 215-224.
- K. Flautner, S. Reinhardt, and T. Mudge. *Thread-level parallelism and interactive performance of desktop applications*. 9th Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-IX), Nov. 2000, pp. 129-138.
- Jason Casmira & Dirk Grunwald, *Dynamic Instruction Scheduling Slack*, Proceedings of the 2000 KoolChips workshop, held in conjunction with MICRO-00
- Soraya Ghiasi, Dirk Grunwald, *A Comparison of Two Architectural Power Models*, In Proceedings, Power Aware Computer Systems Workshop
- Soraya Ghiasi, Jason Casmira & Dirk Grunwald, *IPC Matching Mechanisms: Using IPC Variation in Workloads with Externally Specified Rates to Reduce Power Consumption* 2000 Workshop on Complexity Effective Design
- Dirk Grunwald, Phil Levis, Brad Morrey & Mike Neufeld, *Policies for Dynamic Clock Scheduling*, Proceedings of the 2000 Operating Systems Design and Implementation
- Farkas et. al, *Quantifying the Energy Consumption of a Pocket Computer and Java Virtual Machine*, Proceedings of the 2000 SIGMETRICS Conference on Computer System Performance