Power Analyzer

Trevor Mudge
Todd Austin
University of Michigan

Industrial Partners

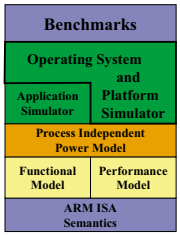
- Intel
  - Support for two students
  - Mentors George Cai (Texas), Doug Carmean and Rich Uhlig (Portland), Chris Newburn (Santa Clara), Mike Morrow (Chandler,AZ)
- Cobalt Networks
  - Equipment for System Level modeling & optimization
- Compaq Computer
  - Itsy motherboards (V1.5 & V2)

Dirk Grunwald
University of Colorado

Extending Widely Used Architectural Simulartor Toolkit

Project Overview

- Project Goal
  - Develop the first high-performance validated architectural-level power model of a power-sensitive embedded target
- PowerAnalyzer
  - Cycle-level architectural simulator for early power/performance studies
  - Calibrated against detailed physical models and real systems (Compaq Itsy & iPAQ)
- Deliverables
  - SimpleScalar ARM simulator and iPAQ device performance models
  - MiBench embedded benchmark suite
  - PowerAnalyzer technology integrated into SimpleScalar/ARM models
- Additional Research Items
  - Architectural Slack Scheduling
  - Operating support for Dynamic Voltage Scheduling



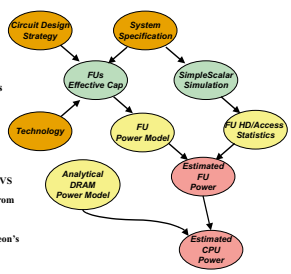
SimpleScalar/ARM Second Release

- Validated core ARM components
  - ARM 7 and FPA emulation, SA-pipeline, memory system, basic I/O
  - ARM cross-compiler kit now available, with pre-built libraries
  - Download from http://www.eecs.umich.edu/~taustin/simplescalar
  - Used by 7 PACC groups
- Validation effort
  - Functional validation via random testing
    - 500+ billion instructions tested against ARMulator and SA-1110 references
    - 6 bugs found in the ARMulator! (reported to ARM Ltd)
  - Performance validation via micro/macro-benchmark testing
    - Against SA-1110 reference hardware using cycle counter

Benchmark	SimpleScalar	SA-1110	% Difference
cache_hit	1.02	1.01	0.9
cache_miss	33.87	33.70	0.5
br_taken	1.04	1.02	1.9
br_nottaken	1.97	1.91	3.1
bzip2 10	3.20	3.10	3.2
cc1 -O cc1in.i	2.84	2.90	2.1
fft short.pcm	1.45	1.44	0.1

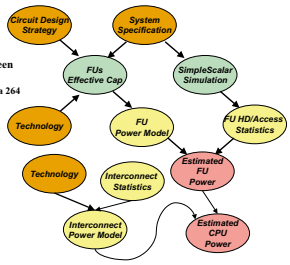
Functional Unit Power Model

- Value-sensitive activity based model
  - Similar to Wattch, Cai & Lim
  - Include grey-coded value sensitive modeling of cache
- "Open" validation process
  - Netlist extraction from Verilog ARM model
  - Functional Unit Power analysis using Synposys PowerGate
- Support for Dynamic Voltage Scaling
  - Simulated "syscall" for DVS control - power values extrapolated using data from LART group
- Analytical DRAM model
  - Adding support for Infineon's "Mobile DRAM"



Adding Interconnect Power Model

- Interconnect & clock distribution need floor-plan estimates
- Significant variance between major processor variants
  - E.g. PentiumPro *vs.* Alpha 264
- Use analytical models (Rents Rule) for interconnect

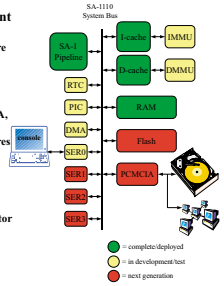


Value Sensitive Activity Model with Components Extracted From Michigan "ARM-like" design

Using Proven Application Simulator & Extending to Platform Simulator

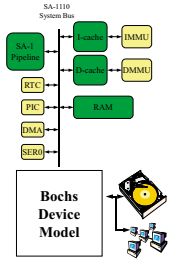
SimpleScalar/ARM System Simulation

- System simulation development
  - SA-1110 device set
  - Compaq IPaq reference hardware
  - Linux + MiBench workload
- Status
  - Core components deployed
  - Virtual memory, RTC, PIC, DMA, SER0 development ongoing
  - Booting Linux kernel only requires serial, DMA, PIC, RTC, MMU
- Concurrent Development
  - Develop SA-1100 specific devices
  - Integrate Bochs platform simulator



SimpleScalar/ARM Platform Simulation

- Bochs Platform Simulator
  - Liberally harvesting components from "Bochs" x86 platform simulator
  - Functional models for IDE, Ethernet, VGA, Cdrom, *etc*
  - Goal: Common devices & interfaces across x86 & ARM simulators
- Augmenting Devices with Approximate Power Models
  - Empirical measurements of 802.11, microdrive, flash, *etc.*



Test Drive: Slack Scheduling

- Program dependence & machine constrains mean some instructions have "scheduling slack"
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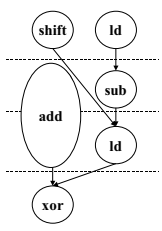
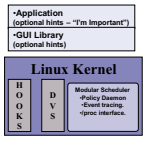
  - Add can execute in cycle 2 or 3
- Alternatively, add can execute during both cycles
  - Slower component
  - Simpler component
- About 15-55% of all integer instructions can execute in 2 cycles w/o performance penalty



Test Drive: DVS Scheduling

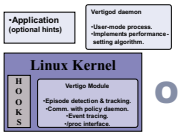
Colorado

- Extend interval methods (OSDI'00)
  - PID controller w/optional signal for responsiveness
  - Accurately hits rate based applications w/o real time interface
- Implementation on SA-1100, AMD K6
  - Allows comparison to RTLinux
- Multi-architecture DVS interface



Michigan

- Use models of process interaction
- Daemon mediates voltage scaling
- Implementation on TransMeta



"Test Driving" Infrastructure via Microarchitectural and Operating Systems Research

2000	H2	SA-1 processor core simulator Component-level power design
2001	H1	SA-1110 processor simulator Power model calibration & integration
	H2	System-level simulator (iPAQ running Linux) Whitebox calibration of existing design (MARM)
2002	H1	Demonstration experiments with Power Analyzer Blackbox calibration of pocket computer (iPAQ)

- SS/ARM available since mid-November
- Power model design nearly completed
- Platform simulator on-target for end-of-summer / early fall
  - Initial release targets SA-1100, later release for full system
- DVS interface available for SA-1100, AMD K6 w/PowerNow!
- Validation target moving to Xscale w/help from Intel

Publications

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- Jason Casmira & Dirk Grunwald, Dynamic Instruction Scheduling Slack, Proceedings of the 2000 KoolChips workshop, held in conjunction with MICRO-00
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- Farkas et. al, Quantifying the Energy Consumption of a Pocket Computer and Java Virtual Machine, Proceedings of the 2000 SIGMETRICS Conference on Computer System Performance